TMS320C672x DSP Real-Time Interrupt

Reference Guide

Literature Number: SPRU717
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Texas Instruments

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About this Manual

This document describes the operation of the Real-Time Interrupt (RTI) module in the TMS320C672x digital signal processors (DSPs) . This document contains the following chapters:

- Chapter 1 provides information about the features, purpose and use of the RTI.
- Appendix A provides a list of registers and register descriptions that are used in RTI.

Notational Conventions

This document uses the following conventions:

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in chapter and described in tables
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

TMS320C672x DSP Peripherals Overview Reference Guide (literature number SPRU723) describes peripherals available on the TMS320C672x™ DSPs.

TMS320C6000 Technical Brief (literature number SPRU197) gives an introduction to the TMS320C62x™ and TMS320C67x™ DSPs, development tools, and third-party support.

TMS320C672xDSP CPU and Instruction Set Reference Guide (literature number SPRU733) describes the TMS320C672x™ CPU architecture, instruction set, pipeline, and interrupts for these digital signal processors.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000 DSPs and includes application program examples.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

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TMS320C672x DSP Real-Time Interrupt (RTI)

This document describes the functionality of the Real-Time Interrupt Module used in TMS320C672x DSPs.

Topic **Page**

1.1 Introduction

The Real-Time Interrupt Module (RTI) provides general-purpose timer functionality. Two examples of how the timer may be used are for operating systems and for benchmarking code. For operating systems, the module incorporates several counters which define the timebases needed for scheduling. For benchmarking, the timers give the ability to read the counter contents at the beginning and the end of the code to be benchmarked.

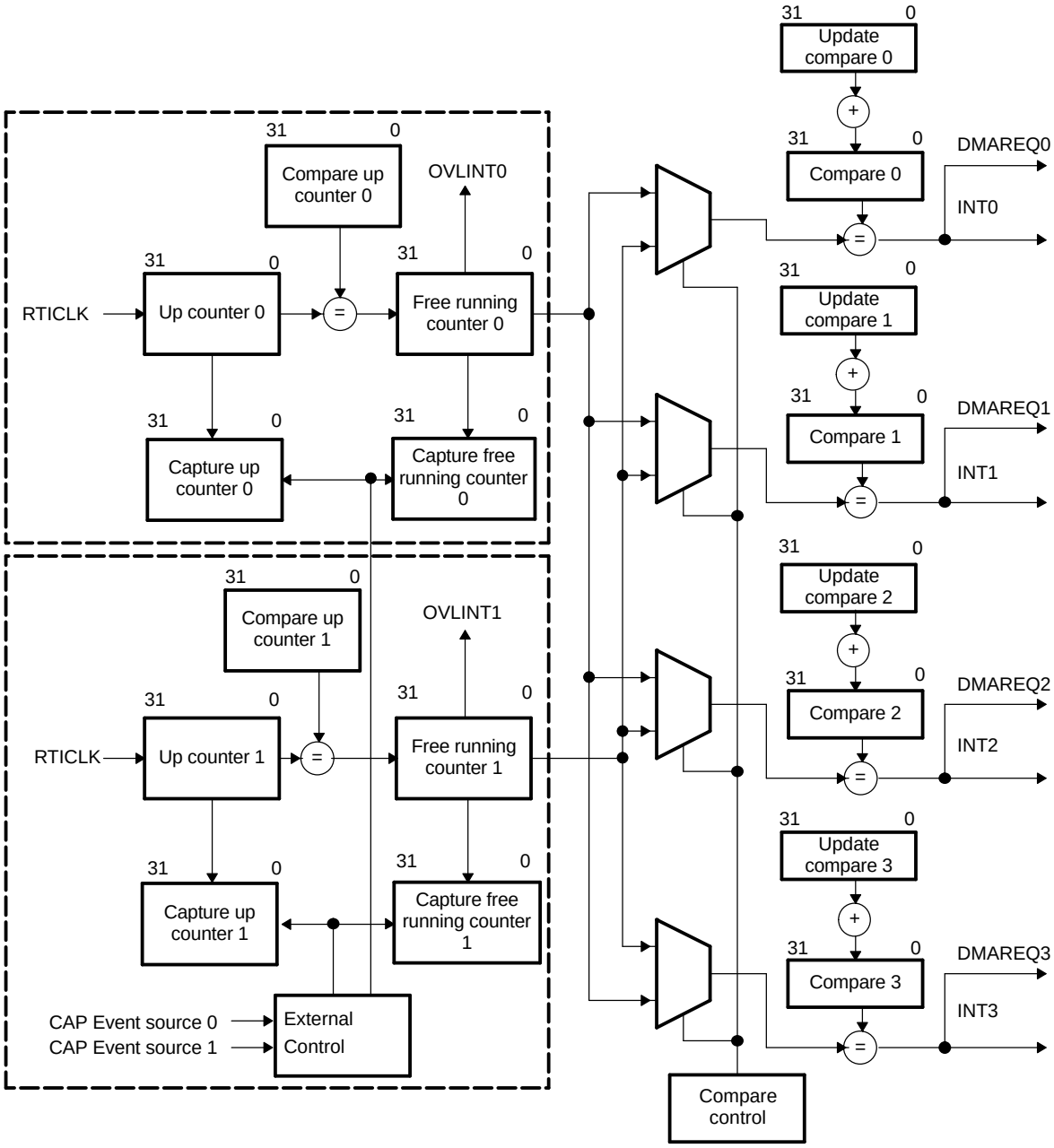
1.1.1 Main Features

- Two independent counter blocks for generating different timebases
  - Each block consists of
    - One 32-bit prescale counter
    - One 32-bit free-running counter
    - Two capture registers for capturing the prescale and free-running counter on a special event
- Free-running counters 0 and 1 can be incremented by the internal prescale counter
- Four configurable compare registers for interrupt generation, working either with counter 0 or counter 1. Compare 0 to 3 can also generate DMA request signals
- Automatic update of all compare registers on compare match to generate periodic interrupts
- Fast enabling/disabling of interrupts
- Digital Watchdog
- RTI clock input (RTICLK) derived from SYSCLK2 (see the device's datasheet).

1.2 Block Diagram

The RTI block diagram is shown in Figure 1-1.

Figure 1-1. Block Diagram



1.3 Module Operation

1.3.1 Counter Operation

The two counter blocks provide the same base functionality. Each block consists of two 32-bit up-counters (Up-Counter and Free-Running Counter). The Up-Counter (UCx) is driven by the RTICLK and counts up until the compare value in the Compare Up-Counter register (CPUCx) is reached. When the compare matches, the second counter, the Free-Running Counter (FRCx), is incremented. At the same time, UCx is reset to zero. If FRCx overflows, an interrupt is generated.

When both counter values need to be determined, first the Free-Running Counter register must be read to serve as a baseline and to ensure consistency. Concurrently, on the CPU cycle on which the Free-Running Counter is read, the Up-Counter value is stored in the Up-Counter register. Finally, the newly updated Up-Counter register may be read.

Both blocks also provide a capture feature on external events. Two capture sources can trigger the capture event (i.e., the event that triggers block 0 or block 1 is configurable). The sources of the capture events should be configured in the device interrupt manager. Please see the device datasheet for more details. When the event is detected, UCx and FRCx are stored in the Capture Up-Counter (CAUCx) and Capture Free-Running Counter (CAFRCx) registers. The read order of the captured values has to be in the same order as the actual counters. So, the CAFRCx must be read first and the CAUCx register must be read after the CAFRCx value is determined. While the CAFRCx is read, the CAUCx value is loaded into a shadow register to ensure data consistency. This action is necessary because, if another capture event happens during the two reads of captured data, and the application fails to read the two registers before a second capture event happens, the previous data will be overwritten.

Four Compare registers (CPx) are available to generate interrupt requests and/or DMA events to the device. Each of the Compare registers can be configured to work with either FRC0 or FRC1. When the Free-Running Counter value matches the Compare value, an interrupt and/or DMA event is generated. All Compare registers provide an additional feature. When a match occurs, the value in the Update Compare register (UDCPx) is added to the value in the Compare registers (CPx). This enables periodic interrupts/DMA requests to be generated, without having to update the Compare registers in software.

1.3.2 Digital Watchdog

The digital watchdog (DWD) generates resets to prevent runaway code (see Figure 1-2). A reset is generated after a programmable period, if no correct key sequence was written to the RTIWDKEY register. By default, the digital watchdog is disabled; however, it can be enabled by writing to the RTIDWDCTRL register, a 32-bit value which is the inverted value of the hardwired code in the module. Once the DWD is enabled, it cannot be disabled.

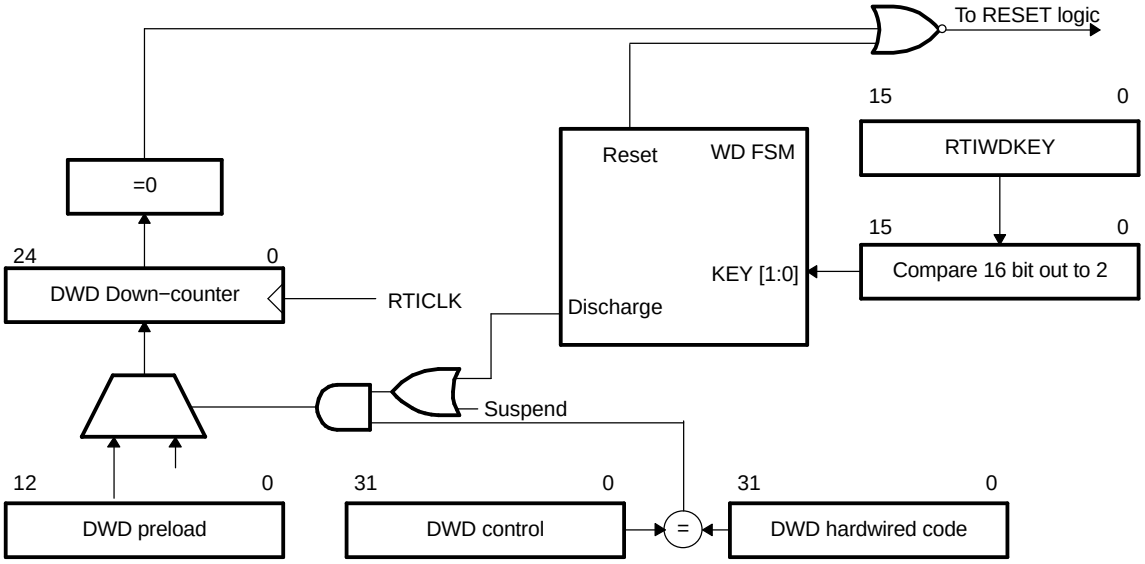
If the correct key sequence is written to the RTIWDKEY register (0xE51A followed by 0xA35C), the 25-bit DWD Down-Counter is reloaded with the 12-bit preload value stored in RTIDWDPRLD. If the incorrect values are written, a watchdog reset will occur immediately. A reset will also be generated, when the DWD Down-Counter is decremented (with RTICLK frequency) to 0. While the device is in debug mode (suspend), the DWD Down-Counter keeps the value it had when entering debug mode. The expiration time of the DWD Down-Counter can be determined with following equation:

Equation 1-1.

$$t_{exp} = (RTIDWDPRLD+1) \times 2^{13} / RTICLK \quad (1)$$

where: RTIDWDPRLD = 0...8191

Figure 1-2. Digital Watchdog



1.3.3 Suspend Mode Behavior

Once the system enters suspend mode, the behaviour of the RTI depends on the COS bit (RTIGCTRL.15). If the bit is cleared and suspend is active, all counters will stop operation. If the bit is set to one, all counters will be clocked normally and the RTI will work in normal mode.

Registers For RTI

This section includes the control and status registers for the Real-Time Interrupt module.

A.1 Control Registers

The RTI registers shown in Table A-1. The offset is relative to the peripheral base address (see the device's datasheet).

Table A-1. RTI Registers

Offset	Acronym	Register Description
00h	RTIGCTRL	Global Control Register. Starts / stops the counters.
04h	Reserved	Reserved bit.
08h	RTICAPCTRL	Capture Control. Controls the capture source for the counters.
0Ch	RTICOMPCTRL	Compare Control. Controls the source for the compare registers.
10h	RTIFRC0	Free-Running Counter 0. Current value of free running counter 0.
14h	RTIUC0	Up-Counter 0. Current value of prescale counter 0.
18h	RTICPUC0	Compare Up-Counter 0. Compare value compared with prescale counter 0.
20h	RTICAFRC0	Capture Free-Running Counter 0. Current value of free running counter 0 on external event.
24h	RTICAUC0	Capture Up-Counter 0. Current value of prescale counter 0 on external event.
30h	RTIFRC1	Free-Running Counter 1. Current value of free running counter 1.
34h	RTIUC1	Up-Counter 1. Current value of prescale counter 1.
38h	RTICPUC1	Compare Up-Counter 1. Compare value compared with prescale counter 1.
40h	RTICAFRC1	Capture Free-Running Counter 1. Current value of free running counter 1 on external event.
44h	RTICAUC1	Capture Up-Counter 1. Current value of prescale counter 1 on external event.
50h	RTICOMP0	Compare 0. Compare value to be compared with the counters.
54h	RTIUDCP0	Update Compare 0. Value to be added to the compare register 0 value on compare match.
58h	RTICOMP1	Compare 1. Compare value to be compared with the counters.
5Ch	RTIUDCP1	Update Compare 1. Value to be added to the compare register 1 value on compare match.
60h	RTICOMP2	Compare 2. Compare value to be compared with the counters.
64h	RTIUDCP2	Update Compare 2. Value to be added to the compare register 2 value on compare match.
68h	RTICOMP3	Compare 3. Compare value to be compared with the counters.
6Ch	RTIUDCP3	Update Compare 3. Value to be added to the compare register 3 value on compare match.
70h	Reserved	Reserved bit.
74h	Reserved	Reserved bit.

Table A-1. RTI Registers (continued)

Offset	Acronym	Register Description
80h	RTISETINT	Set Interrupt Enable. Sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.
84h	RTICLEARINT	Clear Interrupt Enable. Clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.
88h	RTIINTFLAG	Interrupt Flags. Interrupt pending bits.
90h	RTIDWDCTRL	Digital Watchdog Control. Enables the Digital Watchdog.
94h	RTIDWDPRLD	Digital Watchdog Preload. Sets the experation time of the Digital Watchdog.
98h	RTIWDSTATUS	Watchdog Status. Reflects the status of Analog and Digital Watchdog.
9Ch	RTIWDKEY	Watchdog Key. Correct written key values discharge the external capacitor.
A0h	RTIDWDCNTR	Digital Watchdog Down-Counter

A.1.1 RTI Global Control Register (RTIGCTRL)

The RTI Global Control register (RTIGCTRL) is shown in Figure A-1 and described in Table A-2.

Figure A-1. RTI Global Control Register (RTIGCTRL)

31			16
Reserved			
R-0			

15	14	8
COS	Reserved	
R/WP-0	R-0	

7	2	1	0
Reserved		CNT1EN	CNT0EN
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-2. RTI Global Control Register (RTIGCTRL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved		Reads return 0 and writes have no effect
15	COS		Continue On Suspend. This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting.
		0	Stop counters in debug mode
		1	Continue counting in debug mode
14-2	Reserved		Reads return 0 and writes have no effect
1	CNT1EN		Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1).
		0	Stop counters
		1	Start counters

Table A-2. RTI Global Control Register (RTIGCTRL) Field Descriptions (continued)

Bit	Field	Value	Description
0	CNT0EN		Counter 0 Enable. The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0).
		0	Stop counters
		1	Start counters

A.1.2 RTI Capture Control Register (RTICAPCTRL)

The RTI Capture Control register (RTICAPCTRL) is shown in Figure A-2 and described in Table A-3.

Figure A-2. RTI Capture Control Register (RTICAPCTRL)

31															16
Reserved															
R-0															
15															8
Reserved															
R-0															

7						2	1	0
Reserved							CAPCNTR1	CAPCNTR0
R-0							R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

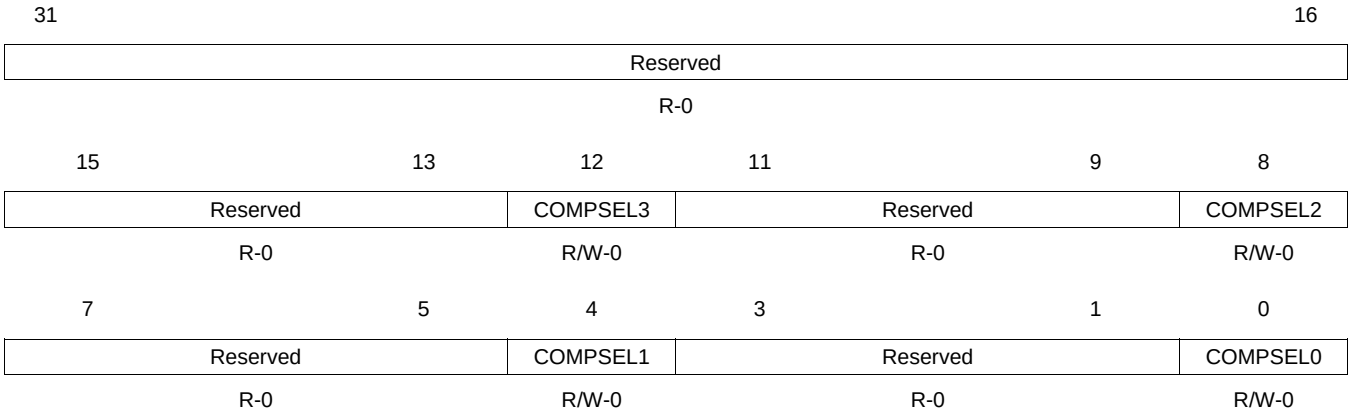
Table A-3. RTI Capture Control Register (RTICAPCTRL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved		Reads return 0 and writes have no effect.
1	CAPCNTR1		Capture Counter 1. This bit determines which external interrupt source triggers a capture event of both UC1 and FRC1.
		0	Enable capture event triggered by Capture Event Source 0
		1	Enable capture event triggered by Capture Event Source 1
0	CAPCNTR0		Capture Counter 0. This bit determines which external interrupt source triggers a capture event of both UC0 and FRC0.
		0	Enable capture event triggered by Capture Event Source 0
		1	Enable capture event triggered by Capture Event Source 1

A.1.3 RTI Compare Control Register (RTICOMPCTRL)

The RTI compare control register (RTICOMPCTRL) is shown in Figure A-3 and described in Table A-4.

Figure A-3. RTI Compare Control Register (RTICOMPCTRL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

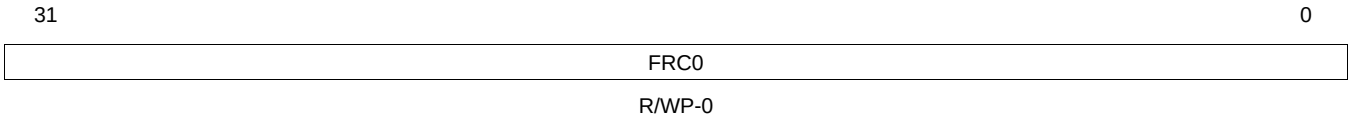
Table A-4. RTI Compare Control Register (RTICOMPCTRL) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved		Reads return 0 and writes have no effect
12	COMPSEL3		Compare Select 3. This bit determines the counter with which the compare value hold in compare register 3 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1
11-9	Reserved		Reads return 0 and writes have no effect
8	COMPSEL2		Compare Select 2. This bit determines the counter with which the compare value hold in compare register 2 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1
7-5	Reserved		Reads return 0 and writes have no effect
4	COMPSEL1		Compare Select 1. This bit determines the counter with which the compare value hold in compare register 1 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1
3-1	Reserved		Reads return 0 and writes have no effect
0	COMPSEL0		Compare Select 0. This bit determines the counter with which the compare value hold in compare register 0 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1

A.1.4 RTI Free Running Counter 0 Register (RTIFRC0)

The RTI Free-Running counter 0 register (RTIFRC0) is shown in Figure A-4 and described in Table A-5.

Figure A-4. RTI Free Running Counter 0 Register (RTIFRC0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

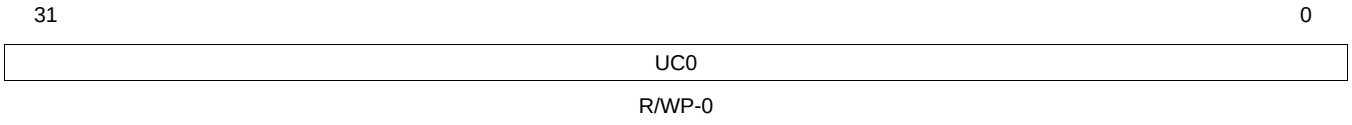
Table A-5. RTI Free Running Counter 0 Register (RTIFRC0) Field Descriptions

Bit	Field	Value	Description
31-0	FRC0	0-FFFF FFFFh	Free-Running Counter 0. This register holds the current value of the Free-Running Counter 0 and will be updated continuously. The counter can be preset by writing to this register. The counter then increments from this preset value upwards. If counters have to be preset, they first have to be disabled in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

A.1.5 RTI Up Counter 0 Register (RTIUC0)

The RTI Up-Counter 0 register (RTIUC0) is shown in Figure A-5 and described in Table A-6.

Figure A-5. RTI Up Counter 0 Register (RTIUC0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-6. RTI Up Counter 0 Register (RTIUC0) Field Descriptions

Bit	Field	Value	Description
31-0	UC0	0-FFFF FFFFh	Up-Counter 0. This register holds the current value of the Up-Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free-Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up-Counter 0 and Free-Running Counter 0. The counter can be preset by writing to this register. The counter then increments from this preset value upwards. If counters have to be preset, they first have to be disabled in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. If the preset value is bigger than the compare value stored in register RTICPUC0, then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

A.1.6 RTI Compare Up Counter 0 Register (RTICPUC0)

The RTI Compare Up-Counter 0 register (RTICPUC0) is shown in Figure A-6 and described in Table A-7.

Figure A-6. RTI Compare Up Counter 0 Register (RTICPUC0)

31	0
CPUC0	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-7. RTI Compare Up Counter 0 Register (RTICPUC0) Field Descriptions

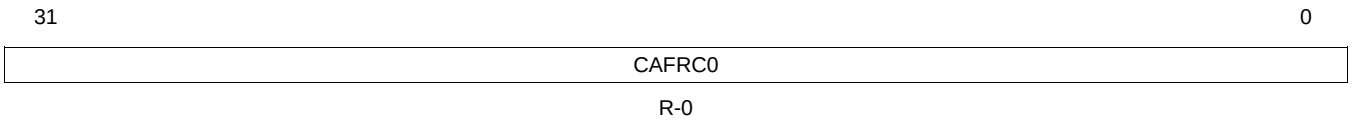
Bit	Field	Value	Description
31-0	CPUC0	0-FFFF FFFFh	Compare Up-Counter 0. This register holds the compare value, which is compared with the Up-Counter 0. When the compare matches, the Free-Running counter 0 is incremented and the Up-Counter is set to zero. The value set in this register prescales the RTI clock. See the equation below.

$$f_{FRC0} = \frac{RTCLK}{CPUC0 + 1}$$

A.1.7 RTI Capture Free Running Counter 0 Register (RTICAFRC0)

The RTI Capture-Free Running counter 0 register (RTICAFRC0) is shown in Figure A-7 and described in Table A-8.

Figure A-7. RTI Capture Free Running Counter 0 Register (RTICAFRC0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

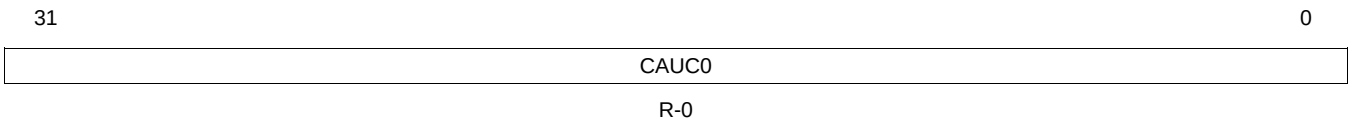
Table A-8. RTI Capture Free Running Counter 0 Register (RTICAFRC0) Field Descriptions

Bit	Field	Value	Description
31-0	CAFRC0	0-FFFF FFFFh	Capture Free-Running Counter 0. This register captures the current value of the Free-Running Counter 0 when an event occurs. The event which triggers this capture is configured in RTICAPCTRL.

A.1.8 RTI Capture Up Counter 0 Register (RTICAUC0)

The RTI Capture-Up Counter 0 register (RTICAUC0) is shown in Figure A-8 and described in Table A-9.

Figure A-8. RTI Capture Up Counter 0 Register (RTICAUC0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-9. RTI Capture Up Counter 0 Register (RTICAUC0) Field Descriptions

Bit	Field	Value	Description
31-0	CAUC0	0-FFFF FFFFh	Capture Up-Counter 0. This register captures the current value of the Up-Counter 0 when an event occurs; the event is configured in RTICAPCTRL. The read sequence has to be the same as with Up-Counter 0 and Free-Running Counter 0; so, the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register corresponds to the value of the RTICAFRC0 register, even if another capture event happens in-between the two reads.

A.1.9 RTI Free Running Counter 1 Register (RTIFRC1)

The RTI Free-Running Counter 1 register (RTIFRC1) is shown in Figure A-9 and described in Table A-10.

Figure A-9. RTI Free Running Counter 1 Register (RTIFRC1)

31	0
FRC1	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-10. RTI Free Running Counter 1 Register (RTIFRC1) Field Descriptions

Bit	Field	Value	Description
31-0	FRC1	0-FFFF FFFFh	Free-Running Counter 1. This register holds the current value of the Free-Running Counter 1 and will be updated continuously. This counter can be preset by writing to this register and then increments from this preset value upwards. If counters have to be preset, they have to be disabled first in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1.

A.1.10 RTI Up Counter 1 Register (RTIUC1)

The RTI Up-Counter 1 register (RTIUC1) is shown in Figure A-10 and described in Table A-11.

Figure A-10. RTI Up Counter 1 Register (RTIUC1)

31	0
UC1	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

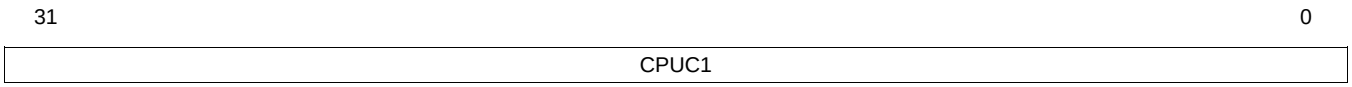
Table A-11. RTI Up Counter 1 Register (RTIUC1) Field Descriptions

Bit	Field	Value	Description
31-0	UC1	0-FFFF FFFFh	Up Counter 1. This register holds the current value of the Up-Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64-bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up-Counter 1 and Free-Running Counter 1. The counter can be preset by writing to this register. The counter increments then from this written value upwards. If counters have to be preset, they first have to be disabled in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. If the preset value is bigger than the compare value stored in register RTICPUC1, then it can take a long time until a compare matches, since UC1 has to count up until it overflows.

A.1.11 RTI Compare Up Counter 1 Register (RTICPUC1)

The RTI Compare Up-Counter 1 register (RTICPUC1) is shown in Figure A-11 and described in Table A-12.

Figure A-11. RTI Compare Up Counter 1 Register (RTICPUC1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

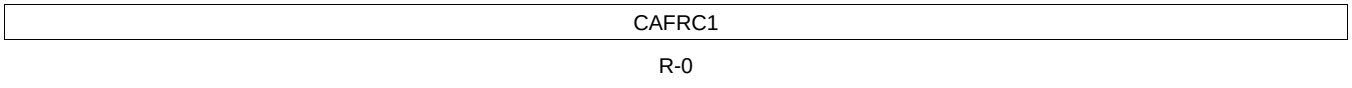
Table A-12. RTI Compare Up Counter 1 Register (RTICPUC1) Field Descriptions

Bit	Field	Value	Description
31-0	CPUC1	0-FFFF FFFFh	Compare Up-Counter 1. This register holds the compare value, which is compared with the Up-Counter 1. When the compare matches, Free-Running Counter 1 is incremented and the Up-Counter is set to zero. The value set in this register prescales the RTI clock.

A.1.12 RTI Capture Free Running Counter 1 Register (RTICAFRC1)

The RTI Capture Free-Funning counter 1 register (RTICAFRC1) is shown in Figure A-12 and described in Table A-13.

Figure A-12. RTI Capture Free Running Counter 1 Register (RTICAFRC1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

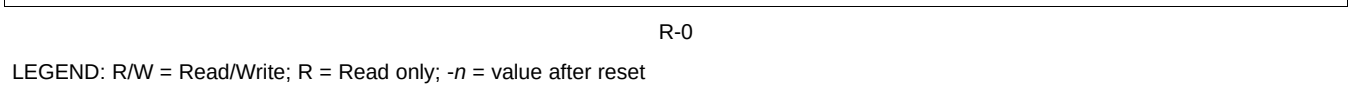
Table A-13. RTI Capture Free Running Counter 1 Register (RTICAFRC1) Field Descriptions

Bit	Field	Value	Description
31-0	CAFRC 1	0-FFFF FFFFh	Capture Free Running Counter 1. This register captures the current value of the Free-Running Counter 1 when an event occurs. The event which triggers this capture is configured in RTICAPCTRL.

A.1.13 RTI Capture Up Counter 1 Register (RTICAUC1)

The RTI Capture Up-Counter 1 register (RTICAUC1) is shown in Figure A-13 and described in Table A-14.

Figure A-13. RTI Capture Up Counter 1 Register (RTICAUC1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-14. RTI Capture Up Counter 1 Register (RTICAUC1) Field Descriptions

Bit	Field	Value	Description
31-0	CAUC1	0-FFFF FFFFh	Capture Up-Counter 1. This register captures the current value of the Up-Counter 1 when a event occurs. This event is configured in RTICAPCTRL. The read sequence has to be the same as with Up-Counter 1 and Free-Running Counter 1. So, the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC0 register corresponds to the value of the RTICAFRC0 register, even if another capture event happens in-between the two reads.

A.1.14 RTI Compare 0 Register (RTICOMP0)

The RTI Compare 0 register (RTICOMP0) is shown in Figure A-14 and described in Table A-15.

Figure A-14. RTI Compare 0 Register (RTICOMP0)

31	0
COMP0	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-15. RTI Compare 0 Register (RTICOMP0) Field Descriptions

Bit	Field	Value	Description
31-0	COMP0	0-FFFF FFFFh	Compare 0. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match since the compare logic will only be active when the associated counter block is enabled in RTIGCTRL.

A.1.15 RTI Update Compare 0 Register (RTIUDCP0)

The RTI Update Compare 0 register (RTIUDCP0) is shown in Figure A-15 and described in Table A-16.

Figure A-15. RTI Update Compare 0 Register (RTIUDCP0)

31	0
UDCP0	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-16. RTI Update Compare 0 Register (RTIUDCP0) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP0	0-FFFF FFFFh	Update Compare 0 Register. This register holds a value, which is added to the value in the Compare 0 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

A.1.16 RTI Compare 1 Register (RTICOMP1)

The RTI Compare 1 register (RTICOMP1) is shown in Figure A-16 and described in Table A-17.

Figure A-16. RTI Compare 1 Register (RTICOMP1)

31	0
COMP1	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-17. RTI Compare 1 Register (RTICOMP1) Field Descriptions

Bit	Field	Value	Description
31-0	COMP1	0-FFFF FFFFh	Compare 1. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled in RTIGCTRL.

A.1.17 RTI Update Compare 1 Register (RTIUDCP1)

The RTI Update Compare 1 register (RTIUDCP1) is shown in Figure A-17 and described in Table A-18.

Figure A-17. RTI Update Compare 1 Register (RTIUDCP1)

31	0
UDC1	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-18. RTI Update Compare 1 Register (RTIUDCP1) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP1	0-FFFF FFFFh	Update Compare 1 Register. This register holds a value, which is added to the value in the Compare 1 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

A.1.18 RTI Compare 2 Register (RTICOMP2)

The RTI Compare 2 register (RTICOMP2) is shown in Figure A-18 and described in Table A-19.

Figure A-18. RTI Compare 2 Register (RTICOMP2)

31	0
COMP2	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-19. RTI Compare 2 Register (RTICOMP2) Field Descriptions

Bit	Field	Value	Description
31-0	COMP2	0-FFFF FFFFh	Compare 2. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match, since the compare logic will only be active when the associated counter block is enabled in RTIGCTRL.

A.1.19 RTI Update Compare 2 Register (RTIUDCP2)

The RTI Update Compare 2 register (RTIUDCP2) is shown in Figure A-19 and described in Table A-20.

Figure A-19. RTI Update Compare 2 Register (RTIUDCP2)

31	0
UDCP2	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-20. RTI Update Compare 2 Register (RTIUDCP2) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP2	0-FFFF FFFFh	Update Compare 2 Register. This register holds a value, which is added to the value in the Compare 2 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

A.1.20 RTI Compare 3 Register (RTICOMP3)

The RTI Compare 3 register (RTICOMP3) is shown in Figure A-20 and described in Table A-21.

Figure A-20. RTI Compare 3 Register (RTICOMP3)

31	0
COMP3	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-21. RTI Compare 3 Register (RTICOMP3) Field Descriptions

Bit	Field	Value	Description
31-0	COMP3	0-FFFF FFFFh	Compare 3. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match, since the compare logic will only be active when the associated counter block is enabled in RTIGCTRL.

A.1.21 RTI Update Compare 3 Register (RTIUDCP3)

The RTI update compare 3 register (RTIUDCP3) is shown in Figure A-21 and described in Table A-22.

Figure A-21. RTI Update Compare 3 Register (RTIUDCP3)

31	0
UDCP3	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-22. RTI Update Compare 3 Register (RTIUDCP3) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP3	0-FFFF FFFFh	Update Compare 3 Register. This register holds a value, which is added to the value in the Compare 3 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

A.1.22 RTI Set/Status Interrupt Register (RTISETINT)

The RTI set/status interrupt register (RTISETINT) is shown in Figure A-22 and described in Table A-23.

Figure A-22. RTI Set/Status Interrupt Register (RTISETINT)

31	24
Reserved	
R-0	

23	19	18	17	16
Reserved		SETOVL1INT	SETOVL0INT	Reserved
R-0		R/WP-0	R/WP-0	R-0

15	12	11	10	9	8
Reserved		SETDMA3	SETDMA2	SETDMA1	SETDMA0
R-0		R/WP-0	R/WP-0	R/WP-0	R/WP-0

7	4	3	2	1	0
Reserved		SETINT3	SETINT2	SETINT1	SETINT0
R-0		R/WP-0	R/WP-0	R/WP-0	R/WP-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

This register prevents the necessity of a read-modify-write operation if a particular interrupt should be enabled.

Table A-23. RTI Set/Status Interrupt Register (RTISETINT) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved		Reads return 0 and writes have no effect
18	SETOVL1INT		Set Free Running Counter 1 Overflow Interrupt
		0	Interrupt is disabled
		1	Interrupt is enabled
17	SETOVL0INT		Set Free Running Counter 0 Overflow Interrupt
		0	Interrupt is disabled
		1	Interrupt is enabled
16-12	Reserved		Reads return 0 and only writes of 0 allowed
11	SETDMA3		Set Compare DMA Request 3
		0	DMA request is disabled
		1	DMA request is enabled
10	SETDMA2		Set Compare DMA Request 2
		0	DMA request is disabled
		1	DMA request is enabled
9	SETDMA1		Set Compare DMA Request 1
		0	DMA request is disabled
		1	DMA request is enabled
8	SETDMA0		Set Compare DMA Request 0
		0	DMA request is disabled
		1	DMA request is enabled
7-4	Reserved		Reads return 0 and writes have no effect
3	SETINT3		Set Compare Interrupt 3
		0	Interrupt is disabled
		1	Interrupt is enabled
2	SETINT2		Set Compare Interrupt 2
		0	Interrupt is disabled
		1	Interrupt is enabled
1	SETINT1		Set Compare Interrupt 1
		0	Interrupt is disabled
		1	Interrupt is enabled
0	SETINT0		Set Compare Interrupt 0
		0	Interrupt is disabled
		1	Interrupt is enabled

A.1.23 RTI Clear/Status Interrupt Register (RTICLEARINT)

The RTI Clear/Status Interrupt (RTICLEARINT) register is shown in Figure A-23 and described in Table A-24.

Figure A-23. RTI Clear/Status Interrupt Register (RTICLEARINT)

31	24
Reserved	
R-0	

23	19	18	17	16
Reserved		CLEAROVL1INT	CLEAROVL0INT	Reserved
R-0		R/WP-0	R/WP-0	R-0

15	12	11	10	9	8
Reserved		CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0
R-0		R/WP-0	R/WP-0	R/WP-0	R/WP-0

7	4	3	2	1	0
Reserved		CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
R-0		R/WP-0	R/WP-0	R/WP-0	R/WP-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

This register prevents the necessity of a read-modify-write operation if a particular interrupt should be disabled.

Table A-24. RTI Clear/Status Interrupt Register (RTICLEARINT) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved		Reads return 0 and writes have no effect
18	CLEAROVL1INT		Clear Free Running Counter 1 Overflow Interrupt
		0	Interrupt is disabled
		1	Interrupt is enabled
17	CLEAROVL0INT		Clear Free Running Counter 0 Overflow Interrupt.
		0	Interrupt is disabled
		1	Interrupt is enabled
16-12	Reserved		Reads return 0 and writes have no effect
11	CLEARDMA3		Clear Compare DMA Request 3
		0	DMA request is disabled
		1	DMA request is enabled
10	CLEARDMA2		Clear Compare DMA Request 2
		0	DMA request is disabled
		1	DMA request is enabled
9	CLEARDMA1		Clear Compare DMA Request 1.
		0	DMA request is disabled
		1	DMA request is enabled
8	CLEARDMA0		Clear Compare DMA Request 0.
		0	DMA request is disabled
		1	DMA request is enabled

Table A-24. RTI Clear/Status Interrupt Register (RTICLEARINT) Field Descriptions (continued)

Bit	Field	Value	Description
7-4	Reserved		Reads return 0 and writes have no effect
3	CLEARINT3		Clear Compare Interrupt 3
		0	Interrupt is disabled
		1	Interrupt is enabled
2	CLEARINT2		Clear Compare Interrupt 2
		0	iIterrupt is disabled
		1	Interrupt is enabled
1	CLEARINT1		Clear Compare Interrupt 1
		0	Interrupt is disabled
		1	Interrupt is enabled
0	CLEARINT0		Clear Compare Interrupt 0
		0	Interrupt is disabled
		1	Interrupt is enabled

A.1.24 RTI Interrupt Flag Register (RTIINTFLAG)

The RTI interrupt flag register (RTIINTFLAG) is shown in Figure A-24 and described in Table A-25.

Figure A-24. RTI Interrupt Flag Register (RTIINTFLAG)

31	24
Reserved	
R-0	

23	19	18	17	16
Reserved		OVL1INT	OVL0INT	Reserved
R-0		RCP-0	RCP-0	R-0

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved		INT3	INT2	INT1	INT0
R-0		RCP-0	RCP-0	RCP-0	RCP-0

LEGEND: R = Read; C = Clear; -*n* = value after reset

The corresponding flags are set at every compare match of Free-Running Counterx and RTICOMPx value, regardless if the interrupt is enabled or not.

Table A-25. RTI Interrupt Flag Register (RTIINTFLAG) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved		Reads return 0 and writes have no effect
18	OVL1INT		Free Running Counter 1 Overflow Interrupt Flag
		0	No interrupt pending
		1	Interrupt pending

Table A-25. RTI Interrupt Flag Register (RTIINTFLAG) Field Descriptions (continued)

Bit	Field	Value	Description
17	OVL0INT		Free Running Counter 0 Overflow Interrupt Flag
		0	No interrupt pending
		1	Interrupt pending
16-4	Reserved		Reads return 0 and writes have no effect
3	INT3		Interrupt Flag 3. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending
2	INT2		Interrupt Flag 2. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending
1	INT1		Interrupt Flag 1. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending
0	INT0		Interrupt Flag 0. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending

A.1.25 Digital Watchdog Control Register (RTIDWDCTRL)

The digital watchdog control register (RTIDWDCTRL) is shown in Figure A-25 and described in Table A-26.

Figure A-25. Digital Watchdog Control Register (RTIDWDCTRL)

31	0
DWDCTRL	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-26. Digital Watchdog Control Register (RTIDWDCTRL) Field Descriptions

Bit	Field	Value	Description
31-0	DWDCTRL	0-FFFF FFFFh	Digital Watchdog Control 0x5312ACED = DWD counter is disabled Any other value = DWD counter is enabled By default, the digital watchdog counter is disabled. Any write other than 0x5312ACED to the DWDCTRL register enables the counter. This initial write can occur at any time during code execution. Once the initial write has occured, all other writes are ignored. TI recommends that the value 0xACED5312 be written to activate the counter. RTIDWDCTRL is a write-once register that allows the opportunity to enable or disable the DWD functionality. The register will only be writable again after a reset.

A.1.26 Digital Watchdog Preload Register (RTIDWDPRLD)

The digital watchdog preload register (RTIDWDPRLD) is shown in Figure A-26 and described in Table A-27.

Figure A-26. Digital Watchdog Preload Register (RTIDWDPRLD)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		DWDPRLD	
R-0		R/W-1FFFh	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-27. Digital Watchdog Preload Register (RTIDWDPRLD) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved		Reserved
11-0	DWDPRLD		Digital Watchdog Preload Value The preload value must be written prior to enabling the DWD Down Counter in RTIDWDCTRL. The expiration time of the counter can be calculated with the formula given in Equation 1-1.

A.1.27 Watchdog Status Register (RTIWDSTATUS)

The watchdog status register (RTIWDSTATUS) is shown in Figure A-27 and described in Table A-28.

Figure A-27. Watchdog Status Register (RTIWDSTATUS)

31	16
Reserved	
R-0	

15	3	2	1	0
Reserved		KEYST	DWDST	Reserved
R-0		RCP-x	RCP-x	R-0

LEGEND: R = Read; C = Clear; -*n* = value after reset

The values of the following status bits will not be affected by a reset. Only the user can clear these bits. These bits are only intended for debug purposes.

Table A-28. Watchdog Status Register (RTIWDSTATUS) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved		Reserved
2	KEYST		Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or key sequence written to the RTIWDKEY register.
		0	No reset generated
		1	Reset generated

Table A-28. Watchdog Status Register (RTIWDSTATUS) Field Descriptions (continued)

Bit	Field		Value	Description
1	DWDST			Digital Watchdog Status.
		Write	0	Leaves the current value unchanged
			1	Sets the bit to 0
		Read	0	No reset generated
			1	Reset generated
0	Reserved			Reserved

A.1.28 Watchdog Key Register (RTIWDKEY)

The watchdog key register (RTIWDKEY) is shown in Figure A-28 and described in Table A-29.

Figure A-28. Watchdog Key Register (RTIWDKEY)

31	16
Reserved	
R-0	
15	0
WDKEY	
R/W-0xA35C	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-29. Watchdog Key Register (RTIWDKEY) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved		Reads return 0 and writes have no effect
15-0	WDKEY		Bit 7:0 : Watchdog Key. Key Sequence location. Reads are indeterminate. A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and reloads the counter RTIDWDCNTL with the preload value RTIDWDPRLD. Writing any other value causes a digital watchdog reset, as shown in Table A-30

Table A-30. Example of a WDKEY Sequence

Step	Value Written to WDKEY	Result
1	0x0A35C	No Action
2	0x0A35C	No Action
3	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
4	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
5	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
6	0x0A35C	Watchdog is reset
7	0x0A35C	No Action
8	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
9	0x0A35C	Watchdog is reset
10	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
11	0x02345	System reset; incorrect value written to WDKEY

A.1.29 WDKEY Digital Watchdog Down Counter (RTIDWDCNTR)

The WDKEY Digital Watchdog Down Counter (RTIDWDCNTR) is shown in Figure A-29 and described in Table A-31.

Figure A-29. WDKEY Digital Watchdog Down Counter (RTIDWDCNTR)

31	25	24	0
Reserved		DWDCNTR	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table A-31. WDKEY Digital Watchdog Down Counter (RTIDWDCNTR) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved		Reads return 0 and writes have no effect
24-0	DWDCNTR		Digital Watchdog Down Counter
		0	Reads return the current counter value
		1	Writes have no effect

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