TMS320VC5503/5507/5509 DSP Real-Time Clock (RTC) Reference Guide

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Preface

Read This First

About This Manual

This manual describes the features and operation of the real-time clock (RTC) that is on the TMS320VC5503, TMS320VC5507, TMS320VC5509, and TMS320VC5509A digital signal processors (DSPs) in the TMS320C55x™ (C55x™) DSP generation.

Notational Conventions

This document uses the following conventions:

- In most cases, hexadecimal numbers are shown with the suffix h. For example, the following number is a hexadecimal 40 (decimal 64):

  40h

  Similarly, binary numbers often are shown with the suffix b. For example, the following number is the decimal number 4 shown in binary form:

  0100b

- If a signal or pin is active low, it has an overbar. For example, the $\overline{\text{RESET}}$ signal is active low.

- Bits and signals are sometimes referenced with the following notations:

Notation	Description	Example
Register(n–m)	Bits n through m of Register	R(3–0) represents bits 3 through 0 of register R.
Bus[n:m]	Signals n through m of Bus	A[21:1] represents signals 21 through 1 of bus A.

- The following terms are used to name portions of data:

Term	Description	Example
LSB	Least significant bit	In R(7–0), bit 0 is the LSB.
MSB	Most significant bit	In R(7–0), bit 7 is the MSB.

Related Documentation From Texas Instruments

The following documents describe the C55x devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

TMS320VC5503 Fixed-Point Digital Signal Processor Data Manual (literature number SPRS245) describes the features of the TMS320VC5503 fixed-point DSP and provides signal descriptions, pinouts, electrical specifications, and timings for the device.

TMS320VC5507 Fixed-Point Digital Signal Processor Data Manual (literature number SPRS244) describes the features of the TMS320VC5507 fixed-point DSP and provides signal descriptions, pinouts, electrical specifications, and timings for the device.

TMS320VC5509 Fixed-Point Digital Signal Processor Data Manual (literature number SPRS163) describes the features of the TMS320VC5509 fixed-point DSP and provides signal descriptions, pinouts, electrical specifications, and timings for the device.

TMS320VC5509A Fixed-Point Digital Signal Processor Data Manual (literature number SPRS205) describes the features of the TMS320VC5509A fixed-point DSP and provides signal descriptions, pinouts, electrical specifications, and timings for the device.

TMS320C55x Technical Overview (literature number SPRU393) introduces the TMS320C55x DSPs, the latest generation of fixed-point DSPs in the TMS320C5000™ DSP platform. Like the previous generations, this processor is optimized for high performance and low-power operation. This book describes the CPU architecture, low-power enhancements, and embedded emulation features.

TMS320C55x DSP CPU Reference Guide (literature number SPRU371) describes the architecture, registers, and operation of the CPU for the TMS320C55x DSPs.

TMS320C55x DSP Peripherals Overview Reference Guide (literature number SPRU317) introduces the peripherals, interfaces, and related hardware that are available on TMS320C55x DSPs.

TMS320C55x DSP Algebraic Instruction Set Reference Guide (literature number SPRU375) describes the TMS320C55x DSP algebraic instructions individually. Also includes a summary of the instruction set, a list of the instruction opcodes, and a cross-reference to the mnemonic instruction set.

TMS320C55x DSP Mnemonic Instruction Set Reference Guide (literature number SPRU374) describes the TMS320C55x DSP mnemonic instructions individually. Also includes a summary of the instruction set, a list of the instruction opcodes, and a cross-reference to the algebraic instruction set.

TMS320C55x Optimizing C/C++ Compiler User's Guide (literature number SPRU281) describes the TMS320C55x C/C++ Compiler. This C/C++ compiler accepts ISO standard C and C++ source code and produces assembly language source code for TMS320C55x devices.

TMS320C55x Assembly Language Tools User's Guide (literature number SPRU280) describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for TMS320C55x devices.

TMS320C55x DSP Programmer's Guide (literature number SPRU376) describes ways to optimize C and assembly code for the TMS320C55x DSPs and explains how to write code that uses special features and instructions of the DSPs.

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Real-Time Clock (RTC)

This document describes the real-time clock (RTC) available on the TMS320VC5503, TMS320VC5507, TMS320VC5509 and TMS320VC5509A DSPs. The RTC provides a time reference and the capability to generate time-based alarms to interrupt the DSP.

1 Introduction to the Real-Time Clock (RTC)

The real-time clock (RTC) provides the following features:

- 100-year calendar up to year 2099
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 12-hour clock mode (with AM and PM) or 24-hour clock mode
- Second, minute, hour, day, or week alarm interrupt
- Update cycle interrupt
- Periodic interrupt
- Single interrupt to the DSP CPU
- Supports external 32.768-kHz crystal or external clock source of the same frequency
- Separate isolated power supply

The RTC provides a time reference to an application running on the DSP. The current date and time is tracked in a set of counter registers that update once per second. The time can be represented in 12-hour or 24-hour mode. The calendar and time registers are buffered during reads and writes so that updates do not interfere with the accuracy of the time and date. For information on how to set the time and date, see section 2.3 on page 15.

Alarms are available to interrupt the DSP CPU at a particular time, or at periodic time intervals, such as once per minute or once per day. In addition, the RTC can interrupt the CPU every time the calendar and time registers are updated, or at programmable periodic intervals. For information on how to set and use alarms, see section 3 on page 18.

The clock reference for the RTC is an external 32.768-kHz crystal (connected between signals RTCINX1 and RTCINX2) or an external clock source of the same frequency. The RTC also has a separate power supply that is isolated from the rest of the DSP. When the DSP is without power, the RTC can remain powered to preserve the current time and calendar information.

Figure 1 shows a block diagram of the RTC. Table 1 lists and describes the signals.

Figure 1. Real-Time Clock Block Diagram

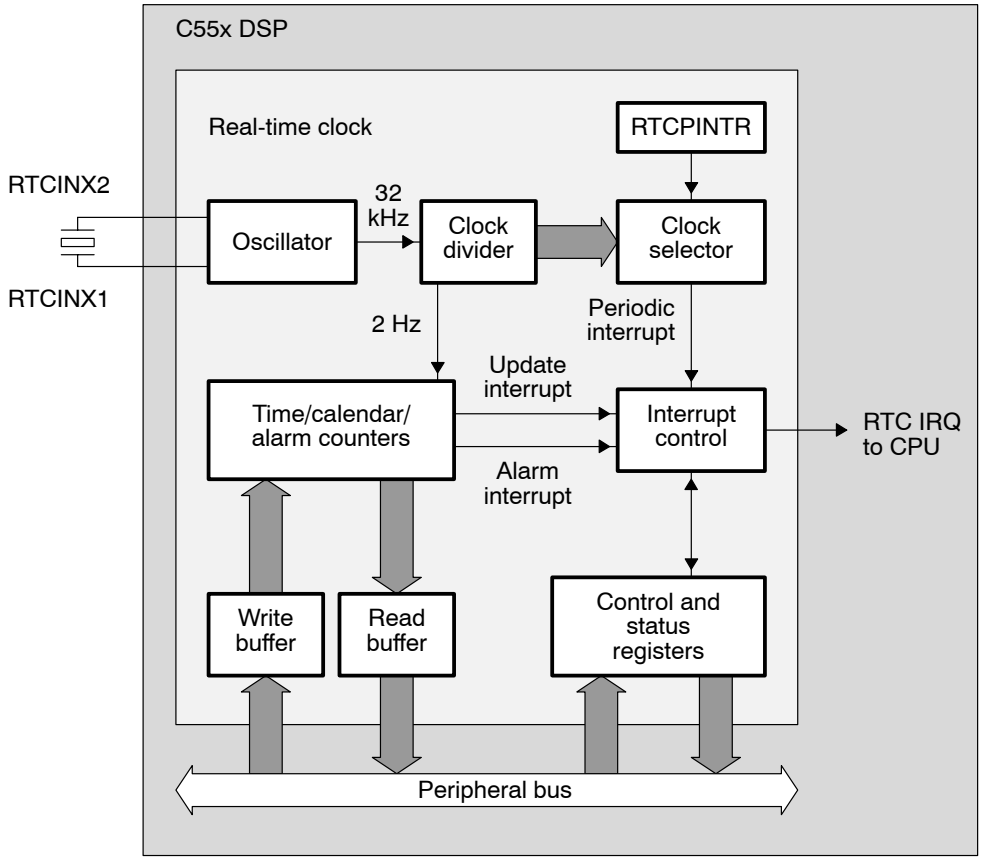


Table 1. Real-Time Clock Signal Descriptions

Name	I/O	Signal Descriptions
RTCINX1	Input	RTC time base input signal RTCINX1 can either be driven with a 32.768-kHz reference clock, or RTCINX1 and RTCINX2 and be connected to an external crystal. This signal is the input to the RTC internal oscillator used by the crystal.
RTCINX2	Output	RTC time base output signal RTCINX2 is the output from the RTC internal oscillator used by the crystal. If a crystal is not used as the time base for RTCINX1, RTCINX2 should be left unconnected.

1.1 Real-Time Clock Power Supply

The RTC has a power supply that is isolated from the rest of the DSP. This allows the RTC to continue to run while the rest of the DSP is not powered. In this state, the RTC time and calendar counters continue to run, but the RTC is unable to cause interrupts to the DSP since the DSP is not powered. The configuration of the alarm registers is also maintained as long as the RTC is powered. Separate power supply pins for the RTC are provided on the device package. For specific information about the RTC power supply connections, see the data manual for the DSP being used.

1.2 Real-Time Clock Reference Clock Source

The RTC uses an external 32.768-kHz reference clock as its basis for keeping time.

The source for the RTC reference clock may be provided by a crystal or by an external clock source. The RTC has an internal oscillator to support operation with a crystal. The crystal is connected between pins RTCINX1 and RTCINX2. RTCINX1 is the input to the on-chip oscillator and RTCINX2 is the output from the oscillator back to the crystal. For more information about the RTC crystal connection, see the data manual for the DSP being used.

An external 32.768-kHz clock source may be used instead of a crystal. In this case, the clock source is connected to RTCINX1, and RTCINX2 is left unconnected.

2 Using the Real-Time Clock Time and Calendar Registers

The current time and date are maintained in the RTC time and calendar registers. Information about how to use these registers is in the sections that follow.

2.1 Time/Calendar Data Format

The time and calendar data in the RTC is stored as binary-coded decimal (BCD) format. In BCD format, the decimal numbers 0 through 9 are encoded with their binary equivalent. Although most of the time/calendar registers have 4 bits assigned to each BCD digit, some of the register fields are shorter since the range of valid numbers may be limited. For example, only 3 bits are required to represent the day since only BCD numbers 1 though 7 are required.

The summary of the time/calendar registers is shown in Table 2. The alarm registers are interleaved with the time/calendar registers and are not shown in this table. The alarm registers are shown in Table 3. A complete description all RTC registers is available in section 7 (page 27).

Table 2. Time/Calendar Registers

Address (Hex)	Name	Function	Decimal Range	BCD Format
1800h	RTCSEC	Seconds	0–59	00–59
1802h	RTCMIN	Minutes	0–59	00–59
1804h	RTCHOUR	12-hour mode	1–12	01–12 (AM), 81–92 (PM)
		24-hour mode	0–23	00–23
1806h	RTCDAYW	Day of the week (Sunday = 1)	1–7	1–7
1807h	RTCDAYM	Day of the month (Date)	1–31	01–31
1808h	RTCMONTH	Month (January = 01)	1–12	01–12
1809h	RTCYEAR	Year	0–99	00–99

The RTC Seconds Register (RTCSEC) stores the seconds value of the current time. The minutes register (RTCMIN) stores the minutes value of the current time. The seconds and minutes are encoded BCD values 00 (0000b 0000b) through 59 (0101b 1001b).

The RTC Hours Register (RTCHOUR) stores the hours value of the current time. The hours are encoded BCD values 01 (0000b 0001b) through 12 (0001b 0010b) in 12-hour mode, or 00 (0000b 0000b) through 23 (0010b 0011b) in 24-hour mode. Selection of 12-hour or 24-hour mode is described in section 2.2.

The RTC Day of the Week and Day Alarm Register (RTCDAYW) stores the day of the week value of the current date. The DAY field of RTCDAYW is 3 bits and encodes the day of the week as BCD values 1 (001b) through 7 (111b). The days of the week are represented as Sunday (1) though Saturday (7).

The RTC Day of the Month Register (RTCDAYM) stores the day of the month for the current date. The day of the month is encoded as BCD values 01 (0000b 0001b) through 31 (0011b 0001b).

The RTC Month Register (RTCMONTH) stores the month for the current date. The month is encoded as BCD values 01 (0000b 0001b) through 12 (0001b 0010b).

The RTC Year Register (RTCYEAR) stores the year for the current date. The year is encoded as BCD values 00 (0000b 0000b) through 99 (1001b 1001b).

2.2 12-Hour and 24-Hour Modes

The current time can be represented in 12-hour or 24-hour mode by configuring the TM bit in the RTC Interrupt Enable Register (RTCINTEN). When
TM = 0, 12-hour mode is selected. In 12-hour mode, the hours are represented as 1 though 12 and the AMPM bit in RTCHOUR indicates AM or PM. When AMPM = 0, the current time is AM. When AMPM = 1, the current time is PM.

When TM = 1, 24-hour mode is selected and the hours are represented as 0 through 23. In this mode, the AMPM bit has no function and should be cleared.

2.3 Reading and Writing the Time/Calendar Registers

The time/calendar registers are updated every second as the time changes. To protect the accuracy of the time/date contained in these registers, the RTC provides a read buffer and a write buffer for access to the time/calendar register. During a read of the time/calendar registers, the RTC copies the current time/date form the time/calendar registers into the read buffer and the read buffer is isolated form the time/calendar registers. This isolation assures that the CPU reads the time/date present at the time of the read request rather than after the automatic updating. During writes, the desired value of the time/date is written to the write buffer and, when complete, is copied to the time/calendar registers. While the CPU is writing to the write buffer, it is isolated from the time/calendar registers, preserving the accuracy of the current time/date.

The SET bit in RTCINTEN controls the isolation of the read and write buffers from the time/calendar registers. When SET = 0, the read and write buffers are directly connected to the time/calendar registers. In this state, the current time/date can be read directly but there is no protection of the read data during an update cycle. In other words, if the RTC updates the current time/date while the CPU is reading the time/calendar registers, an inaccurate time/date could be read. When SET = 1, the time/calendar registers are copied to the read buffer and then the read buffer is isolated form the time/calendar registers. So even if the RTC updates the current time/date, the read value is preserved in the read buffers. Procedures for reading and writing the time/calendar registers are described in the sections that follow.

2.3.1 How to Set the Time/Calendar

To write a new value to the time/calendar registers, use the following procedure:

- ❏ Set the SET bit in RTCINTEN to isolate the write buffer from the time/calendar registers.
- ❏ Write the desired time and date to the time/calendar registers (RTCSEC, RTCMIN, RTCHOUR, RTCDAYW, RTCDAYM, RTCMONTH and RTCYEAR). Since SET = 1, these values actually go to the write buffer.
- ❏ Clear the SET bit to copy the write buffer values to the time/calendar registers.

2.3.2 How to Read the Time/Calendar Using the SET Bit

To read the current time/date using the SET bit, use the following procedure:

- ❏ Set the SET bit in RTCINTEN to copy the current time/date into the read buffer and isolate the read buffer from the time/calendar registers.
- ❏ Read the current time and date from the time/calendar registers (RTCSEC, RTCMIN, RTCHOUR, RTCDAYW, RTCDAYM, RTCMONTH and RTCYEAR). Since SET = 1, these values are actually being read from the read buffer.
- ❏ Clear the SET bit reconnect the read buffer to the time/calendar registers.

This method will provide the time/date that was current when the SET bit was set and prevents reading an incorrect time due to an RTC update.

2.3.3 How to Read the Time/Calendar Without Using the SET Bit

To read the current time/date without using the SET bit, use the following procedure:

- ❏ Leave the SET bit cleared.
- ❏ Read the RTCSEC for the seconds value of the current time/date.
- ❏ Read the remaining time/calendar register values (RTCMIN, RTCHOUR, RTCDAYW, RTCDAYM, RTCMONTH and RTCYEAR) of the current time/date.
- ❏ Read RTCSEC again and compare to the previous value. If both values are the same, an RTC update did not occur while the other registers were being read and the all of the values read represent the current time. If the seconds have changed, this indicates an RTC update occurred while the registers were being read and the process should be repeated.

This method provides the time/date that was current when the registers were read.

3 Using the Real-Time Clock Time and Calendar Alarms

Alarms can be configured to interrupt the CPU at any of the following intervals:

- On a specific seconds value, or every second
- On a specific minutes value, or every minute
- On a specific hours value, or every hour
- On a specific day of the week value, or every day

The time/calendar alarm registers control the setting of alarms. Information about how to use these registers is in the sections that follow. The alarms can also be configured to generate an interrupt to the CPU. The operation of the alarm interrupt is described in section 4.3 (page 24).

3.1 Time/Calendar Alarm Data Format

The time and calendar alarm data in the RTC is stored as binary-coded decimal (BCD) format. In BCD format, the decimal numbers 0 through 9 are encoded with their binary equivalent. Although most of the time/calendar alarm registers have 4 bits assigned to each BCD digit, some of the register field lengths may differ to accommodate the desired function.

The summary of the time/calendar alarm registers is shown in Table 3. The time/calendar registers are interleaved with the alarm registers and are not shown in this table. The time/calendar registers are shown in Table 2. A complete description of all RTC registers is available in section 7 (page 27).

Table 3. Time/Calendar Alarm Registers

Address (Hex)	Name	Function	Decimal Range	BCD Format
1801h	RTCSECA	Seconds alarm	0–59	00–59
			don't care	C0–FF
1803h	RTCMINA	Minutes alarm	0–59	00–59
			don't care	C0–FF
1805h	RTCHOURA	12-hour mode alarm	1–12	01–12 (AM), 81–92 (PM)
			don't care	C0–FF
		24-hour mode alarm	0–23	00–23
			don't care	C0–FF
1806h	RTCDAYW	Day of the week alarm (Sunday = 1)	1–7	1–7
			don't care	8–F

3.2 Day Alarm

The RTC Day of the Week and Day Alarm Register (RTCDAYW) stores the day of the week value of the desired alarm. The DAR field of RTCDAYW is 4 bits. Bits 6-4 encode the desired day for the alarm as BCD values 1 (001b) through 7 (111b). The days of the week are represented as Sunday (1) though Saturday (7).

Bit 7 represents a “don’t care” condition and causes an alarm to occur every day. Therefore, while DAR values 0h through 7h cause an alarm to occur on the specified day of the week, DAR values 8h through Fh cause an alarm to occur every day.

3.3 Hours Alarm

The RTC Hours Alarm Register (RTCHOURA) stores the hour value of the desired alarm. The hours are encoded BCD values 01 (0000b 0001b) through 12 (0001b 0010b) in 12-hour mode, or 00 (0000b 0000b) through 23 (0010b 0011b) in 24-hour mode. Selection of 12-hour or 24-hour mode is described in section 2.2 (page 15).

In 12-hour mode (TM = 0 in RTCINTEN), the HAR field contains the hour of the desired alarm time and the AMPM bit indicates whether the alarm should occur in the morning or evening. When AMPM = 0, the value in the HAR field represents AM. When AMPM = 1, the value in the HAR field represents PM.

In 24-hour mode (TM = 1 in RTCINTEN), the HAR field contains the hour of the desired alarm time and the AMPM bit should be cleared.

An alarm can be generated every hour by setting bits 7 and 6 in RTCHOURA. In this case, the remaining bits in the register do not affect the alarm.

3.4 Minutes Alarm

The RTC Minutes Alarm Register (RTCMINA) stores the minute value of the desired alarm. The minutes are encoded BCD values 00 (0000b 0000b) through 59 (0101b 1001b).

An alarm can be generated every minute by setting bits 7 and 6 in RTCMINA. In this case, the remaining bits in the register to not affect the alarm.

3.5 Seconds Alarm

The RTC Seconds Alarm Register (RTCSECA) stores the seconds value of the desired alarm. The seconds are encoded BCD values 00 (0000b 0000b) through 59 (0101b 1001b).

The seconds alarm register cannot be used to generate an alarm every second, but the update-ended interrupt can. The update-ended interrupt is described in section 4.4 (page 24).

3.6 Reading and Writing the Time/Calendar Alarm Registers

To write a new value to the time/calendar alarm registers, use the following procedure:

- ❑ Set the SET bit in RTCINTEN to isolate the write buffer from the time/calendar alarm registers.
- ❑ Write the desired alarm values to the time/calendar alarm registers (RTCSECA, RTCMINA, RTCHOURA, and RTCDAYW). Since SET = 1, these values actually go to the write buffer.
- ❑ Clear the SET bit to copy the write buffer values to the time/calendar alarm registers.

The time/calendar alarm registers can be read directly without using the SET bit since they do not change when the RTC updates the current time/date.

3.7 Examples of Time/Calendar Alarms Settings

Some examples of various alarm settings are shown in Table 4. Entries marked "–" indicate that the "don't care" value for that particular register should be used. A complete description of the RTC registers and their functions is provided in section 7 (page 27).

Table 4. Real-Time Clock Alarm Example Settings

Alarm occurs...	TM	DAR in RTCDAYW	HAR in RTCHOURA	AMPM in RTCHOURA	MAR in RTCMINA	SAR in RTCSECA
Every Monday at 3:19:46 AM (12-hour mode)	0	2 (Monday)	3	0	19	46
Every Monday at 3:19:46 PM (12-hour mode)	0	2 (Monday)	3	1	19	46
Every Monday at 3:19:46 PM (24-hour mode)	1	2 (Monday)	15	0	19	46
Every day at 3:19:46 PM	0	–	3	1	19	46
Every hour on Mondays at xx:19:46	–	2 (Monday)	–	–	19	46
Every minute on Mondays at 3:xx:46 PM (24-hour mode)	1	2 (Monday)	15	0	–	46
Every minute at xx:xx:46	1	–	–	0	–	46

4 Real-Time Clock Interrupt Requests

The RTC provides the ability to interrupt the CPU based on three events: a periodic interrupt, an alarm interrupt, or an update-ended interrupt. Although three interrupt sources are available, the RTC makes a single interrupt request to the CPU. Specific information about using each of the interrupt types is in the sections that follow.

4.1 Interrupt Enable and Flag Bits

Three bits (PIE, AIE, and UIE) in the interrupt enable register (RTCINTEN) enable the interrupts. PIE enables the periodic interrupt, AIE enables the alarm interrupt, and UIE enables the update-ended interrupt. Writing a logic 1 to an interrupt enable bit allows that interrupt to generate an RTC interrupt request to the CPU when the event occurs. If an RTC interrupt flag is already set when an interrupt is enabled, the RTC interrupt to the CPU occurs immediately, although the interrupt initiating the event may have occurred much earlier. Pending interrupts should be cleared before first enabling new interrupts.

When an interrupt event occurs, the corresponding flag bit (PF, AF, or UF) is set in the interrupt flag register (RTCINTFL). PF is associated with the periodic interrupt, AF is associated with the alarm interrupt, and UF is associated with the update-ended interrupt. These flag bits are set independent of the state of the corresponding enable bit in RTCINTEN. The flag bit can be used in a polling mode without enabling the corresponding enable bits.

If one of the three flag bits becomes active and the corresponding enable bit is set, an RTC interrupt to the CPU occurs. The RTC interrupt is asserted as long as at least one of the three interrupt flag bits and enable bits are set. The IRQF bit in RTCINTFL is set to 1 when the RTC interrupt to the CPU is asserted. The IRQF bit indicates that one or more interrupts have been initiated by the RTC. When an interrupt occurs from the RTC, the source of the interrupt can be determined by reading the flag bits in RTCINTFL.

Note:

On the TMS320VC5503/5507/5509 and TMS320VC5509A DSPs, the RTC interrupt is shared with external interrupt 4 (INT4) in interrupt flag register 1 (bit 3 in IFR1). The presence of an interrupt flag in this bit indicates that either INT4 or the RTC interrupt has occurred. The source of an RTC interrupt can be identified by reading RTCINTFL. If no RTC interrupt flags are present, the interrupt source was INT4.

This interrupt should not be used for both INT4 and RTC at the same time because some interrupt events may be missed if both interrupt sources occur near the same time. In this case, when the interrupt service is entered, the CPU clears the interrupt flag in the CPU. After the return from the interrupt service routine, the second interrupt source is not serviced since the interrupt flag in the CPU was cleared.

4.2 Periodic Interrupt Request

The periodic interrupt causes the RTC to make an interrupt request to the CPU periodically from once every minute to once every 122 μs. The periodic interrupt rate is selected using the RATE bits in the periodic interrupt selection register (RTCPINTR); see Table 5. Changing bits 3-0 of the RATE bits affects the periodic interrupt rate. When bit 4 of the RATE bits is set to 1, the periodic interrupt is asserted every minute regardless of the other RATE bit values. The minute interrupt is triggered when the seconds register is changed from 59 to 00. The periodic interrupts are enabled by the PIE bit in RTCINTEN.

Table 5. RTC Periodic Interrupt Rates Based on RATE Bits

RTCPINTR Bits RATE(4–0)	Periodic Interrupt Rate
00000	No interrupt
00001	Reserved
00010	Reserved
00011	122.070 μs (8192 per second)
00100	244.141 μs (4096 per second)
00101	488.281 μs (2048 per second)
00110	976.5625 μs (1024 per second)
00111	1.953125 ms (512 per second)
01000	3.90625 ms (256 per second)
01001	7.8125 ms (128 per second)
01010	15.625 ms (64 per second)
01011	31.25 ms (32 per second)
01100	62.5 ms (16 per second)
01101	125 ms (8 per second)
01110	250 ms (4 per second)
01111	500 ms (2 per second)
1xxxx	1 minute

To use the RTC periodic interrupt:

- ❑ Select the desired interrupt rate using by configuring the RATE bits in RTCPINTR.
- ❑ Enable the RTC periodic interrupt by setting the PIE bit in RTCINTEN.
- ❑ Enable the RTC interrupt in the CPU interrupt enable register 1 (IER1).

When the periodic interrupt occurs, the PF and IRQF flags in RTCINTFL are set and the RTC interrupt is sent to the CPU.

4.3 Alarm Interrupt Request

The RTC alarm interrupt can be used to generate an interrupt to the CPU at specific times. The alarm interrupt occurs when the alarm time programmed in the RTC alarm registers (RTCSECA, RTCMINA, RTCHOURA, and RTCDAYW) match the current time. For information about programming an alarm time, see section 3 on page 18.

To use the RTC alarm interrupt:

- ❏ Select the desired alarm time by configuring the RTC alarm registers.
- ❏ Enable the RTC alarm interrupt by setting the AIE bit in RTCINTEN.
- ❏ Enable the RTC interrupt in the CPU interrupt enable register 1 (IER1).

When the alarm interrupt occurs, the AF and IRQF flags in RTCINTFL are set and the RTC interrupt is sent to the CPU.

4.4 Update-Ended Interrupt Request

The RTC update-ended interrupt can be used to generate an interrupt to the CPU after each update of the RTC time/calendar registers. For more detailed information on the operation of the RTC update cycle, see section 5 on page 25.

To use the RTC update-ended interrupt:

- ❏ Enable the RTC update-ended interrupt by setting the UIE bit in RTCINTEN.
- ❏ Enable the RTC interrupt in the CPU interrupt enable register 1 (IER1).

When the update-ended interrupt occurs, the UF and IRQF flags in RTCINTFL are set and the RTC interrupt is sent to the CPU.

5 Real-Time Clock Update Cycle

The RTC executes an update cycle once per second to update the current time in the time/calendar registers. This update occurs regardless of the SET bit value in the interrupt enable register (RTCINTEN). When the SET bit is set to 1, the time, calendar, and alarm registers are double buffered and become separate from the actual time, calendar, and alarm registers. This allows the RTC to maintain accuracy independent of reading or writing to the buffers. The update cycle also compares each alarm register with the corresponding time register. These comparisons are done to determine when to trigger an alarm.

The RTC provides two mechanisms to indicate when the time/calendar registers are updated:

- The first method uses the update-ended interrupt enable (UIE) bit in RTCINTEN. If the update-ended interrupt is enabled, an interrupt occurs after every update cycle. When the interrupt occurs, the update flag (UF) is set, indicating that an update has just been completed.
- The second method uses the update-in-progress (UIP) bit in the periodic interrupt selection register (RTCPINTR) to determine if the update cycle is in progress. When UIP goes high, an update occurs within 244 μs. When UIP returns low again, the update has been completed.

6 Power, Emulation, and Reset Considerations

The following sections describe how the RTC is affected by DSP low power modes (idle configurations), emulation breakpoints and a DSP reset.

6.1 Real-Time Clock Response to Low Power Modes (Idle Configurations)

The DSP is divided into idle domains that can be programmed to be idle or active. The state of all domains is called the idle configuration. The RTC runs on its own external clock source and is not affected by any of the DSP idle domains.

6.2 Emulation Modes of the Real-Time Clock

The RTC always continues to run regardless of the state (running/halted) of the emulation debugger software.

6.3 Real-Time Clock After a DSP Reset

A DSP reset resets only certain register fields in the RTC. The time/calendar and alarm registers are not affected by a DSP reset. For detailed information on how each RTC register responds to a DSP reset, see the register descriptions in section 7.

7 Real-Time Clock Registers

The RTC registers are listed in Table 6 and described in detail in the sections that follow.

Table 6. Real-Time Clock Registers

Address	Name	Description	See ...
1800h	RTCSEC	Seconds Register	This page
1801h	RTCSECA	Seconds Alarm Register	Page 28
1802h	RTCMIN	Minutes Register	Page 28
1803h	RTCMINA	Minutes Alarm Register	Page 29
1804h	RTCHOUR	Hours Register	Page 29
1805h	RTCHOURA	Hours Alarm Register	Page 30
1806h	RTCDAYW	Day of the Week and Day Alarm Register	Page 32
1807h	RTCDAYM	Day of the Month (Date) Register	Page 32
1808h	RTCMONTH	Month Register	Page 33
1809h	RTCYEAR	Year Register	Page 33
180Ah	RTCPINTR	Periodic Interrupt Selection Register	Page 34
180Bh	RTCINTEN	Interrupt Enable Register	Page 35
180Ch	RTCINTFL	Interrupt Flag Register	Page 37
180Dh–1BFFh	–	Reserved	–

7.1 Seconds Register (RTCSEC)

Figure 2. Seconds Register (RTCSEC)

7							0
SEC							
R/W–U							

Legend: R = Read; W = Write; –U = Value unchanged by reset

Table 7. Seconds Register (RTCSEC) Field Values

Bit	Field	BCD Value	Description
7–0	SEC	00–59	Seconds select bits. This BCD value sets the seconds value of the current time.

7.2 Seconds Alarm Register (RTCSECA)

Figure 3. Seconds Alarm Register (RTCSECA)

7							0
SAR							
R/W−U							

Legend: R = Read; W = Write; −U = Value unchanged by reset

Table 8. Seconds Alarm Register (RTCSECA) Field Values

Bit	Field	BCD Value	Description
7−0	SAR	00−59	Seconds alarm select bits. This BCD value sets the seconds value of the alarm time.

7.3 Minutes Register (RTCMIN)

Figure 4. Minutes Register (RTCMIN)

7							0
MIN							
R/W−U							

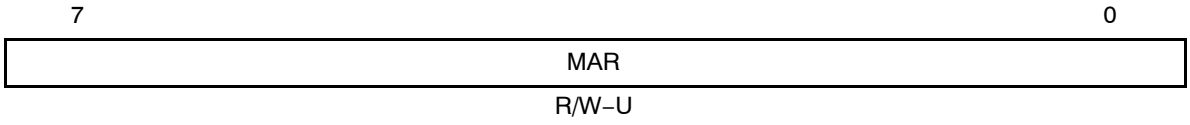
Legend: R = Read; W = Write; −U = Value unchanged by reset

Table 9. Minutes Register (RTCMIN) Field Values

Bit	Field	BCD Value	Description
7−0	MIN	00−59	Minutes select bits. This BCD value sets the minutes value of the current time.

7.4 Minutes Alarm Register (RTCMINA)

Figure 5. Minutes Alarm Register (RTCMINA)



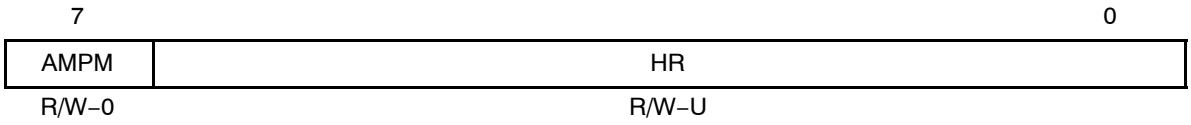
Legend: R = Read; W = Write; –U = Value unchanged by reset

Table 10. Minutes Alarm Register (RTCMINA) Field Values

Bit	Field	BCD Value	Description
7–0	MAR	00–59	Minutes alarm select bits. This BCD value sets the minute of the alarm time. When bits 7 and 6 are set to 1, a “don’t care” condition is set and the RTC generates an interrupt every minute.

7.5 Hours Register (RTCHOUR)

Figure 6. Hours Register (RTCHOUR)



Legend: R = Read; W = Write; –*n* = Value after reset; –U = Value unchanged by reset

Table 11. Hours Register (RTCHOUR) Field Values

Bit	Field	BCD Value	Description
7	AMPM		AM/PM select bit.
		0	Time is set for AM.
		1	Time is set for PM.

Table 11. Hours Register (RTCHOUR) Field Values (Continued)

Bit	Field	BCD Value	Description
6–0	HR		Hours select bits. This BCD value sets the hour of the time.
			For 12-hour mode (TM = 0 in RTCINTEN):
		01–12	This BCD value sets the hour of the current time in conjunction with the AMPM bit. For AM, AMPM bit must be cleared to 0; for PM, AMPM bit must be set to 1.
			For 24-hour mode (TM = 1 in RTCINTEN):
		00–23	This BCD value sets the hour of the current time. The AMPM bit must be cleared to 0.

7.6 Hours Alarm Register (RTCHOURA)

Figure 7. Hours Alarm Register (RTCHOURA)

7	6	0
AMPM	HAR	
R/W–0	R/W–U	

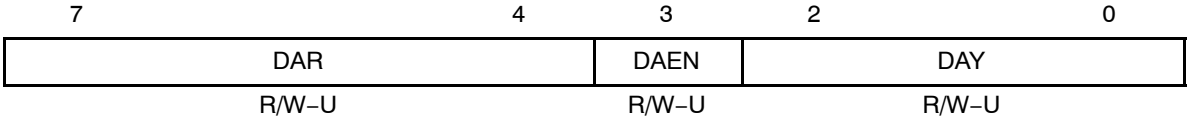
Legend: R = Read; W = Write; –*n* = Value after reset, –U = Value unchanged by reset

Table 12. Hours Alarm Register (RTCHOURA) Field Values

Bit	Field	BCD Value	Description
7	AMPM		AM/PM select bit.
		0	Alarm time is set for AM or is in 24-hour mode.
		1	Alarm time is set for PM.
6–0	HAR		Hours alarm select bits. This BCD value sets the hour of the alarm time. When bits 7 and 6 are set to 1, a “don’t care” condition is set and the RTC generates an interrupt every hour.
			For 12-hour mode (TM = 0 in RTCINTEN):
		01–12	This BCD value sets the hour of the alarm time in conjunction with the AMPM bit. For AM, AMPM bit must be cleared to 0; for PM, AMPM bit must be set to 1.
			For 24-hour mode (TM = 1 in RTCINTEN):
		00–23	This BCD value sets the hour of the alarm time. The AMPM bit must be cleared to 0.

7.7 Day of the Week and Day Alarm Register (RTCDAYW)

Figure 8. Day of the Week and Day Alarm Register (RTCDAYW)



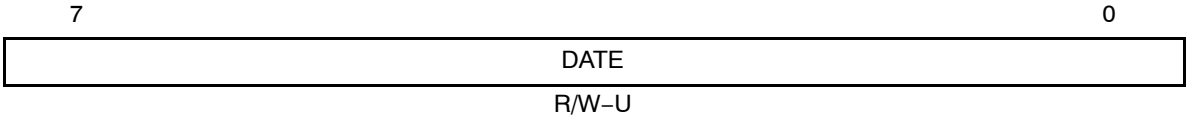
Legend: R = Read; W = Write; –U = Value unchanged by reset

Table 13. Day of the Week and Day Alarm Register (RTCDAYW) Field Values

Bit	Field	BCD Value	Description
7–4	DAR	1–7	Day-of-the-week alarm select bits. This BCD value sets the day-of-the-week alarm (Sunday = 1). When bit 7 is set to 1 (values 1000b-1111b), a “don’t care” condition is set and the RTC generates an interrupt every day.
3	DAEN		Day-of-the-week alarm enable bit.
		0	Day-of-the-week alarm is disabled.
		1	Day-of-the-week alarm is enabled. The day-of-the-week alarm is set to BCD value of DAR bits.
2–0	DAY	1–7	Day-of-the-week select bits. This BCD value sets the current day of the week (Sunday = 1).

7.8 Day of the Month (Date) Register (RTCDAYM)

Figure 9. Day of the Month (Date) Register (RTCDAYM)



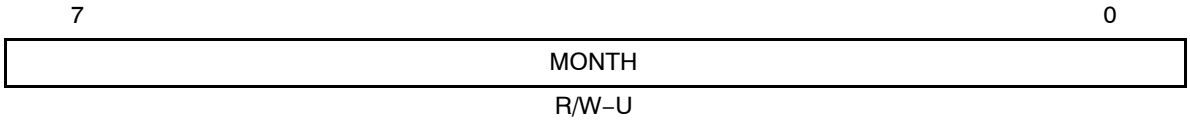
Legend: R = Read; W = Write; –U = Value unchanged by reset

Table 14. Day of the Month (Date) Register (RTCDAYM) Field Values

Bit	Field	BCD Value	Description
7–0	DATE	01–31	Date select bits. This BCD value sets the date of the calendar.

7.9 Month Register (RTCMONTH)

Figure 10. Month Register (RTCMONTH)



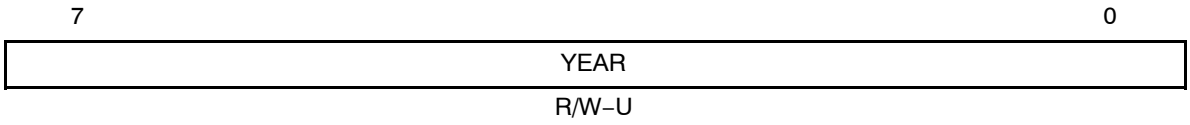
Legend: R = Read; W = Write; −U = Value unchanged by reset

Table 15. Month Register (RTCMONTH) Field Values

Bit	Field	BCD Value	Description
7−0	MONTH	01−12	Month select bits. This BCD value sets the month of the calendar (January = 01).

7.10 Year Register (RTCYEAR)

Figure 11. Year Register (RTCYEAR)



Legend: R = Read; W = Write; −U = Value unchanged by reset

Table 16. Year Register (RTCYEAR) Field Values

Bit	Field	BCD Value	Description
7−0	YEAR	00−99	Year select bits. This BCD value sets the year of the calendar.

7.11 Interrupt Registers

The RTC has three interrupt control registers that can be accessed at any time.

7.11.1 Periodic Interrupt Selection Register (RTCPINTR)

Figure 12. Periodic Interrupt Selection Register (RTCPINTR)

7	6	5	4	0
UIP	Reserved		RATE	
R−U	R−0		R/W−U	

Legend: R = Read; W = Write; −*n* = Value after reset, −U = Value unchanged by reset

Table 17. Periodic Interrupt Selection Register (RTCPINTR) Field Values

Bit	Field	Value	Description
7	UIP		Update-in-progress bit.
		0	An update cycle is not currently in progress.
		1	An update cycle is currently in progress.
6−5	Reserved		These read-only reserved bits always return 0s.

Table 17. Periodic Interrupt Selection Register (RTCPINTR) Field Values (Continued)

Bit	Field	Value	Description
4–0	RATE		Periodic interrupt rate select bits.
		00000	No interrupt.
		00001	Reserved.
		00010	Reserved.
		00011	Periodic interrupt occurs every 122.070 μs (8192 per second).
		00100	Periodic interrupt occurs every 244.141 μs (4096 per second).
		00101	Periodic interrupt occurs every 488.281 μs (2048 per second).
		00110	Periodic interrupt occurs every 976.5625 μs (1024 per second).
		00111	Periodic interrupt occurs every 1.953125 ms (512 per second).
		01000	Periodic interrupt occurs every 3.90625 ms (256 per second).
		01001	Periodic interrupt occurs every 7.8125 ms (128 per second).
		01010	Periodic interrupt occurs every 15.625 ms (64 per second).
		01011	Periodic interrupt occurs every 31.25 ms (32 per second).
		01100	Periodic interrupt occurs every 62.5 ms (16 per second).
		01101	Periodic interrupt occurs every 125 ms (8 per second).
		01110	Periodic interrupt occurs every 250 ms (4 per second).
		01111	Periodic interrupt occurs every 500 ms (2 per second).
		10000-11111	Periodic interrupt occurs every minute.

7.11.2 Interrupt Enable Register (RTCINTEN)

Figure 13. Interrupt Enable Register (RTCINTEN)

7	6	5	4	3	2	1	0
SET	PIE	AIE	UIE	Reserved		TM	Reserved
R/W–U	R/W–0	R/W–0	R/W–0	R–0		R/W–U	R–0

Legend: R = Read; W = Write; –*n* = Value after reset; –U = Value unchanged by reset

Table 18. Interrupt Enable Register (RTCINTEN) Field Values

Bit	Field	Value	Description
7	SET		SET bit isolates or connects the write and read buffers from the time, calendar, and alarm registers. The SET bit is a read/write bit that is not affected by the DSP $\overline{\text{RESET}}$ signal.
		0	The write and read buffers are connected to the time, calendar, and alarm registers.
		1	The write and read buffers are isolated from the time, calendar, and alarm registers so that a read or write operation can be executed independent of the update cycle.
6	PIE		Periodic interrupt enable bit allows the periodic interrupt flag (PF) bit in the interrupt flag register (RTCINTFL) to cause an RTC interrupt to the DSP CPU. The PIE bit is a read/write bit that is cleared by a DSP reset.
		0	Periodic interrupts are disabled.
		1	Periodic interrupts are enabled.
5	AIE		Alarm interrupt enable (AIE) bit allows the alarm interrupt flag (AF) bit in the interrupt flag register (RTCINTFL) to cause an RTC interrupt to the DSP CPU. The AIE bit is a read/write bit that is cleared by a DSP reset.
		0	Alarm interrupts are disabled.
		1	Alarm interrupts are enabled.
4	UIE		Update-ended interrupt enable (UIE) bit allows the update-ended flag (UF) bit in the interrupt flag register (RTCINTFL) to cause an RTC interrupt to the DSP CPU. The UIE bit is a read/write bit that is cleared by a DSP reset.
		0	Update-ended interrupts are disabled.
		1	Update-ended interrupts are enabled.
3–2	Reserved		These read-only reserved bits always return 0s.
1	TM		Time mode bit indicates whether the hour byte is in 24-hour mode or 12-hour mode. The TM bit is a read/write bit that is not affected by a DSP reset.
		0	12-hour mode.
		1	24-hour mode.
0	Reserved		These read-only reserved bits always return 0s.

7.11.3 Interrupt Flag Register (RTCINTFL)

Figure 14. Interrupt Flag Register (RTCINTFL)

7	6	5	4	3 – 0
IRQF	PF	AF	UF	Reserved
R–0	R–0	R–0	R–0	R–0

Legend: R = Read; W = Write; –*n* = Value after reset

Table 19. Interrupt Flag Register (RTCINTFL) Field Values

Bit	Field	Value	Description
7	IRQF		Interrupt request status flag bit indicates if an interrupt has occurred.
		0	No interrupt flags are set.
		1	One or more of the interrupt flags and the corresponding enables are set. Any time the IRQF bit is set, an RTC interrupt request is sent to the DSP CPU. To clear an interrupt flag, write a 1 to the interrupt flag bit that caused the interrupt.
6	PF		Periodic interrupt flag bit indicates if a periodic interrupt has occurred.
		0	No periodic interrupt occurred.
		1	Periodic interrupt has occurred. The PF bit can only be set if the PIE bit in the interrupt enable register (RTCINTEN) is also set (enabled). The PF bit is cleared by a DSP reset or by writing a 1 into this bit.
5	AF		Alarm interrupt flag bit indicates if an alarm interrupt has occurred.
		0	No alarm interrupt occurred.
		1	Alarm interrupt has occurred. The AF bit can only be set if the AIE bit in the interrupt enable register (RTCINTEN) is also set (enabled). The AF bit is cleared by a DSP reset or by writing a 1 into this bit.
4	UF		Update-ended interrupt flag bit indicates if an update-ended interrupt has occurred.
		0	No update-ended interrupt occurred.
		1	Update-ended interrupt has occurred. The UF bit can only be set if the UIE bit in the interrupt enable register (RTCINTEN) is also set (enabled). The UF bit is cleared by a DSP reset or by writing a 1 into this bit.
3–0	Reserved		These read-only reserved bits always return 0s.

Revision History

This document was revised to SPRU594B from SPRU594A, which was released in November 2003.

The scope of this revision was limited to adding support for the TMS320VC5503/5507 devices, and some minor edits.

The following changes were made in this revision:

Page	Additions/Modifications/Deletions
Global	Added the TMS320VC5503/5507 devices.
11	Changed the description of one of the features to: Supports external 32.768-kHz crystal or external clock source of the same frequency.
13	Removed last two sentences from first paragraph of section 1.2.

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