TMS320C6000 DSP
External Memory Interface (EMIF)

Reference Guide

Literature Number: SPRU266E
April 2008

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About This Manual

This document describes the operation of the external memory interface (EMIF) in the digital signal processors (DSPs) of the TMS320C6000™ DSP family. For operation and registers unique in the TMS320C620x/C670x EMIF, see Chapter 2. For operation and registers unique in the TMS320C621x/C671x EMIF, see Chapter 3. For operation and registers unique in the TMS320C64x™ EMIF, see Chapter 4.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the C6000 devices, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRU189 — *TMS320C6000 DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C6000 digital signal processors (DSPs).

SPRU190 — *TMS320C6000 DSP Peripherals Overview Reference Guide.* Provides an overview and briefly describes the peripherals available on the TMS320C6000 family of digital signal processors (DSPs).

SPRU197 — *TMS320C6000 Technical Brief.* Provides an introduction to the TMS320C62x and TMS320C67x digital signal processors (DSPs) of the TMS320C6000 DSP family. Describes the CPU architecture, peripherals, development tools and third-party support for the C62x and C67x DSPs.

SPRU395 — *TMS320C64x Technical Overview.* Provides an introduction to the TMS320C64x digital signal processors (DSPs) of the TMS320C6000 DSP family.

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Overview

This chapter provides an overview and describes the common operation of the external memory interface (EMIF) in the digital signal processors (DSPs) of the TMS320C6000™ DSP family. For operation and registers unique in the TMS320C620x/C670x™ EMIF, see Chapter 2. For operation and registers unique in the TMS320C621x/C671x™ EMIF, see Chapter 3. For operation and registers unique in the TMS320C64x™ EMIF, see Chapter 4.

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1.1 Overview

The external memory interfaces (EMIFs) of all C6000 devices support a glueless interface to a variety of external devices, including:

- Pipelined synchronous-burst SRAM (SBSRAM)
- Synchronous DRAM (SDRAM)
- Asynchronous devices, including SRAM, ROM, and FIFOs
- An external shared-memory device

Table 1-1 summarizes the differences between the C6000 EMIFs.

Table 1-1. Differences Between the C62x/C67x and C64x EMIF

	C62x/C67x EMIF			C64x EMIF[1]		
				EMIFA		EMIFB
Feature	C6201/C6701	Other C620x/C670x	C621x/C671x[2]	C6416/15/14/12, DM642/643	C6411, DM640/641	C6416/15/14
Bus width	32-bit	32-bit	32-bit[2]	64-bit	32-bit	16-bit
Number of memory spaces	4	4	4	4	4	4
Addressable space (Mbytes)	52	52	512[2]	1024	512	256
Synchronous clocking	CPU clock and/or 1/2ıCPU clock	1/2ıCPU clock	Independent ECLKIN	Independent ECLKIN, 1/4ıCPU clock or 1/6ıCPU clock	Independent ECLKIN, 1/4ıCPU clock or 1/6ıCPU clock	Independent ECLKIN, 1/4ıCPU clock or 1/6ıCPU clock
Width support	32 bit; 8-/16-bit ROM	32 bit; 8-/16-bit ROM	8-/16-bit, 32-bit[2]	8-, 16-, 32-, or 64-bit	8-, 16-, or 32-bit	8-bit or 16-bit
Supported memory type at CE1	Asynchronous memory	Asynchronous memory	All types	All types	All types	All types
Control signals	Separate	Muxed synchronous signals	Muxed all control signals	Muxed all control signals	Muxed all control signals	Muxed all control signals
Synchronous memory in system	Both SDRAM and SBSRAM	Either SDRAM or SBSRAM	Both SDRAM and SBSRAM	All synchronous	All synchronous	All synchronous
Additional registers	—	—	SDEXT	SDEXT CESEC	SDEXT CESEC	SDEXT CESEC
PDT support	No	No	No	Yes	Yes	Yes
ROM/Flash	√	√	√	√	√	√
Asynchronous memory I/O	√	√	√	√	√	√
Pipeline SBSRAM	√	√	√	√	√	√
Flow thru SBSRAM				√	√	√
ZBT SRAM				√	√	√
Standard Synchronous FIFO				√	√	√
FWFT FIFO				√	√	√

(1) On the C64x DSP, the EMIFA bus width is device specific, either 64-bit or 32-bit wide. EMIFB has a 16-bit bus width.
(2) On the C6712/C6712C DSP, the EMIF is only 16-bits wide. Addressable space is 256M bytes. It supports memory widths of 8 bits and 16 bits.

1.2 Command-to-Command Turnaround Time

The C6000 EMIF has a one cycle command-to-command turnaround time. At least 1 data dead cycle is always included between commands so that read data and write data are never driven in the same cycle.

1.3 SDRAM Interface

The C6000 EMIF supports the SDRAM commands shown in Table 1-2. Table 1-3 shows the signal truth table for the SDRAM commands. The 16-bit EMIF, 32-bit EMIF, and 64-bit EMIF table entries refer to the total bus width of the EMIF and not the size of the transfer. Table 1-4 summarizes the pin connection and related signals specific to SDRAM operation. Table 1-5 summarizes the similarities and differences on the C6000 SDRAM interface.

Table 1-2. TMS320C6000 EMIF SDRAM Commands

Command	Function
ACTV	Activates the selected bank and selects the row
DCAB	Deactivates (also known as PRECHARGE) all banks
DEAC(1)	Deactivates a single bank
MRS	Mode register set, configures SDRAM mode register
READ	Inputs the starting column address and begins the read operation
REFR	Autorefresh cycle with internal address
SLFREFR(2)	Self-refresh mode
WRT	Inputs the starting column address and begins the write operation

(1) TMS320C621x/C671x/C64x DSP only.
(2) TMS320C64x DSP only.

Table 1-3. Truth Table for SDRAM Commands

SDRAM:	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A[19:16]	A[15:11]	A10	A[9:0]
16-bit EMIF: (1)	**SDCKE**	$\overline{CE}$	$\overline{SDRAS}$	$\overline{SDCAS}$	$\overline{SDWE}$	**EA[20:17]** (2)	**EA[16:12]**	**EA11**	**EA[10:1]**
32-bit EMIF: (1)	**SDCKE** (3)	$\overline{CE}$	$\overline{SDRAS}$	$\overline{SDCAS}$	$\overline{SDWE}$	**EA[21:18]** (4)	**EA[17:13]**	**EA12** (5)	**EA[11:2]** (6)
64-bit EMIF: (1)	**SDCKE**	$\overline{CE}$	$\overline{SDRAS}$	$\overline{SDCAS}$	$\overline{SDWE}$	**EA[22:19]** (2)	**EA[18:14]**	**EA13**	**EA[12:3]** (7)
ACTV	H	L	L	H	H	0001b or 0000b (4)	Bank/Row	Row	Row
READ	H	L	H	L	H	X	Bank/ Column	L	Column
WRT	H	L	H	L	L	X	Bank/ Column	L	Column
MRS	H	L	L	L	L	L	L/Mode	Mode	Mode
DCAB	H	L	L	H	L	X	X	H	X
DEAC	H	L	L	H	L	X	Bank/X	L	X
REFR	H	L	L	L	H	X	X	X	X
SLFREFR	L	L	L	L	H	X	X	X	X

(1) 16-bit EMIF includes C64x EMIFB; 32-bit EMIF includes all C62x/C67x EMIF, both 32-bit and 16-bit interfaces; 64-bit EMIF includes C64x EMIFA, both 64-bit and 32-bit interfaces.
(2) For C64x DSP, upper address bits are used during ACTV to indicate non-PDT (0001b) vs. PDT (0000b) access. During all other accesses, address bits indicated with X hold previous value.
(3) SDCKE does not exist on C62x/C67x DSP.
(4) For C62x/C67x DSP, upper address bits are reserved for future use. Undefined.
(5) SDA10 is used on C620x/C670x DSP. EA12 is used on C621x/C671x DSP.
(6) EMIF address numbering for the C6712/C6712C 16-bit EMIF begins with EA2 to maintain signal name compatibility with the C62x/C67x 32-bit EMIF.
(7) EMIF address numbering for the C64x 32-bit EMIFA begins with EA3 to maintain signal name compatibility with the C64x 64-bit EMIFA.

Table 1-4. TMS320C6000 SDRAM Signal Descriptions

EMIF Signal	SDRAM Signal	SDRAM Function
$\overline{BEx}$	DQMx	Data/output mask. DQM is an input/output buffer control signal. When high, it disables writes and places outputs in the high impedance state during reads. DQM has a 2-CLK-cycle latency on reads and a 0-CLK-cycle latency on writes. DQM pins serve as byte strobes and are connected to $\overline{BE}$ outputs.
$\overline{CE3}$, $\overline{CE2}$, $\overline{CE1}$[1], or $\overline{CE0}$	$\overline{CS}$	Chip select and command enable. $\overline{CS}$ must be active (low) for a command to be clocked into the SDRAM. $\overline{CE1}$ does not support SDRAM on C620x/C670x DSP.
CLKOUT2	CLK	SDRAM clock input. Runs at 1/2 the CPU clock rate. Used for synchronous memory interface on the C6202(B)/C6203(B)/C6204/C6205 DSP.
ECLKOUT	CLK	SDRAM clock input. Used for synchronous memory interface on the C621x/C671x/C64x DSP. For C6713 DSP, runs at either ECLKIN or SYSCLK3 (programmable divide-down clock with PLL output as reference clock), configurable using EKSRC bit in DEVCFG. For C621x/C671x DSP, runs at ECLKIN rate. For C64x DSP, ECLKOUT1 is used. ECLKOUT1 runs at EMIF input clock rate (ECLKIN, CPU/4 clock, or CPU/6 clock).
SDA10[2]	A10	Address line A10/autoprecharge disable. Serves as a row address bit during ACTV commands and also disables the autoprecharging function of SDRAM. (C620x/C670x DSP only)
$\overline{SDCAS}$	$\overline{CAS}$	Column address strobe and command Input. Latched by the rising edge of CLK to determine current operation. Valid only if $\overline{CS}$ is active (low) during that clock edge.
SDCKE[3]	CKE	CKE clock enable. For C64x DSP, SDCKE is connected to CKE to minimize SDRAM power consumption when self-refresh mode is enabled. For C62x/C67x SDRAM interface, CKE is tied high (on the SDRAM device) since the Self Refresh command is not supported.
SDCLK	CLK	SDRAM clock input. Runs at 1/2 the CPU clock rate. Used for SDRAM interface on C6201/C6701 DSP.
$\overline{SDRAS}$	$\overline{RAS}$	Row address strobe and command input. Latched by the rising edge of CLK to determine current operation. Valid only if $\overline{CS}$ is active (low) during that clock edge.
$\overline{SDWE}$	$\overline{WE}$	Write strobe and command input. Latched by the rising edge of CLK to determine current operation. Valid only if $\overline{CS}$ is active (low) during that clock edge.

(1) For C620x/C670x DSP, $\overline{CE1}$ does not support SDRAM.
(2) SDA10 is used on C620x/C670x DSP. EA12 is used on C621x/C671x DSP. EA13 is used on C64x EMIFA; EA11 is used on C64x EMIFB.
(3) SDCKE exists on C64x DSP only.

Table 1-5. TMS320C6000 SDRAM Interface Summary

	C62x/C67x EMIF			C64x EMIF		
				EMIFA		EMIFB
Feature	**C6201/C6701**	**Other C620x/C670x[1]**	**C621x/C671x[2]**	**C6416/15/14/12, DM642**	**C6411, DM640/641**	**C6416/15/14**
Interface width	32-bit	32-bit	32-, 16-, 8-bit	64-, 32-, 16-, 8-bit	32-, 16-, 8-bit	16-, 8-bit
SDRAM clock	SDCLK	CLKOUT2	ECLKOUT	ECLKOUT1	ECLKOUT1	ECLKOUT1
Registers for SDRAM timing parameters	SDCTL, SDTIM	SDCTL, SDTIM	SDCTL, SDTIM, SDEXT	SDCTL, SDTIM, SDEXT	SDCTL, SDTIM, SDEXT	SDCTL, SDTIM, SDEXT
SDRAM control signals	Dedicated SDRAM control signals	MUXed with SBSRAM control signals	MUXed with SBSRAM and Async control signals	MUXed with Async and Programmable Sync control signals	MUXed with Async and Programmable Sync control signals	MUXed with Async and Programmable Sync control signals
Number of open pages	Single open page per CE space	Single open page per CE space	4 open pages in any CE space	4 open pages in any CE space	4 open pages in any CE space	4 open pages in any CE space
Programmable SDRAM configuration	8- or 9-column address bits	8- or 9-column address bits	column, row, and bank size	column, row, and bank size	column, row, and bank size	column, row, and bank size
Burst mode	Not supported. Performs bursts by issuing back-to-back commands	Not supported. Performs bursts by issuing back-to-back commands	Supports SDRAM burst mode with a 4-word burst	Supports SDRAM burst mode with a 4-word burst	Supports SDRAM burst mode with a 4-word burst	Supports SDRAM burst mode with a 4-word burst
Background refresh	Yes	Yes	No	No	No	No
Precharge pin	SDA10	SDA10	EA12	EA13	EA13	EA11
SDRAM self-refresh mode	No	No	No	Yes	Yes	No
Page replacement	Fixed	Fixed	Random	LRU	LRU	LRU

(1) This column applies to all C620x/C670x devices, except C6201/C6701 DSP.
(2) C6712/C6712C DSP interfaces to 8-bit and 16-bit SDRAM only.

1.3.1 SDRAM Initialization

After reset, none of the CE spaces are configured as SDRAM. The CPU should initialize all of the CE space control registers and the SDRAM extension register before performing SDRAM initialization by setting the INIT bit to 1. If SDRAM does not exist in the system, you should not write a 1 to the INIT bit.

The EMIF performs the following steps when INIT is set to 1:

1. Sends a DCAB command to all CE spaces configured as SDRAM.
2. Sends eight refresh commands.
3. Sends an MRS command to all CE spaces configured as SDRAM.

For the duration of SDRAM initialization, the $\overline{BE}$ signals are inactive high. The SDRAM initialization is noninterruptible by other EMIF accesses.

SDRAM initialization status may be monitored using the INIT bit. The INIT bit returns to 0 automatically when initialization is complete.

1.3.2 Monitoring Page Boundaries

SDRAM is a paged memory type, thus the EMIF SDRAM controller monitors the active row of SDRAM so that row boundaries are not crossed during the course of an access. To accomplish this priority, the EMIF stores the address of the open row in internal page register(s), then performs compares against that address for subsequent accesses to any SDRAM CE space.

For all C6000 devices, ending the current access is not a condition that forces the active SDRAM row to be closed. The EMIF leaves the active row open until it becomes necessary to close it. This decreases the deactivate-reactivate overhead and allows the interface to capitalize fully on the address locality of memory accesses.

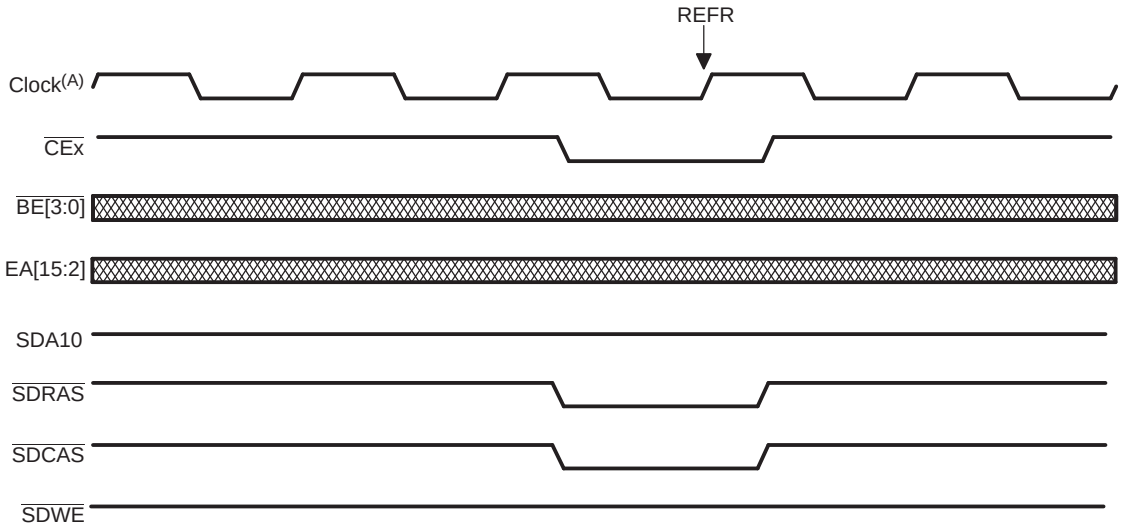
1.3.3 SDRAM Refresh Mode

The RFEN bit in the SDRAM control register (SDCTL) selects the SDRAM refresh mode of the EMIF. When RFEN = 0, all EMIF refreshes are disabled, and you must ensure that refreshes are implemented in an external device. When RFEN = 1, the EMIF performs refreshes of SDRAM.

Refresh commands (REFR) enable all $\overline{CE}$ signals for all CE spaces selected to use SDRAM (with the MTYPE field of the CE space control register). REFR is automatically preceded by a DCAB command, ensuring the deactivation of all CE spaces selected with SDRAM. Following the DCAB command, the EMIF begins performing trickle refreshes at a rate defined by the PERIOD value in SDTIM, provided no other SDRAM access is pending.

For all C6000 devices, the EMIF SDRAM interface performs $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles for SDRAM. Some SDRAM manufacturers call this autorefresh. Prior to an REFR command, a DCAB command is performed to all CE spaces specifying SDRAM to ensure the closure of all active banks. Page information is always invalid before and after a REFR command; thus, a refresh cycle always forces a page miss. A deactivate cycle is required prior to the refresh command. Figure 1-1 shows the timing diagram for an SDRAM refresh.

Figure 1-1. SDRAM Refresh Timing Diagram



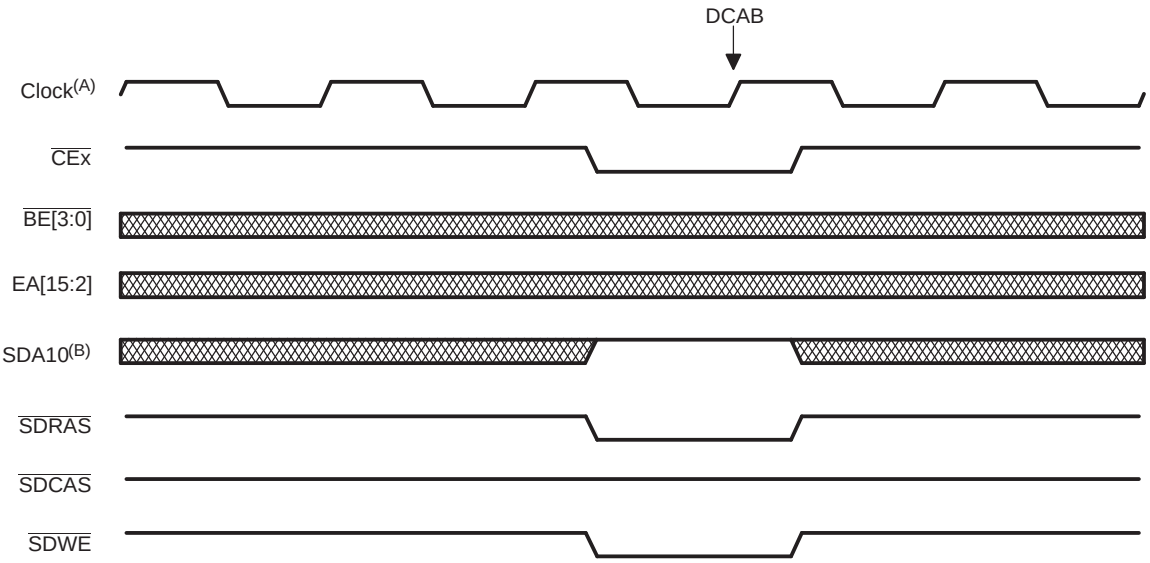
A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.
= ECLKOUT for C621x/C671x DSP.
= ECLKOUT1 for C64x DSP.

1.3.4 SDRAM Deactivation (DCAB and DEAC)

The SDRAM deactivation (DCAB) is performed after a hardware reset or when INIT = 1 in the SDRAM control register (SDCTL). The SDRAMs also require this cycle prior to a refresh (REFR) and mode set register (MRS) command. On the C6000 EMIF, a DCAB is issued when a page boundary is crossed. During the DCAB command, SDA10 is driven high to ensure the deactivation of all SDRAM banks. Figure 1-2 shows the timing diagram for SDRAM deactivation.

The C621x/C671x EMIF and C64x™ EMIF also support the DEAC command, which closes a single page of SDRAM specified by the bank select signals. When a page boundary is crossed, the DEAC command is used to close the open page. The C621x/C671x EMIF and C64x EMIF still support the DCAB command to close all pages prior to REFR and MRS commands. Figure 1-3 shows the timing diagram for SDRAM deactivation.

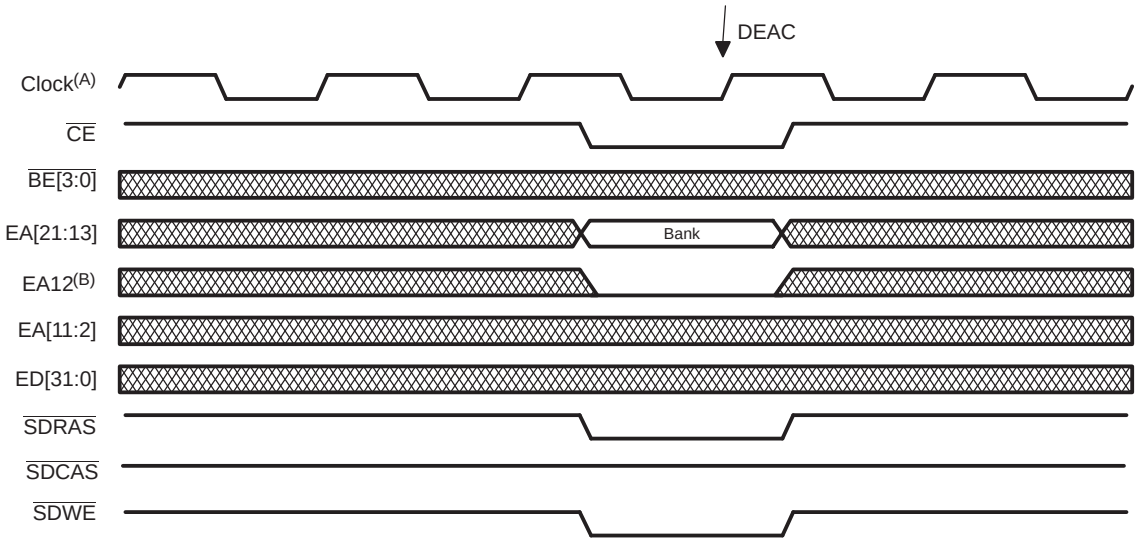
Figure 1-2. TMS320C6000 SDRAM Deactivate All Banks (DCAB) Command Timing Diagram



A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.
= ECLKOUT for C621x/C671x DSP.
= ECLKOUT1 for C64x DSP.

B SDA10 applies to C620x/C670x DSP only. On C621x/C671x DSP, EA12 is used. On C64x EMIFA, EA13 is used; on EMIFB, EA11 is used.

Figure 1-3. TMS320C621x/C671x and TMS320C64x SDRAM Deactivate Single Bank (DEAC) Command Timing Diagram



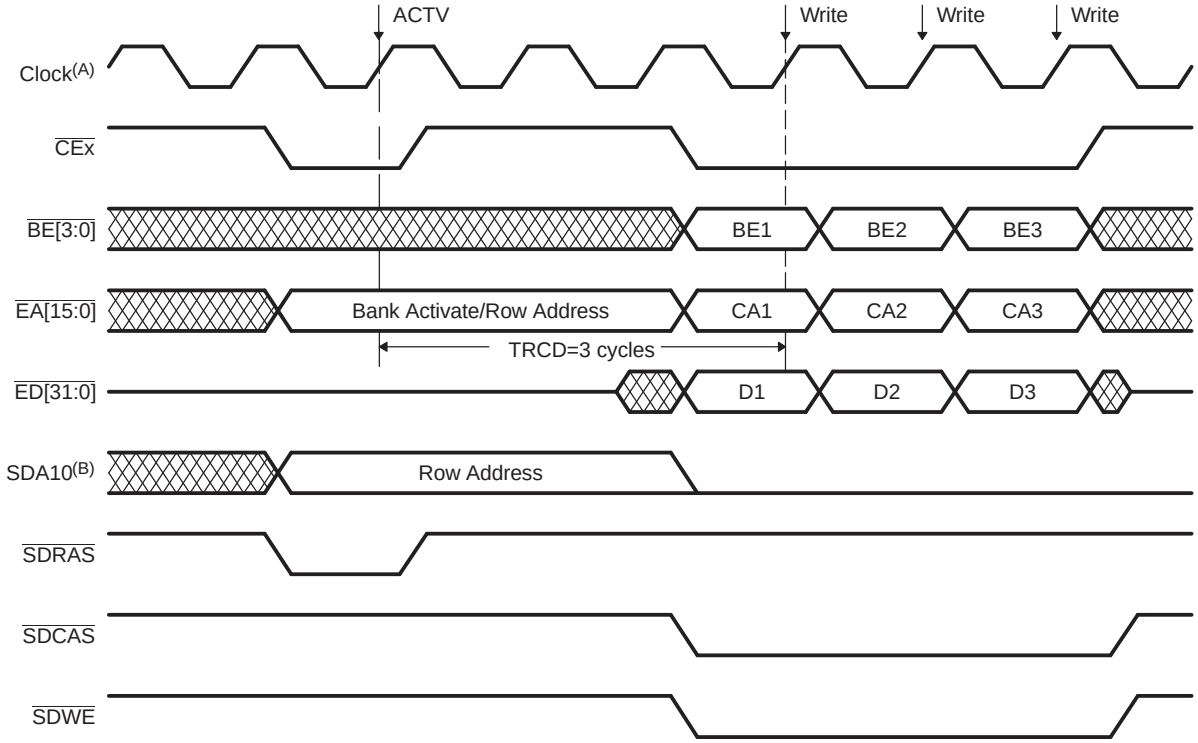
A Clock = ECLKOUT for C621x/C671x DSP.
= ECLKOUT1 for C64x DSP.

B For C64x EMIFA, EA13 is used; for EMIFB, EA11 is used.

1.3.5 SDRAM Activation (ACTV)

The C6000 EMIF automatically issues the activate (ACTV) command before a read or write to a new row of SDRAM. The ACTV command opens up a page of memory, allowing future accesses (reads or writes) with minimum latency. When the EMIF issues an ACTV command, a delay of t_{RCD} is incurred before a read or write command is issued. Figure 1-4 shows an example of an ACTV command before an SDRAM write. In this example, t_{RCD} = 3 EMIF clock cycles. The ACTV command for SDRAM reads are identical. Reads or writes to the currently active row and bank of SDRAM can achieve much higher throughput than reads or writes to random areas, because every time a new page is accessed, the ACTV command must be issued.

Figure 1-4. TMS320C6000 SDRAM Activate (ACTV) Command Before an SDRAM Write Timing Diagram



A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.
= ECLKOUT for C621x/C671x DSP.
= ECLKOUT1 for C64x DSP.

B SDA10 applies to C620x/C670x DSP only. On C621x/C671x DSP, EA12 is used. On C64x EMIFA, EA13 is used; on EMIFB, EA11 is used.

1.4 SBSRAM Interface

The C6000 EMIF interfaces directly to industry-standard synchronous burst SRAMs (SBSRAMs). This memory interface allows a high-speed memory interface without some of the limitations of SDRAM. Most notably, since SBSRAMs are SRAM devices, random accesses in the same direction can occur in a single cycle. Besides supporting the SBSRAM interface, the programmable synchronous interface on the C64x DSP supports additional synchronous device interfaces. See section Section 4.5 for details on the C64x DSP interface with the other synchronous devices. This section discusses the SBSRAM interface on all the C6000 devices.

SBSRAMs are latent by their architecture, since read data follows address and control information by two cycles. Consequently, the EMIF inserts cycles between read and write commands to ensure that no conflict exists on the ED[31:0] bus. The EMIF keeps this turnaround penalty to a minimum.

For the C6000 EMIF, the SBSRAM interface can run at either the CPU clock speed or at 1/2 of this rate, see Table 1-6. The selection is made based on the setting of the SSCRT bit in the EMIF global control register (GBLCTL).

Table 1-6. TMS320C6000 SBSRAM Operating Speeds

Device	Operates at...
C6201 DSP only	CPU clock or 1/2 CPU clock
C620x DSP	1/2 CPU clock
C6701 DSP only	CPU clock or 1/2 CPU clock
C670x DSP	1/2 CPU clock
C621x DSP	ECLKOUT
C671x DSP	ECLKOUT
C64x DSP	ECLKOUT1 or ECLKOUT2

The four SBSRAM control pins are latched by the SBSRAM on the rising EMIF clock edge to determine the current operation. Table 1-7 lists these pins. These signals are valid only if the chip select line for the SBSRAM is low.

Table 1-8 provides an overview of similarities and differences on the C6000 SBSRAM interface.

Table 1-7. TMS320C6000 SBSRAM Signal Descriptions

EMIF Signal(1)	SBSRAM Signal	SBSRAM Function
$\overline{\text{SSADS}}$	$\overline{\text{ADSC}}$	Address strobe
$\overline{\text{SSOE}}$	$\overline{\text{OE}}$	Output enable
$\overline{\text{SSWE}}$	$\overline{\text{WE}}$	Write enable
SSCLK/CLKOUT2/ECLKOUT(2)	CLK	SBSRAM clock

(1) For C64x DSP, SBSRAM control signals are renamed as $\overline{\text{SADS}}$/$\overline{\text{SRE}}$, $\overline{\text{SOE}}$, and $\overline{\text{SWE}}$, respectively.
(2) For C64x DSP, SBSRAM interface can run off of either ECLKOUT1 or ECLKOUT2.

Table 1-8. TMS320C6000 SBSRAM Interface Summary

	C62x/C67x EMIF			C64x EMIF		
				EMIFA		EMIFB
Feature	C6201/C6701	Other C620x/C670x(1)	C621x/C671x(2)	C6416/15/14/12, DM642/643	C6411, DM640/641	C6416/15/14
Interface width	32-bit	32-bit	32-, 16-, 8-bit	64-, 32-, 16-, 8-bit	32-, 16-, 8-bit	16-, 8-bit
SBSRAM clock	SSCLK (1/2 or 1 CPU rate)	CLKOUT2	ECLKOUT	ECLKOUT1 or ECLKOUT2(3)	ECLKOUT1 or ECLKOUT2(3)	ECLKOUT1 or ECLKOUT2(3)
SBSRAM control signals	Dedicated SDRAM control signals	MUXed with SDRAM control signals	MUXed with SDRAM and async control signals	MUXed with SDRAM and async control signals	MUXed with SDRAM and async control signals	MUXed with SDRAM and async control signals
Burst mode	Not supported. Performs bursts by issuing back-to-back commands	Not supported. Performs bursts by issuing back-to-back commands	Supports SBSRAM burst mode with a 4-word burst	Not supported. Performs bursts by issuing back-to-back commands. Still issues deselect command	Not supported. Performs bursts by issuing back-to-back commands. Still issues deselect command	Not supported. Performs bursts by issuing back-to-back commands. Still issues deselect command
Programmable latency	No	No	No	Read, Write	Read, Write	Read, Write

(1) This column applies to all C620x/C670x devices, except C6201/C6701 DSP.
(2) The C6712/C6712C DSP interfaces to 8-bit and 16-bit SBSRAM only.
(3) The ECLKOUT*n* used is selected by the SNCCLK bit in CESEC.

1.5 Asynchronous Interface

The asynchronous interface offers configurable memory cycle types to interface to a variety of memory and peripheral types, including SRAM, EPROM, and flash memory, as well as FPGA and ASIC designs. Table 1-9 lists the asynchronous interface pins.

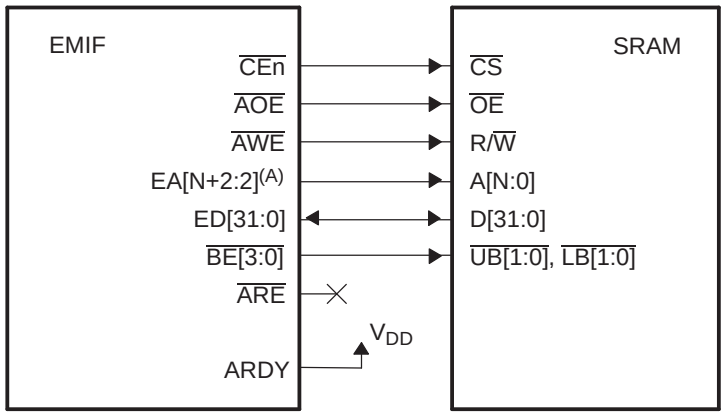
Figure 1-5 shows an EMIF interface to standard SRAM. Figure 1-6, Figure 1-7, and Figure 1-8 show EMIF interfaces to 8-, 16-, and 32-bit ROM, respectively

Table 1-10 provides an overview of similarities and differences on the C6000 ASRAM interface.

Table 1-9. Asynchronous Interface Signal Descriptions

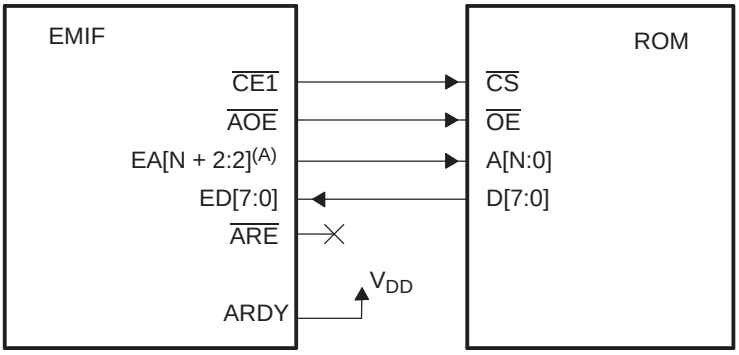
EMIF Signal	Function
$\overline{\text{AOE}}$	Output enable. Active (low) during the entire period of a read access.
$\overline{\text{AWE}}$	Write enable. Active (low) during a write transfer strobe period.
$\overline{\text{ARE}}$	Read enable. Active (low) during a read transfer strobe period.
ARDY	Ready. Input used to insert wait states into the memory cycle.

Figure 1-5. EMIF to 32-bit SRAM Interface Block Diagram



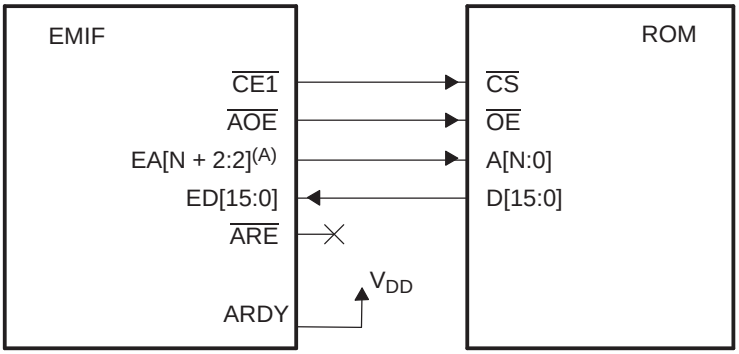
A For C64x EMIFA, EA[N + 3:3] is used; for EMIFB, EA[N + 1:1] is used.

Figure 1-6. EMIF to 8-Bit ROM Interface Block Diagram



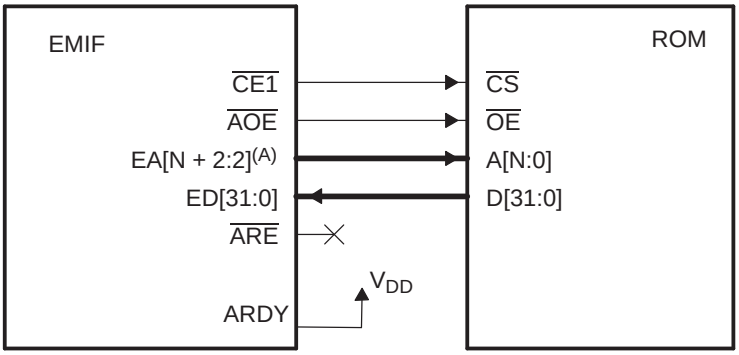
A For C64x EMIFA, EA[N + 3:3] is used; for EMIFB, EA[N + 1:1] is used.

Figure 1-7. EMIF to 16-Bit ROM Interface Block Diagram



A For C64x EMIFA, EA[N + 3:3] is used; for EMIFB, EA[N + 1:1] is used.

Figure 1-8. EMIF to 32-Bit ROM Interface Block Diagram



A For C64x EMIFA, EA[N + 3:3] is used; for EMIFB, EA[N + 1:1] is used.

Table 1-10. TMS320C6000 ASRAM Interface Summary

	C62x/C67x EMIF		C64x EMIF		
			EMIFA		EMIFB
Feature	C620x/C670x	C621x/C671x[1]	C6416/15/14/12, DM642/643	C6411, DM640/641	C6416/15/14
Interface width	32-bit ASRAM; ‘2, ‘16, ROM	32-, 16-, 8-bit	64-, 32-, 16-, 8-bit	32-, 16-, 8-bit	16-, 8-bit
Internal synchronization	CLKOUT1	ECLKOUT	ECLKOUT1	ECLKOUT1	ECLKOUT1
Control signals	Dedicated ASRAM control signals.	ASRAM control signals are MUXed with SDRAM and SBSRAM control signals.	ASRAM control signals are MUXed with SDRAM and programmable synchronous control signals.	ASRAM control signals are MUXed with SDRAM and programmable synchronous control signals.	ASRAM control signals are MUXed with SDRAM and programmable synchronous control signals.
Memory endianness	Packing format in ROM is little-endian only.	Supports both little- or big-endian.	Supports both little- or big-endian.	Supports both little- or big-endian.	Supports both little- or big-endian.

(1) C6712/C6712C DSP interfaces to 8-bit and 16-bit SDRAM only.

Although the C620x/C670x EMIF ROM can be interfaced at any of the CE spaces, it is often used at CE1 because that space can be configured for widths of less than 32 bits. See Section 2.6 for more details.

The C621x/C671x EMIF and C64x EMIF allow widths of less than 32 bits on any CE space, as shown in the MTYPE description of CECTL. The asynchronous interface signals on the C621x/C671x EMIF and C64x EMIF are similar to the C6201 EMIF, except that the signals have been combined with the SDRAM and SBSRAM memory interface. It has also been enhanced to allow for longer read hold time, and the 8-bit and 16-bit interface modes have been extended to include writable asynchronous memories, instead of ROM devices. To avoid bus contention, a programmable turnaround time (TA) also allows you to control the minimum number of cycles between a read followed by a write (same or different CE spaces), or between reads from different CE spaces.

1.5.1 Programmable ASRAM Parameters

The C6000 EMIF allows a high degree of programmability for shaping asynchronous accesses. The programmable parameters are:

- **Setup:** The time between the beginning of a memory cycle ($\overline{CE}$ low, address valid) and the activation of the read or write strobe.
- **Strobe:** The time between the activation and deactivation of the read ($\overline{ARE}$) or write strobe ($\overline{AWE}$).
- **Hold:** The time between the deactivation of the read or write strobe and the end of the cycle, which can be either an address change or the deactivation of the $\overline{CE}$ signal.

For the C620x/C670x EMIF, these parameters are programmable in terms of CPU clock cycles using fields in the CE space control register (CECTL). For the C621x/C671x EMIF and C64x EMIF, these parameters are programmed in terms of ECLKOUT (or ECLKOUT1) cycles. Separate setup, strobe, and hold timing parameters are available for read and write accesses. Minimum values for ASRAM are:

- SETUP ≥ 1 (0 treated as 1)
- STROBE ≥ 1 (0 treated as 1)
- HOLD ≥ 0
- On the C620x/C670x EMIF, for the first access in a set of consecutive accesses or a single access, the setup period has a minimum count of 2.

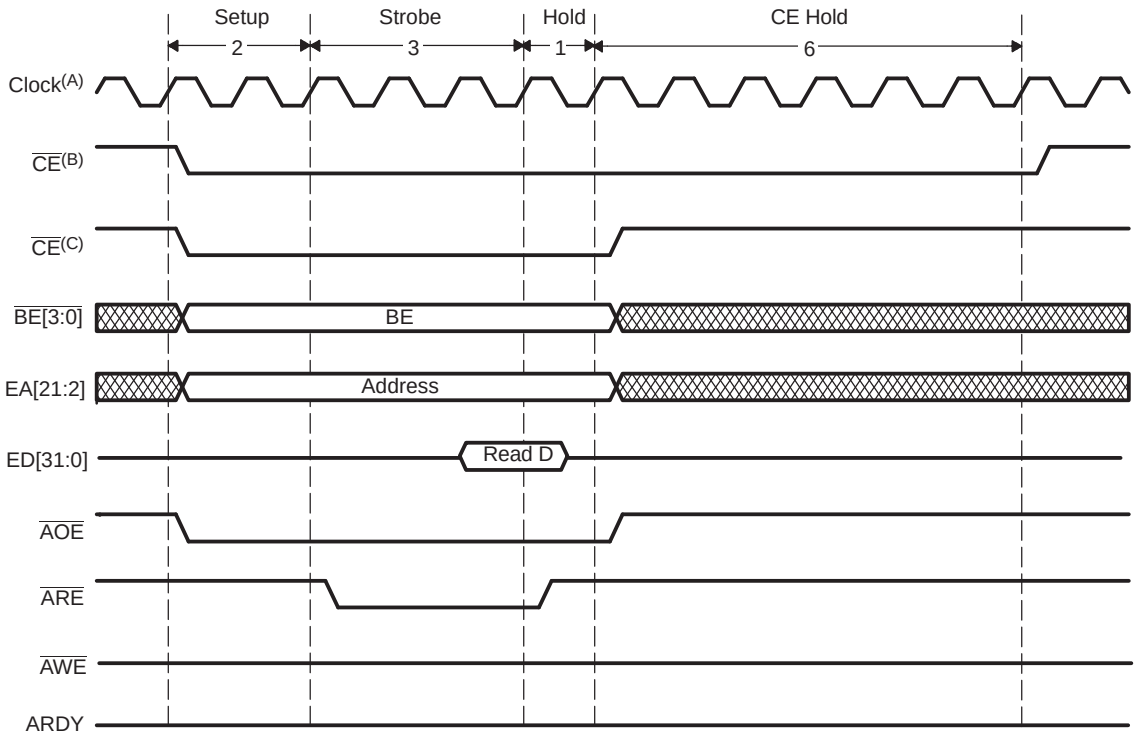
1.5.2 Asynchronous Reads

Figure 1-9 shows an asynchronous read with the setup, strobe, and hold parameter programmed with the values 2, 3, and 1, respectively. An asynchronous read proceeds as:

- At the beginning of the setup period:
  - $\overline{CE}$ becomes active.

  - $\overline{AOE}$ becomes active.
  - $\overline{BE}[3:0]$ becomes valid.
  - EA becomes valid.
  - For the C620x/C670x EMIF, the first access has a setup period minimum value of 2. After the first access, setup has a minimum value of 1.
- At the beginning of a strobe period, $\overline{ARE}$ becomes active.
- At the beginning of a hold period:
  - $\overline{ARE}$ becomes inactive (high).
  - Data is sampled on the CLKOUT1 or the ECLKOUT rising edge concurrent with the beginning of the hold period (the end of the strobe period) and just prior to the $\overline{ARE}$ low-to-high transition.
- At the end of the hold period:
  - $\overline{AOE}$ becomes inactive as long as another read access to the same CE space is not scheduled for the next cycle.
  - $\overline{CE}$ becomes inactive only if another read or write access to the same CE space is not pending.
- For the C620x/C670x EMIF, CE stays active for 7 minus the value of read hold cycles after the last access (DMA transfer or CPU access). For example, if read HOLD = 1, then CE stays active for six more cycles. This does not affect performance and merely reflects the EMIF's overhead.
- For the C621x/C671x EMIF and C64x EMIF, the $\overline{CEn}$ signal goes high just after the programmed hold period.

Figure 1-9. Asynchronous Read Timing Diagram



A Clock = CLKOUT1 for C620x/C670x DSP.
= ECLKOUT for C621x/C671x DSP.
= ECLKOUT1 for C64x DSP.

B $\overline{CE}$ waveform for C620x/C670x DSP.

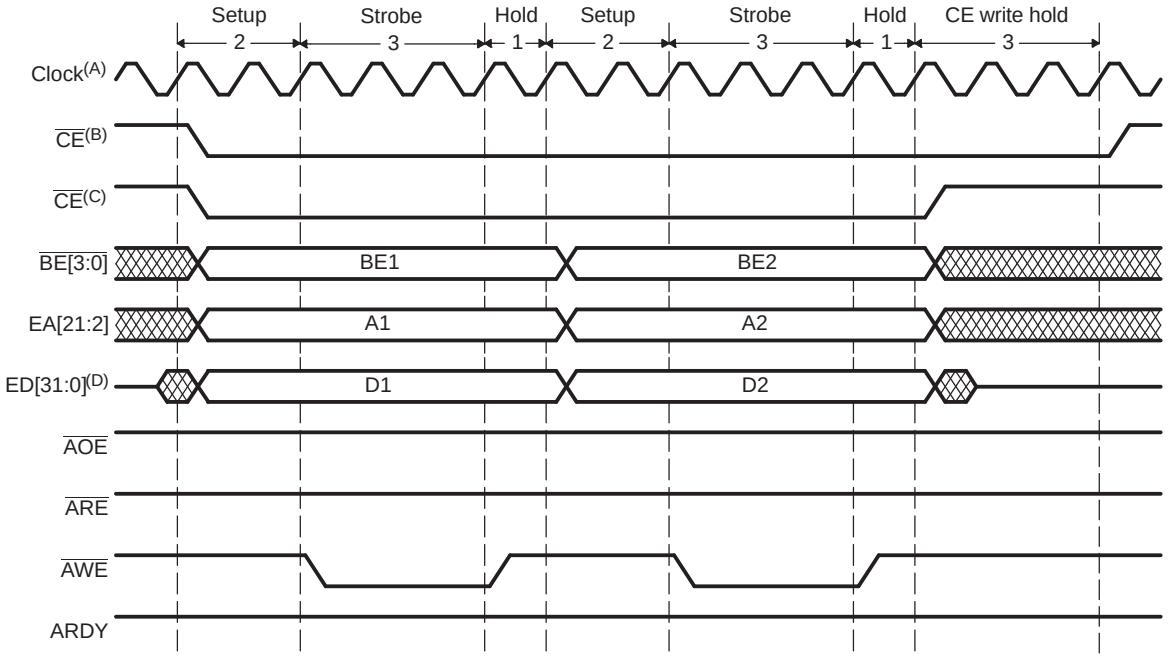
C $\overline{CE}$ waveform for C621x/C671x DSP and C64x DSP.

1.5.3 Asynchronous Writes

Figure 1-10 shows two back-to-back asynchronous write cycles with the ARDY signal pulled high (always ready). The SETUP, STROBE, and HOLD are programmed to 2, 3, and 1, respectively.

- At the beginning of the setup period:
  - CE becomes active.
  - BE[3:0] becomes valid.
  - EA becomes valid.
  - ED becomes valid. For the C621x/C671x EMIF, see section Section 1.5.3.1 for the exact cycle where ED becomes valid.
- At the beginning of a strobe period, AWE becomes active.
- At the beginning of a hold period, AWE becomes inactive.
- At the end of the hold period:
  - ED goes into the high-impedance state only if another write access to the same CE space is not scheduled for the next cycle.
  - CE becomes inactive only if another read or write access to the same CE space is not pending.
- For the C620x/C670x EMIF: If no write accesses are scheduled for the next cycle and write hold is set to 1 or greater, then CE stays active for 3 cycles after the value of the programmed hold period. If write hold is cleared to 0, then CE stays active for four more cycles. This does not affect performance and merely reflects the EMIF's overhead.
- For the C621x/C671x EMIF and C64x EMIF: The CEn signal goes high immediately after the programmed hold period.

Figure 1-10. Asynchronous Write Timing Diagram



A Clock = CLKOUT1 for C620x/C670x DSP.
= ECLKOUT for C621x/C671x DSP.
= ECLKOUT1 for C64x DSP.

B CE waveform for C620x/C670x DSP.

C CE waveform for C621x/C671x DSP and C64x DSP.

D For C621x/C671x EMIF, ED may become valid one cycle later (see Section 1.5.3.1).

1.5.3.1 C621x/C671x Asynchronous Writes Setup Timing

For a C621x/C671x asynchronous write cycle, the address (EA) and strobe ($\overline{CE}$ and $\overline{BE}$) signals have setup time of WRSETUP cycles as programmed in the EMIF CE space control register (CECTL). However, the data lines (ED) may become valid one cycle later than the address (EA) and strobe ($\overline{CE}$ and $\overline{BE}$) signals. In other words, the setup period of the ED may be one cycle less than the programmed value in the WRSETUP field of CECTL. The exact ED setup timing depends on the access width and EMIF bus width as follows:

- Access Size <= EMIF Bus Width

  For an EMIF access size less than or equal to the EMIF bus width, **every** asynchronous write has a data line (ED) setup of one less than the programmed value in the WRSETUP field of CECTL. For example, for every 32-bit access (CPU instruction STW) on a 32-bit wide EMIF, the ED setup is one cycle less than the value programmed in the WRSETUP field, while the $\overline{CE}$, $\overline{BE}$, and EA setup are the value as programmed in the WRSETUP field.
- Access size > EMIF Bus Width

  For an EMIF access size greater than the EMIF bus width, the first write has an ED setup of one cycle less than the programmed value in the WRSETUP field of CECTL. Remaining writes for the same write command have an ED setup matching the WRSETUP field. The $\overline{CE}$, $\overline{BE}$, and EA setup are also exactly as programmed in the WRSETUP field. For example, for every 32-bit access (CPU instruction STW) on an 8-bit wide EMIF, the ED setup for the first byte is one cycle less than the value programmed in the WRSETUP field, but the ED setup for the remaining three bytes is exactly as programmed in the WRSETUP field.

Therefore, you should properly configure the WRSETUP field in CECTL to ensure sufficient ED setup time. For example, if ED setup requires 3 cycles, the WRSETUP field should be programmed to 4.

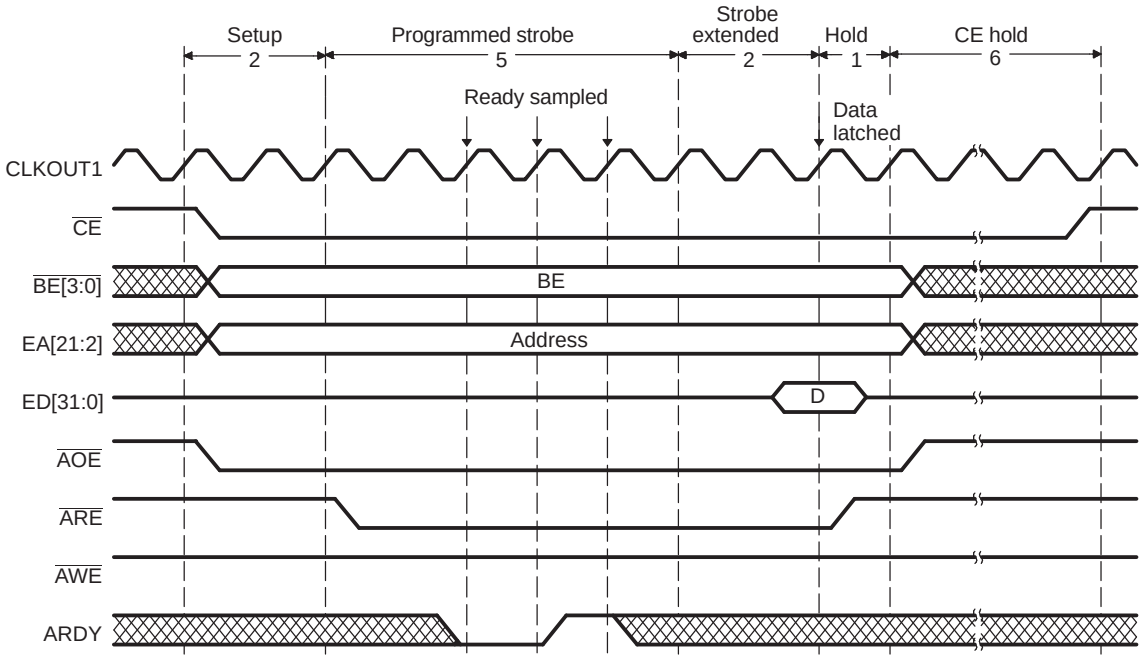
1.5.4 Ready Input

In addition to programmable access shaping, you can insert extra cycles into the strobe period by deactivating the ARDY input. The ready input is internally synchronized to the CPU clock (C620x/C670x EMIF), ECLKOUT (C621x/C671x EMIF), or ECLKOUT1 (C64x EMIF). This synchronization allows an asynchronous ARDY input while avoiding metastablility.

1.5.4.1 C620x/C670x EMIF

If ARDY is low on the third rising edge of CLKOUT1 before the end of the programmed strobe period, then the strobe period is extended by one CLKOUT1 cycle. For each subsequent CLKOUT1 rising edge that ARDY is sampled low, the strobe period is extended by one CLKOUT1 cycle. Thus, to effectively use CE to generate ARDY inactive with external logic, the minimum value of SETUP and STROBE should be 4. Figure 1-11 shows the read cycle for a ready operation.

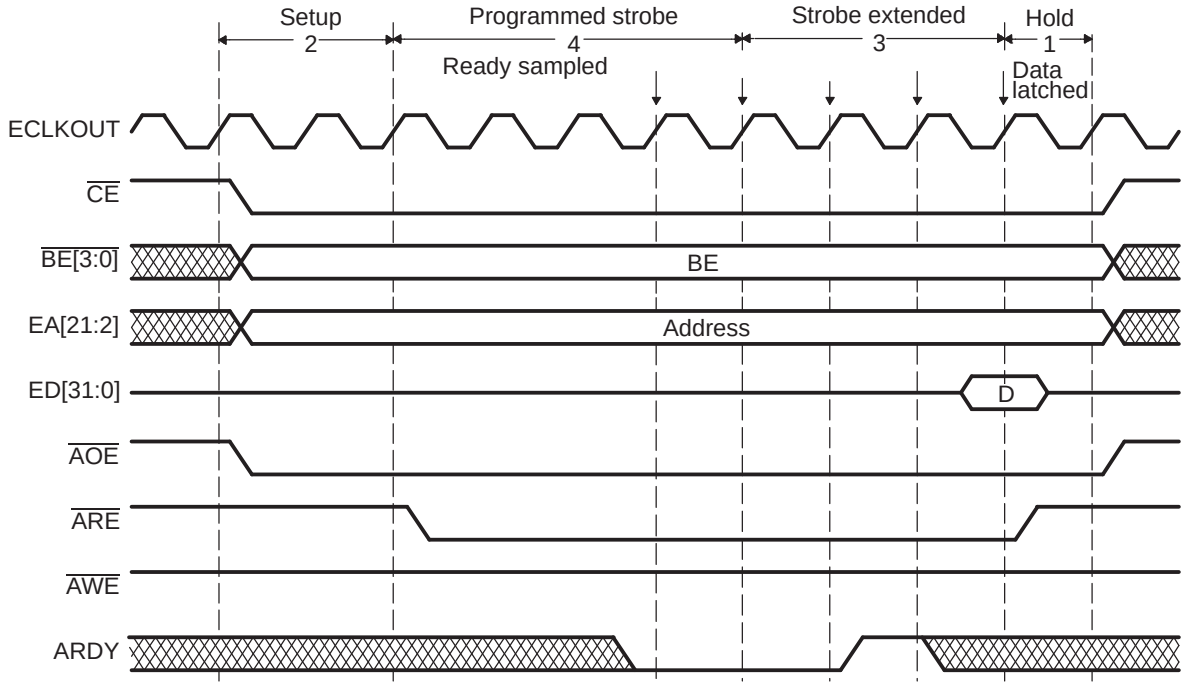
Figure 1-11. TMS320C620x/C670x EMIF Ready Operation Timing Diagram



1.5.4.2 C621x/C671x EMIF

If ARDY is low on the first rising edge of ECLKOUT before the end of the programmed strobe period (see Figure 1-12), then the strobe period is extended by one ECLKOUT cycle. For each subsequent ECLKOUT rising edge that ARDY is sampled low, the strobe period is extended by one ECLKOUT cycle. Thus, to effectively use CE to generate ARDY inactive with external logic the minimum of SETUP and STROBE should be 2.

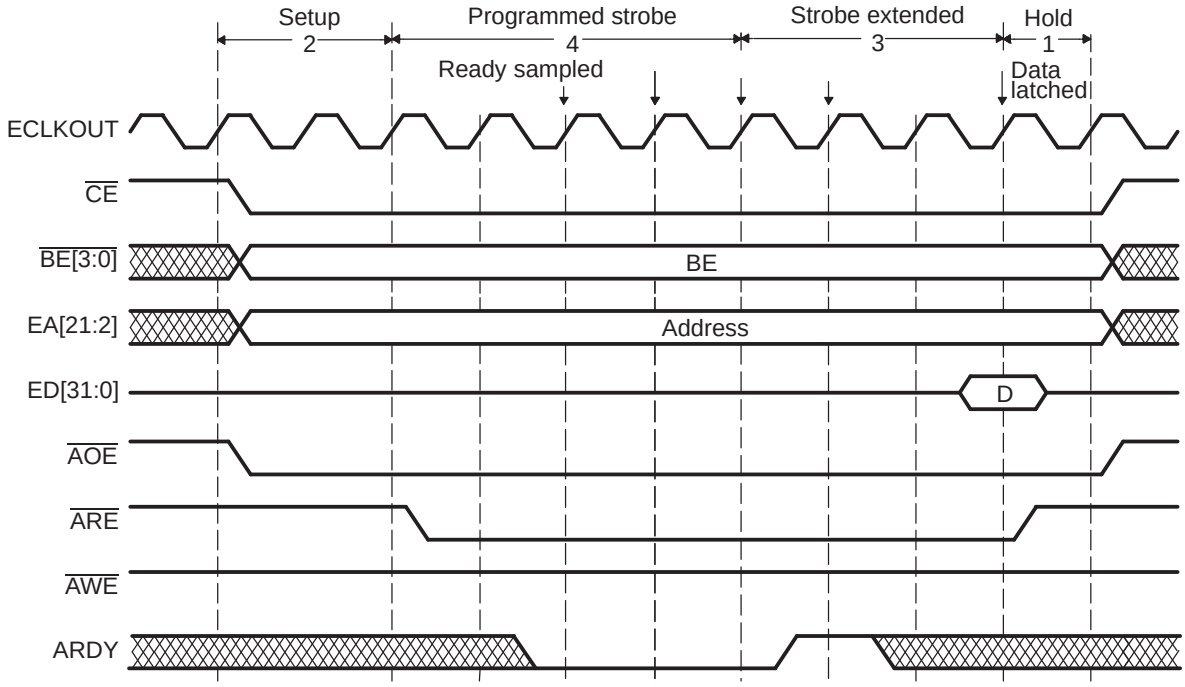
Figure 1-12. TMS320C621x/C671x EMIF Ready Operation Timing Diagram



1.5.4.3 C64x EMIF

If ARDY is low on the second rising edge of ECLKOUT before the end of the programmed strobe period (see Figure 1-13), then the strobe period is extended by one ECLKOUT cycle. For each subsequent ECLKOUT rising edge that ARDY is sampled low, the strobe period is extended by one ECLKOUT cycle. Thus, to effectively use CE to generate ARDY inactive with external logic the minimum of SETUP and STROBE should be 3.

Figure 1-13. TMS320C64x EMIF Ready Operation Timing Diagram



1.5.5 C620x/C670x DSP Illegal Access to Asynchronous Memory

An access to a section of memory that does not return a ready indication is not allowed. This includes accesses to EMIF asynchronous spaces with ARDY pulled inactive externally or left floating on the device. Possible requestors are: CPU program fetches, CPU loads and stores, programmed DMA channels or HPI/PCI/XBUS host mastering of the DMA through the auxiliary DMA. This type of access can create a stall indefinitely.

1.6 Resetting the EMIF

A hardware reset using the $\overline{\text{RESET}}$ pin on the device forces all register values to their reset state. During reset, all outputs are driven to their inactive levels, with the exception of the clock outputs (SDCLK, SSCLK, CLKOUT1, and CLKOUT2). Refer to the device-specific datasheet for the behavior of the clock outputs during active $\overline{\text{RESET}}$.

1.6.1 Valid EMIF Clock During Reset

The EMIF (EMIFA on C64x DSP) has a usage condition that can affect the functionality of CLKOUT*n*. The EMIF global control register (GBLCTL) controls the logic that outputs the internal CPU/x clocks to the CLKOUT*n* pins. The bits in GBLCTL that enable CLKOUT*n* are clocked with the boot-time selected EMIF clock. Without the selection of a valid EMIF clock, ECLKIN (AECLKIN on C64x DSP) or an internal clock, it is possible to have unknown values in GLBCTL and, therefore, a nonfunctional CLKOUT*n*. This happens only when ECLKIN is selected at boot time, but no external clock is provided. Furthermore, without a valid EMIF clock, the EMIF registers are not accessible or assured to have their default values. To avoid a nonfunctional CLKOUT*n*, a valid clock must be provided to the EMIF during the entire RESET active pulse.

1.7 Hold Interface

The EMIF responds to hold requests for the external bus. The hold handshake allows an external device and the EMIF to share the external bus. The handshake mechanism uses:

- $\overline{\text{HOLD}}$: hold request input. $\overline{\text{HOLD}}$ synchronizes internally to the CPU clock. This synchronization allows an asynchronous input, while avoiding metastability. The external device drives this pin low to request bus access. $\overline{\text{HOLD}}$ is the highest priority request that the EMIF can receive during active operation. When the hold is requested, the EMIF stops driving the bus at the earliest possible moment, which may entail completion of the current accesses, device deactivation, and SDRAM bank deactivation. The external device must continue to drive $\overline{\text{HOLD}}$ low for as long as it wants to drive the bus. The external device may deassert $\overline{\text{HOLD}}$ after $\overline{\text{HOLDA}}$ is asserted and the bus is no longer needed. Any memory spaces configured for SDRAM are deactivated and refreshed after the external master releases $\overline{\text{HOLD}}$.
- $\overline{\text{HOLDA}}$: Hold acknowledge output. The EMIF asserts this signal active after it has placed its signal outputs in the high-impedance state. The external device can then drive the bus as required. The EMIF places all outputs in the high-impedance state with the exception of BUSREQ, $\overline{\text{HOLDA}}$, and the clock outputs (CLKOUT1, CLKOUT2, ECLKOUT, SDCLK, and/or SSCLK, depending on the device). For the C64x EMIF, the EK*n*HZ bits in GBLCTL determine the state of the ECLKOUT*n* signals while $\overline{\text{HOLDA}}$ is asserted. Glitches may appear on the ECLKOUT*n* signals when they transition from being driven to being placed in the high-impedance state, and conversely. If any memory spaces are configured for SDRAM, these memory spaces are deactivated before $\overline{\text{HOLDA}}$ is asserted to the external master.
- BUSREQ. Bus request output (C621x/C671x/C64x DSP only). The EMIF asserts this signal active when any request is either pending to the EMIF or is in progress. The BUSREQ signal is driven without regard to the state of the $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ signals or the type of access pending. An external master can use this signal to release control of the bus if desired and it may be ignored in some systems. The BUSREQ signal may also go active when the SDRAM timer count reaches zero, if SDRAM refresh is enabled (RFEN = 1). For C64x EMIF, the BRMODE bit in GBLCTL indicates the bus request mode (see register sections in device documents).

Note: There is no mechanism to ensure that the external device does not attempt to drive the bus indefinitely. You should be aware of system-level issues, such as refresh, that you may need to perform.

During host requests, the refresh counters within the EMIF continue to log refresh requests; however, no refresh cycles can be performed until bus control is again granted to the EMIF when the $\overline{\text{HOLD}}$ input returns to the inactive level. You can prevent an external hold by setting the NOHOLD bit in GBLCTL.

1.7.1 TMS320C62x/C67x EMIF Reset Considerations With the Hold Interface

For the C62x/C67x EMIF, if a hold request is pending ($\overline{\text{HOLD}}$ low) upon exiting reset, the EMIF outputs are driven for a brief period of time (less than 5 CLKOUT2/ECLKOUT cycles) in the default state. That is, active-low output strobes are high and address outputs are driven low. If other memory controller devices are connected on the bus, there is a potential for data contention if the outputs are driven at opposite states during this short amount of time. If multiple C62x/C67x devices are connected on the same bus and come out of reset simultaneously, then the brief period of time that the output buffers are all driven will not result in device damage, since the outputs are all driven to the same logic level.

1.7.2 TMS320C64x EMIF Reset Considerations With the Hold Interface

For the C64x EMIF, if a hold request is pending upon exiting reset, none of the EMIF output signals are driven active. All output signals stay in a high-impedance state. The $\overline{\text{HOLDA}}$ signal is asserted immediately.

1.8 Boundary Conditions When Accessing EMIF Registers

The C6000 EMIF has internal registers that change memory type, asynchronous memory timing, SDRAM refresh, SDRAM initialization (MRS COMMAND), clock speed, arbitration type, HOLD/NOHOLD condition, etc.

The following actions can cause improper data reads or writes:

- Writing to the CE0, CE1, CE2, or CE3 space control registers while an external access to that CE space is active.
- Changing the memory type (MTYPE) in the CE space control register (CECTL) while any external operation is in progress (SDRAM type while SDRAM initialization is active).
- Changing the state of NOHOLD in the configuration while HOLD is active at the pin.
- Changing the RBTR8 bit in the EMIF global control register (GBLCTL) while multiple EMIF requests are pending (C620x/C670x EMIF only).
- Initiating an SDRAM INIT (MRS) while the $\overline{\text{HOLD}}$ input or the $\overline{\text{HOLDA}}$ output is active.
  - The EMIF global control register (GBLCTL) can be read before the INIT bit is set to determine if the HOLD function is active. GBLCTL must be read immediately after the INIT bit is written to make sure that the two events did not occur simultaneously.
  - GBLCTL has status on the HOLD/HOLDA, DMC/PMC/DMA active access and false access detection.
- Reading or writing registers if the EMIF is unclocked (if EMIF is configured to be clocked externally and no clock is provided).
  - Attempting to do so will lock up the device.
  - Some tools will attempt to access these registers automatically or as part of a script to provide default memory configurations. This must be disabled to prevent locking up the device.

1.9 Clock Output Enabling

To reduce electromagnetic interference (EMI) radiation, the C62x/C67x EMIF allows the disabling (holding high) of CLKOUT2, CLKOUT1 (all C62x/C67x devices, except C6713 DSP), SSCLK, and SDCLK. This disabling is performed by clearing the CLK2EN, CLK1EN, SSCEN, and SDCEN bits to 0 in the EMIF global control register (GBLCTL). ECLKOUT on the C6713 DSP can also be disabled (held low) by clearing the EKEN bit to 0 in GBLCTL.

For the C64x EMIF, the CLKOUT*n* and ECLKOUT*n* can be disabled by setting the appropriate bits (CLK4EN, CLK6EN, EK1EN, EK2EN) in GBLCTL. The ECLKOUT2 can be configured to run at 1 1/2 or 1/4ıthe ECLKIN rate for the generic synchronous interface. ECLKOUT2 rate should only be changed once during EMIF initialization from the default (1/4ש to either 1/2ıor 1 In addition, the EK1HZ and EK2HZ bits in GBLCTL configure the output EMIF clock behavior during hold. The reset controller controls the output buffer of ECLKOUT1, ensuring that ECLKOUT1 is in a high-impedance state during device reset, see Figure 1-14. Table 1-11 summarizes the function of the EK*n*EN and EK*n*HZ bits.

ECLKOUT*n* does not turn off/on glitch free when it is disabled by setting the EK*n*EN or EK*n*HZ bits in the global control register. Therefore, ECLKOUT:

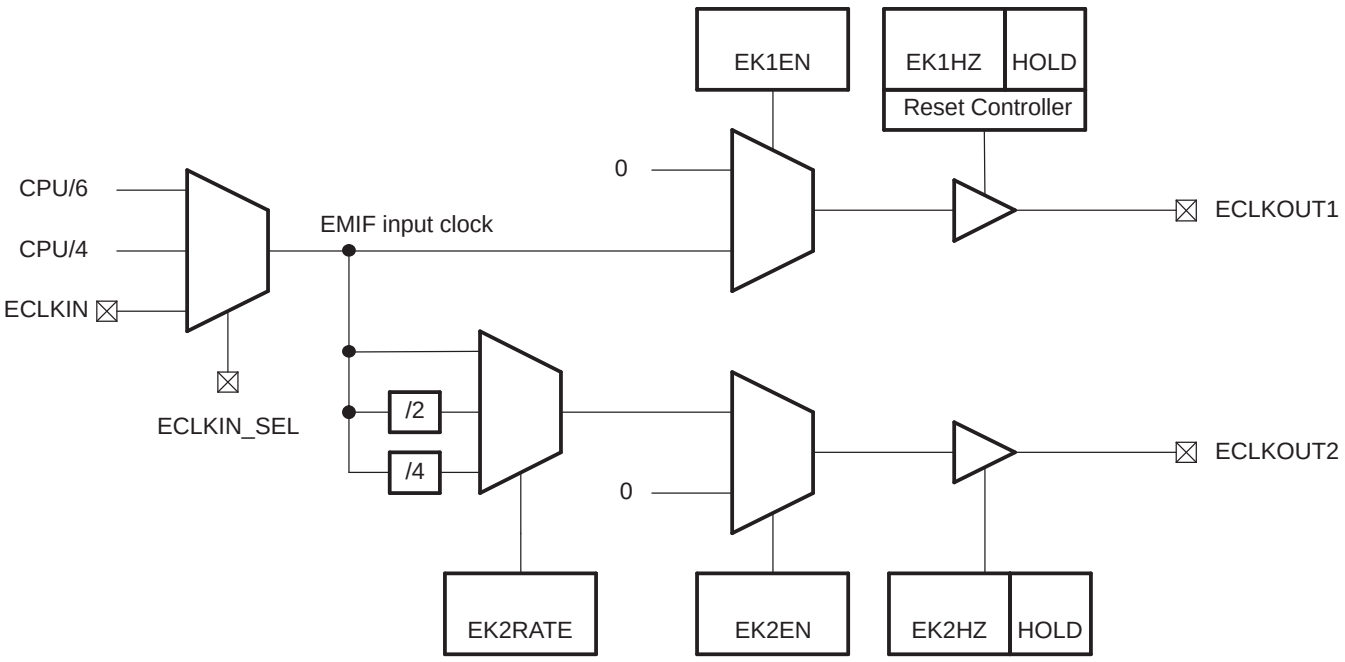
- Should not be disabled/enabled when connected to devices that have a strict requirement for glitch free disable/enable or external logic should be implemented to provide glitch free disable/enable.
- Should only be disabled if unused.

On the C64x EMIF, the CLKOUT4 and CLKOUT6 pins are MUXed with the general-purpose input/output (GPIO) pins GP1 and GP2, respectively. When these pins are configured as GPIO pins by setting the GPIO enable register (GPEN), the corresponding CLK*n*EN bits in GBLCTL are ignored.

Table 1-11. EMIF Output Clock (ECLKOUTn) Operation

EK*n*EN	EK*n*HZ	ECLKOUT*n* Behavior
0	0	ECLKOUT*n* remains low.
0	1	ECLKOUT*n* is low, except during Hold. In high-impedance state during Hold.
1	0	ECLKOUT*n* is clocking.
1	1	ECLKOUT*n* is clocking, except during Hold. In high-impedance state during Hold.

Figure 1-14. TMS320C64x EMIF Clock Block Diagram



1.10 Emulation Halt Operation

The EMIF continues operating during emulation halts. Emulator accesses through the EMIF can work differently than the way the actual device works during EMIF accesses. This discrepancy can cause start-up penalties after a halt operation.

1.11 Power Down

In power-down 2 mode, refresh is enabled. SSCLK, CLKOUT1, and CLKOUT2 are held low during power-down 2 and power-down 3 modes. In power-down 3 mode, the EMIF acts as if it were in reset.

For the C621x/C671x EMIF and C64x EMIF, refreshes are only issued to SDRAM if ECLKIN or SYSCLK3 (C6713 device only) is provided.

TMS320C620x/C670x EMIF

This chapter describes the operation and registers of the EMIF in the TMS320C620x/C670x DSP. For operation and registers unique to the TMS320C621x/C671x EMIF, see Chapter 3. For operation and registers unique to the TMS320C64x™ EMIF, see Chapter 4.

Topic **Page**

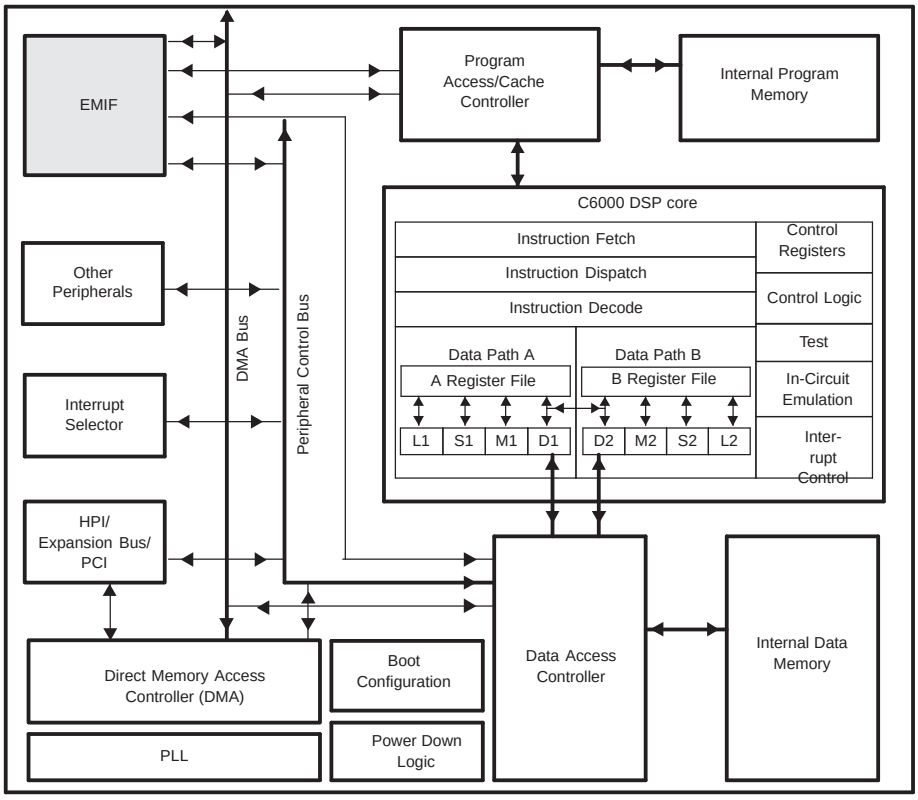
2.1 Overview

The C620x/C670x EMIF services requests of the external bus from four requestors:

- On-chip program memory controller that services CPU program fetches
- On-chip data memory controller that services CPU data fetches
- On-chip direct-memory access (DMA) controller
- External shared-memory device controller (using EMIF arbitration signals)

If multiple requests arrive simultaneously, the EMIF prioritizes them and performs the necessary number of operations. A block diagram of the C620x/C670x DSP is shown in Figure 2-1. The C620x/C670x EMIF has a 32-bit data bus interface.

Figure 2-1. TMS320C620x/C670x DSP Block Diagram



(1) Not all peripherals exist on all C620x/C670x devices. Refer to the device-specific datasheet for the peripheral set.

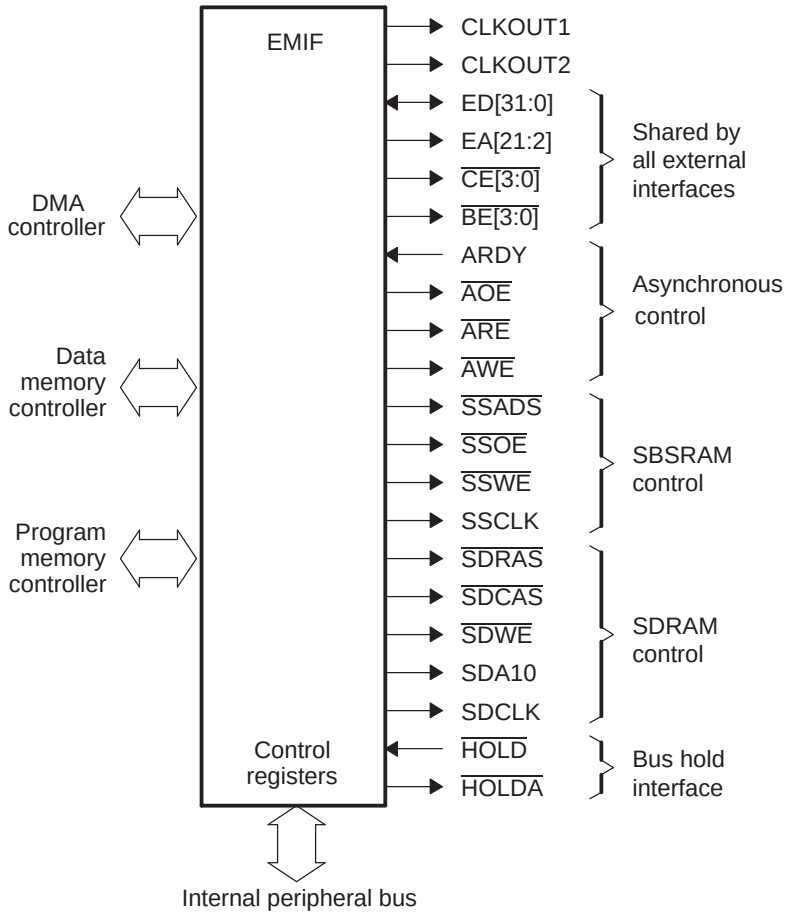
2.2 EMIF Interface Signals

The following describes the EMIF interface signals on the C620x/C670x devices.

2.2.1 C6201/C6701 EMIF

The EMIF signals of the C6201/C6701 DSP are shown in Figure 2-2 and described in Table 2-1. The C6201/C6701 devices provide separate clock and control signals for the SBSRAM and SDRAM interface. The SDRAM runs off SDCLK, while the SBSRAM runs off SSCLK. All three memory types (SDRAM, SBSRAM, and asynchronous devices) can be included in a system. Asynchronous interface is supported on all CE spaces, but CE1 is used for asynchronous interface only.

Figure 2-2. TMS320C6201/C6701 EMIF Interface Signals



2.2.2 C6202(B)/C6203(B)/C6204/C6205 EMIF

The EMIF signals of the C6202/C6203/C6204/C6205 DSP are shown in Figure 2-3 and described in Table 2-1. These C620x devices have combined the SDRAM and SBSRAM signals. Only one of these two memory types can be used in a system. These memories run off CLKOUT2 (EMIF clock cycle), which is equal to half the CPU clock rate.

Asynchronous interface is supported on all CE spaces, but CE1 is used for asynchronous interface only.

Figure 2-3. TMS320C6202/C6203/C6204/C6205 EMIF Interface Signals

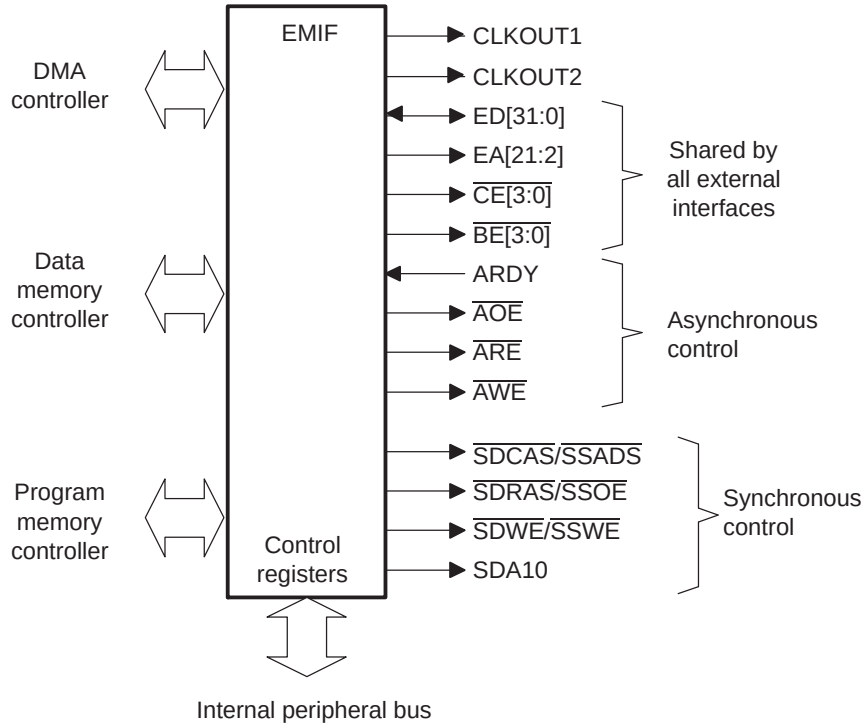


Table 2-1. TMS320C620x/C670x EMIF Interface Signal Descriptions

Pin	I/O/Z	Description
CLKOUT1	O	Clock output. Runs at the CPU clock rate.
CLKOUT2	O	Clock output. Runs at 1/2 the CPU clock rate. Used for synchronous memory interface on all C620x/C670x devices, except C6201/C6701 DSP.
ED[31:0]	I/O/Z	EMIF 32-bit data bus I/O.
EA[21:2]	O/Z	External address output. Drives bits 21-2 of the byte address. (Effectively a word address.)
$\overline{CE0}$	O/Z	Active-low chip select for memory space CE0.
$\overline{CE1}$	O/Z	Active-low chip select for memory space CE1.
$\overline{CE2}$	O/Z	Active-low chip select for memory space CE2.
$\overline{CE3}$	O/Z	Active-low chip select for memory space CE3.
$\overline{BE[3:0]}$	O/Z	Active-low byte enables. Individual bytes and halfwords can be selected for write cycles. For read cycles, all four byte-enables are active.
ARDY	I	Ready. Active-high asynchronous ready input used to insert wait states for slow memories and peripherals.
$\overline{AOE}$	O/Z	Active-low output enable for asynchronous memory interface.
$\overline{ARE}$	O/Z	Active-low read strobe for asynchronous memory interface.
$\overline{AWE}$	O/Z	Active-low write strobe for asynchronous memory interface.
$\overline{SSADS}$	O/Z	Active-low address strobe/enable for SBSRAM interface.
$\overline{SSOE}$	O/Z	Active low output buffer enable for SBSRAM interface.
$\overline{SSWE}$	O/Z	Active-low write enable for SBSRAM interface.
SSCLK	O/Z	SBSRAM interface clock. Programmable to either the CPU clock rate or half of the CPU clock rate. (C6201/C6701 DSP only)
$\overline{SDRAS}$	O/Z	Active-low row address strobe for SDRAM memory interface.
$\overline{SDCAS}$	O/Z	Active-low column address strobe for SDRAM memory interface.
$\overline{SDWE}$	O/Z	Active-low write enable for SDRAM memory interface.
SDA10	O/Z	SDRAM A10 address line. Address line/autoprecharge disable for SDRAM memory.
SDCLK	O/Z	SDRAM interface clock. Runs at 1/2 the CPU clock rate. Equivalent to CLKOUT2. (C6201/C6701 DSP only)
$\overline{HOLD}$	I	Active-low external bus hold (3-state) request.
$\overline{HOLDA}$	O	Active-low external bus hold acknowledge.

2.3 Memory Width and Byte Alignment

The C620x/C670x EMIF supports 32-bit-wide ASRAM, SDRAM, and SBSRAM interface in both big-endian and little-endian modes. CE1 space supports ×16 and ×8 read-only memory (ROM) interfaces. The packing format in ROM is always little-endian, regardless of the value of the LENDIAN configuration bit. Table 2-2 summarizes the addressable memory ranges on the C620x/C670x device.

Table 2-2. Addressable Memory Ranges

Memory type	Memory width	Maximum addressable bytes per CE space	Address output on EA[21:2]	Represents
ASRAM	×32	4M	A[21:2]	Word address
SBSRAM	×32	4M	A[21:2]	Word address
SDRAM	×32	16M	See Section 2.4	Word address

2.4 SDRAM Interface

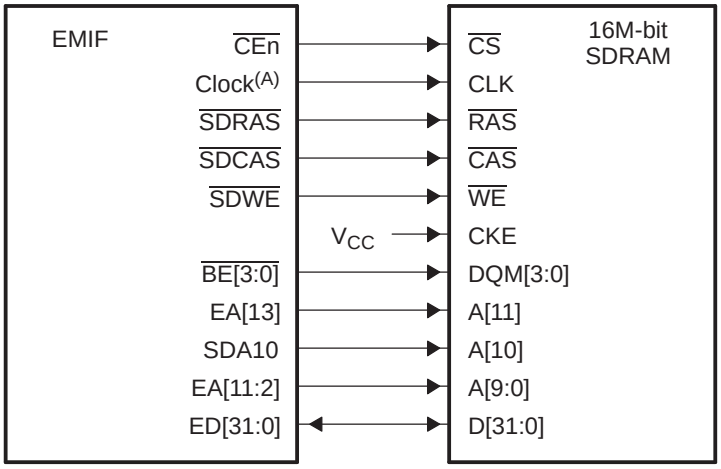
The C620x/C670x EMIF supports SDRAM commands shown in Table 1-2, and Table 1-3 shows the signal truth table for the SDRAM commands. Table 1-4 summarizes the pin connection and related signals specific to SDRAM operation. Table 1-5 summarizes the similarities and differences on the C6000 SDRAM interface.

The 16M-bit SDRAM interface is shown in Figure 2-4 and the 64M-bit SDRAM interface is shown in Figure 2-5.

The C620x/C670x EMIF allows programming of the SDRAM column size to be 8 or 9 address bits. The number of row address bits and bank bits are not user-programmable. Once the number of column address bits is programmed, the number of address bits (EA pins) used during the $\overline{RAS}$ command is fixed. If the column size is set to 8 address bits, the total number of row and bank bits is 14 bits. If the column size is set to 9 address bits, the total number of row and bank bits is 13 bits. See details in Section 2.4.3 and Table 2-5.

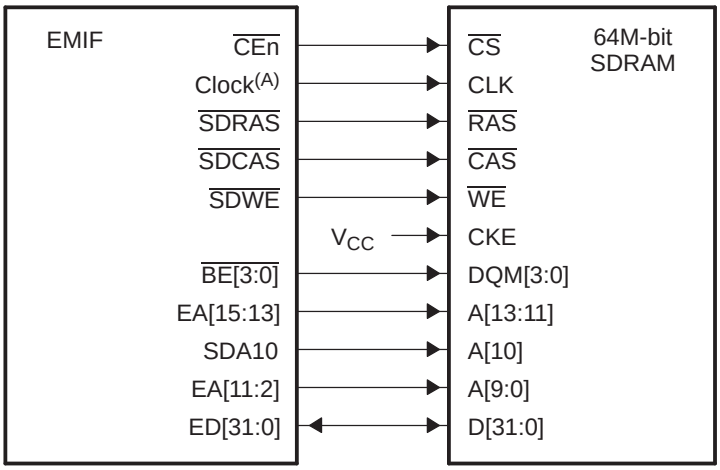
Table 2-3 lists some common SDRAM configurations that can interface to the C620x/C670x DSP directly. The number of column, row, and bank bits supported by the C620x/C670x EMIF limits the maximum addressable space to 16M bytes. Therefore, if larger memories are interfaced directly to the C620x/C670x EMIF, not all the memory space is accessible. Table 2-4 provides examples of possible SDRAM interface to larger memories where only part of the larger memories is accessible.

Figure 2-4. EMIF to 16M-Bit SDRAM Interface Block Diagram



A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all other C620x/C670x DSP.

Figure 2-5. EMIF to 64M-Bit SDRAM Interface Block Diagram



A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all other C620x/C670x DSP.

Table 2-3. TMS320C620x/C670x DSP Compatible SDRAM

SDRAM Size	B	W	D	Max Devices/ CE	Addressable Space (MBytes)		Column Address	Row Address	Bank Select	Pre-charge
16M bit	2	×8	1M	4	8M	SDRAM	A8-A0	A10-A0	BA0	A10
						EMIF	EA10-EA2	SDA10, EA11-EA2	EA13	SDA10
	2	×16	512K	2	4M	SDRAM	A7-A0	A10-A0	BA0	A10
						EMIF	EA9-EA2	SDA10, EA11-EA2	EA13	SDA10
64M bit	4	×16	1M	2	16M	SDRAM	A7-A0	A11-A0	BA1-BA0	A10
						EMIF	EA9-EA2	EA13, SDA10, EA11-EA2	EA15-EA14	SDA10
	4	×32	512K	1	8M	SDRAM	A7-A0	A10-A0	BA1-BA0	A10
						EMIF	EA9-EA2	SDA10, EA11-EA2	EA14-EA13	SDA10
128M bit	4	×32	1M	1	16M	SDRAM	A7-A0	A11-A0	BA1-BA0	A10
						EMIF	EA9-EA2	EA13, SDA10, EA11-EA2	EA15-EA14	SDA10

B = Banks; W = Width; D = Depth

Table 2-4. Example C620x/C670x SDRAM Interface with Unused SDRAM Address Pins

SDRAM Size	B	W	D	Max Devices/ CE	Addressable Space (MBytes)		Column Address	Row Address	Bank Select	Pre-charge
128M bit	4	×16	2M	2	16M (2)	SDRAM	A8-A0	A11-A0 (3)	BA1-BA0	A10
						EMIF	EA10-EA2	SDA10, EA11-EA2	EA14-EA13	SDA10
256M bit	4	×16	4M	2	16M (2)	SDRAM	A8-A0	A12-A0 (3)	BA1-BA0	A10
						EMIF	EA10-EA2	SDA10, EA11-EA2	EA14-EA13	SDA10
512M bit	4	×16	8M	2	16M (2)	SDRAM	A9-A0 (4)	A12-A0 (3)	BA1-BA0	A10
						EMIF	EA10-EA2	SDA10, EA11-EA2	EA14-EA13	SDA10

(1) B = Banks; W = Width; D = Depth

(2) Due to column and row address size limitations, not all of the memory space in the larger memories is used. The actual usable address space is shown.

(3) The number of available EMIF row address pins is less than the number of row address pins required by the SDRAM interface.

(4) The number of available EMIF column address pins is less than the number of column address pins required by the SDRAM interface.

2.4.1 C620x/C670x Bootmode

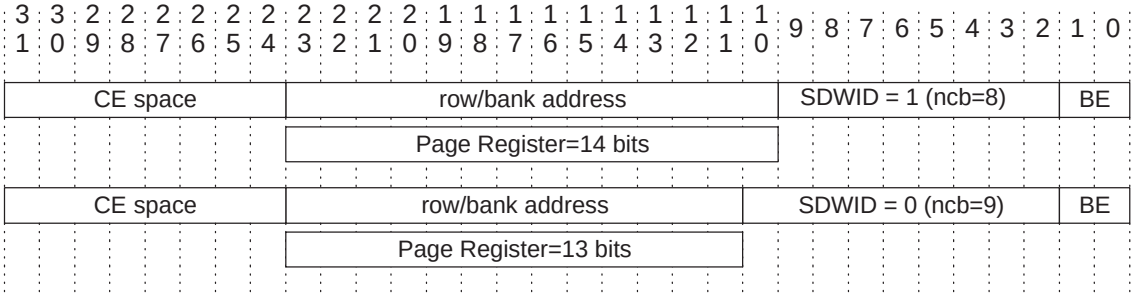
If BOOTMODE[4:0] bits are set such that CE0 is configured for SDRAM, SDRAM initialization proceeds according to the steps listed in Section 1.3.1 under the control of hardware, prior to the boot process. However, if $\overline{\text{HOLD}}$ is active, the DCAB command is not performed until the hold condition is removed. In this case, the external requester should not attempt to access any SDRAM banks, unless it performs SDRAM initialization and control. If other CE spaces besides CE0 are configured for SDRAM, and since CE0 is initialized with slower default timings following reset, SDRAM initialization should be performed by software.

2.4.2 Monitoring Page Boundaries

The C620x/C670x EMIF storage and comparison is performed independently for each CE space. The C620x/C670x EMIF has 4 internal page registers. Each page register corresponds to a single CE space. If a given CE space is configured for SDRAM operation (by the MTYPE field in CECTL), the corresponding page register is used for accesses to that CE space. If the CE space is not configured for SDRAM operation, the corresponding page register is not used. Therefore, the C620x/C670x devices can support a single open page per CE space.

Address bits are compared during an SDRAM access to determine whether the page is open. The number of address bits compared is a function of the page size programmed in the SDWID field of the SDRAM control register (SDCTL). If SDWID = 0, the EMIF expects CE spaces configured as SDRAM to have a page size of 512 elements (that is, number of column address bits = NCB = 9). Thus, the logical byte address bits compared are 23-11. Logical addresses with the same bits 23-11 belong to the same page. If SDWID = 1, the EMIF expects CE spaces with SDRAM to have a page size of 256 elements (NCB = 8). Thus, the logical byte address bits compared are 23-10. The logical address bits 25 and 24 (and above) determine the CE space. If a page boundary is crossed during an access to the same CE space, the EMIF performs a DCAB command and starts a new row access. Figure 2-6 details how a 32-bit logical address maps to the page register.

Figure 2-6. Logical Address-to-Page Register Mapping



(1) ncb = number of column address bits

2.4.3 Address Shift

The same EMIF pins determine the row and column address, thus the C620x/C670x EMIF interface appropriately shifts the address in row and column address selection. Table 2-5 shows the translation between bits of the byte address and how they appear on the EA pins for row and column addresses on the C620x/C670x DSP. SDRAMs use the address inputs for control and address.

The following factors apply to the address shifting process:

- The address shift is controlled completely by the SDWID field, which is programmed according to the column size of the SDRAM.
- The upper address bits (EA[14:11] when SDWID = 0, or EA[15:10] when SDWID = 1) are latched internally by the SDRAM controller during a RAS cycle. This ensures that the SDRAM bank select inputs are correct during READ and WRT commands. Thus, the EMIF maintains these values as shown in both row and column addresses.
- The EMIF forces SDA10 to be low during READ or WRT commands. This prevents autoprecharge from occurring following a READ or WRT command.

Table 2-5. Byte Address-to-EA Mapping for SDRAM $\overline{RAS}$ and $\overline{CAS}$

# of column address bits	Interface bus width[1]	DRAM Cmd[2]	E A [21:17]	EA 16	EA 15	EA 14	EA 13	SDA 10	EA 11	EA 10	EA9	EA8	EA7	EA6	EA5	EA4	EA3	EA2
					A 13	A 12	A 11	A 10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8 (SDWID = 1)	32	$\overline{RAS}$		(3)	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$	(3)	(3)	23[4]	22[4]	21[4]	L	19[4]	18[4]	9	8	7	6	5	4	3	2
9 (SDWID = 0)	32	$\overline{RAS}$	(3)	(3)		23	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$	(3)	(3)		23[4]	22[4]	L	20[4]	10	9	8	7	6	5	4	3	2

[1] The C620x/C670x EMIF only supports a 32-bit interface bus width

[2] The $\overline{RAS}$ and $\overline{CAS}$ values indicate the bit of the byte address present on the corresponding EA pin during a $\overline{RAS}$ or $\overline{CAS}$ cycle.

[3] L = Low; SDA10 is driven low during READ or WRT commands to disable autoprecharge.

[4] Bit is internally latched during an ACTV command.

[5] Reserved for future use. Undefined.

2.4.4 SDRAM Refresh Mode

The RFEN bit in the SDRAM control register (SDCTL) enables the SDRAM refresh mode of the C620x/C670x EMIF. When RFEN = 0, all EMIF refreshes are disabled, and you must ensure that refreshes are implemented in an external device. When RFEN = 1, the EMIF performs refreshes of SDRAM.

The refresh command (REFR) enables all $\overline{CE}$ signals for all CE spaces selected to use SDRAM (with the MTYPE field of the CE space control register). REFR is automatically preceded by a deactivate (DCAB) command, this ensures that all CE spaces selected with SDRAM are deactivated. Following the DCAB command, the EMIF begins performing trickle refreshes at a rate defined by the PERIOD value in the SDRAM timing register (SDTIM), provided no other SDRAM access is pending.

The SDRAM interface monitors the number of refresh requests posted to it and performs the refreshes. Within the EMIF SDRAM control block, a 2-bit counter monitors the backlog of refresh requests. The counter increments once for each refresh request and decrements once for each refresh cycle performed. The counter saturates at the values of 11b and 00b. At reset, the counter is automatically set to 11b to ensure that several refreshes occur before accesses begin.

The EMIF SDRAM controller prioritizes SDRAM refresh requests with other data access requests posted to it from the EMIF requesters. The following rules apply:

- A counter value of 11b invalidates the page information register, forcing the controller to close the current SDRAM page. The value 11b indicates an urgent refresh condition. Thus, following the DCAB command, the EMIF SDRAM controller performs three REFR commands, thereby decrementing the counter to 00b before proceeding with the remainder of the current access. If SDRAM is present in multiple CE spaces, the DCAB-refresh sequence occurs in all spaces containing SDRAM.
- During idle times on the SDRAM interface(s), if no request is pending from the EMIF, the SDRAM interface performs REFR commands as long as the counter value is nonzero. This feature reduces the likelihood of having to perform urgent refreshes during actual SDRAM accesses. If SDRAM is present in multiple CE spaces, this refresh occurs only if all interfaces are idle with invalid page information.

2.4.5 Mode Register Set (MRS)

The C620x/C670x EMIF automatically performs a deactivate (DCAB) command followed by a mode register set (MRS) command whenever the INIT field in the SDRAM control register (SDCTL) is set. INIT can be set by device reset or by a write. Like DCAB and refresh (REFR) commands, MRS commands are performed to all CE spaces configured as SDRAM through the MTYPE field in CECTL. Following a hold, the external requester should return the SDRAM MRS register's original value before returning control of the bus to the EMIF. Alternatively, you could poll the HOLD and HOLDA bits in the EMIF global control register (GBLCTL) and, upon detecting completion of an external hold, reinitialize the EMIF by writing a 1 to the INIT bit in SDCTL.

The C620x/C670x EMIF always uses a mode register value of 0030h during an MRS command. shows the mapping between mode register bits, EMIF pins, and the mode register value. Table 2-6 shows the JEDEC standard SDRAM configuration values selected by this mode register value. Figure 2-8 shows the timing diagram during execution of the MRS command.

Figure 2-7. Mode Register Value

13	12	11	10	9	8	7
EA15	EA14	EA13	SDA10	EA11	EA10	EA9
Reserved				Write burst length	Reserved	
0000				0	00	

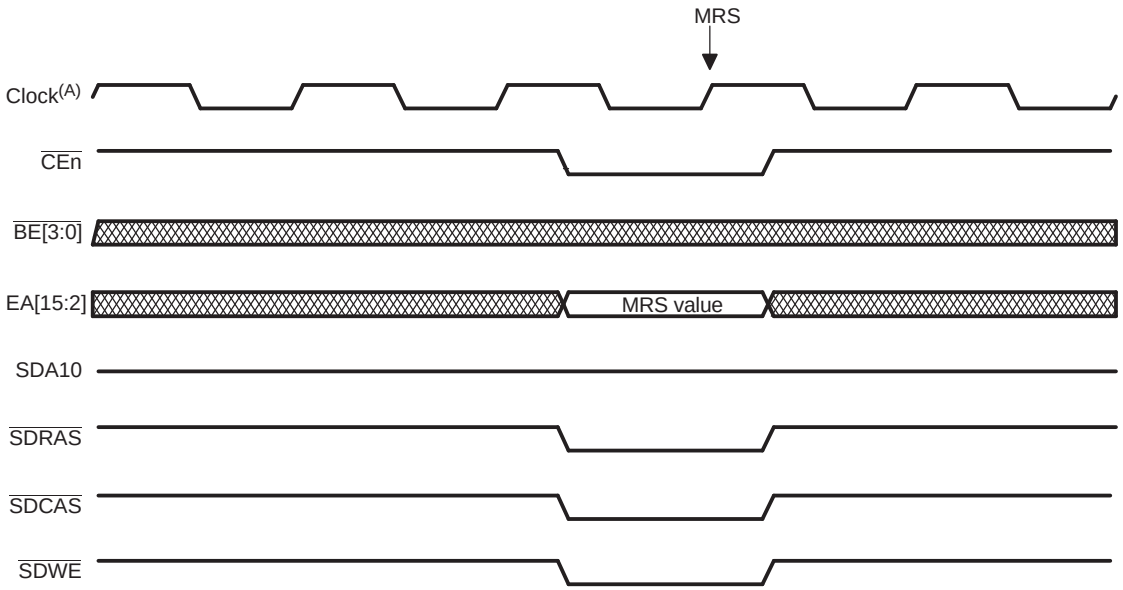
6	5	4	3	2	1	0
EA8	EA7	EA6	EA5	EA4	EA3	EA2
Read latency			S/I	Burst Length		
011			0	000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2-6. Implied SDRAM Configuration by MRS Command

Bit	Field	Selection
9	Write burst length	1 word
6-4	Read latency	3 cycles
3	Serial/interleave burst type	Serial
2-0	Burst length	1 word

Figure 2-8. SDRAM Mode Register Set: MRS Command Timing Diagram



A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.

2.4.6 Timing Requirements

Several SDRAM timing parameters decouple the EMIF from SDRAM speed limitations. For the C620x/C670x EMIF, three of these parameters are programmable using the SDRAM control register (SDCTL); the remaining two parameters are assumed to be static values, as shown in Table 2-7. The three programmable values ensure that EMIF control of SDRAM obeys these minimum timing requirements. Consult the SDRAM data sheet for information on the appropriate parameters for a specific SDRAM.

Table 2-7. SDRAM Timing Parameters

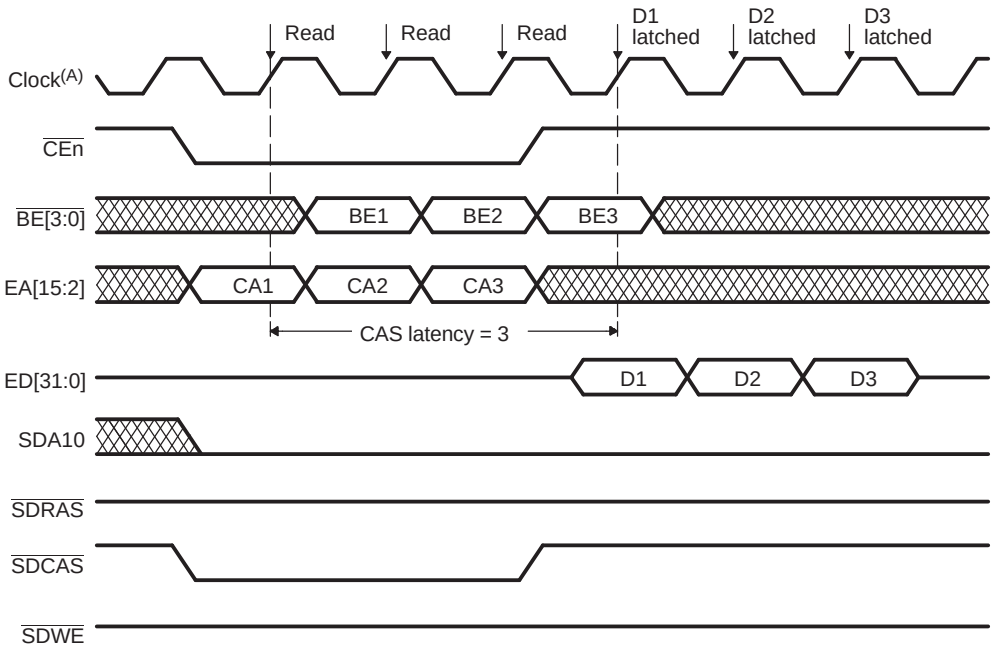
Parameter	Description	Value in EMIF Clock Cycles(1)
t_{RC}	REFR command to ACTV, MRS, or subsequent REFR command	TRC + 1
t_{RCD}	ACTV command to READ or WRT command	TRCD + 1
t_{RP}	DCAB command to ACTV, MRS, or REFR command	TRP + 1
t_{RAS}	ACTV command to DEAC to DCAB command	7
t_{nEP}	Overlap between read data and a DCAB command	2

(1) EMIF clock cycles = CLKOUT2 cycles.

2.4.7 SDRAM Read

During an SDRAM read, the selected bank is activated with the row address during the ACTV command. Figure 2-9 shows the timing for the C620x/C670x EMIF issuing three read commands performed at three different column addresses. The EMIF uses a $\overline{CAS}$ latency of three and a burst length of one. The three-cycle latency causes data to appear three cycles after the corresponding column address. Following the final read command, an idle cycle is inserted to meet timing requirements. If required, the bank is then deactivated with a DCAB command and the EMIF can begin a new page access. If no new access is pending or an access is pending to the same page, the DCAB command is not performed until the page information becomes invalid. The values on EA[15:13] during column accesses and execution of the DCAB command are the values latched during the ACTV command.

Figure 2-9. SDRAM Read Timing Diagram



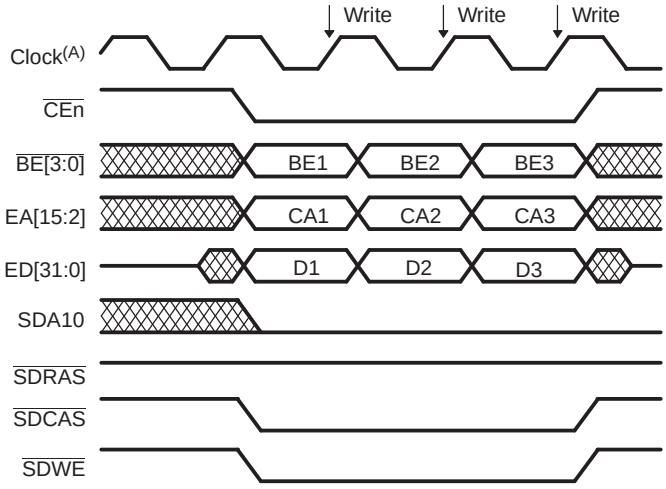
A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.

2.4.8 SDRAM Write

All SDRAM writes have a burst length of one on the C620x/C670x EMIF. The bank is activated with the row address during the ACTV command. There is no latency on writes, so data is output on the same cycle as the column address. Writes to particular bytes are disabled using the appropriate DQM inputs; this feature allows for byte and halfword writes. Figure 2-10 shows the timing for a three-word write on the EMIF. Since the default write-burst length is one word, a new write command is issued each cycle to perform the three-word burst. Following the final write command, the EMIF inserts an idle cycle to meet SDRAM timing requirements. The bank is then deactivated with a DCAB command, and the memory interface can begin a new page access. If no new access is pending, the DCAB command is not performed until the page information becomes invalid (see Section 2.4.2). The values on EA[15:13] (if SDWID = 1) or EA[14:13] (if SDWID = 0) during column accesses and the DCAB command are the values latched during the ACTV command.

If a page boundary is crossed during the course of an access, the EMIF performs a DCAB command and starts a new row access. If a write burst crosses a page boundary, the $\overline{CAS}$ and $\overline{WE}$ signals stay active for one additional cycle before the DCAB command. The $\overline{BE}$ signals are inactive high during this additional cycle to prevent the EMIF from incorrectly writing an extra word.

Figure 2-10. SDRAM Three-Word Write Timing Diagram

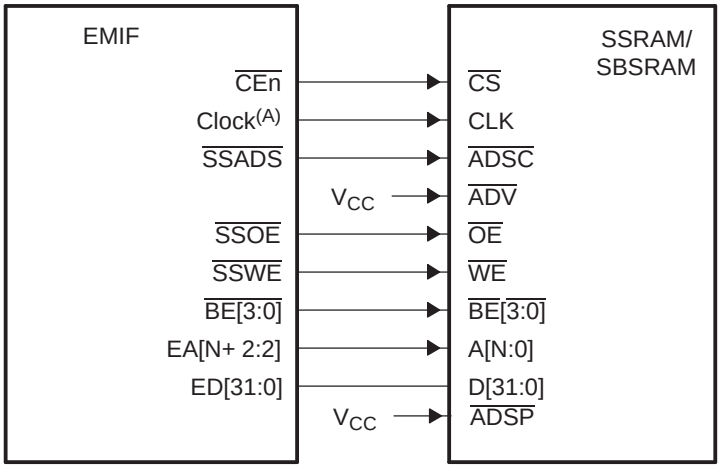


A Clock = SDCLK for C6201/C6701 DSP.
= CLKOUT2 for all other C620x/C670x DSP, except C6201/C6701 DSP.

2.5 SBSRAM Interface

The SBSRAM interface on the C620x/C670x EMIF is shown in Figure 2-11. For the C620x/C670x EMIF, the $\overline{\text{ADV}}$ signal of the SBSRAM is pulled high. This disables the internal burst advance counter of the SBSRAM. This interface allows bursting by strobing a new address into the SBSRAM on every cycle.

Figure 2-11. EMIF to SBSRAM Interface Block Diagram

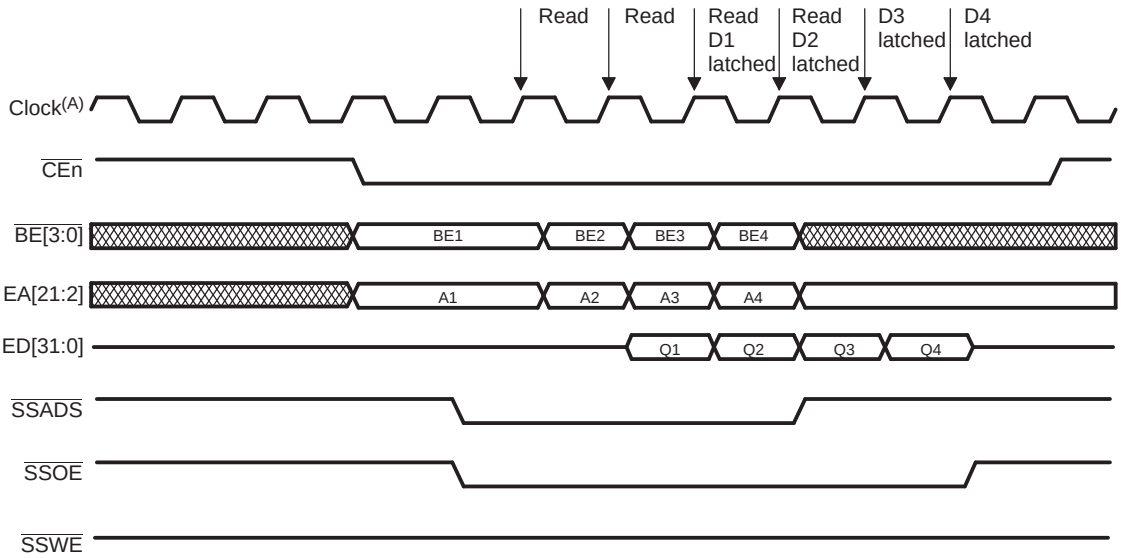


A Clock = SSCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.

2.5.1 SBSRAM Read

Figure 2-12 shows a four-word read of an SBSRAM. Every access strobes a new address into the SBSRAM, indicated by the $\overline{\text{SSADS}}$ strobe low. The first access requires an initial start-up penalty of two cycles; thereafter, all accesses occur in a single EMIF clock cycle.

Figure 2-12. SBSRAM Four-Word Read Timing Diagram

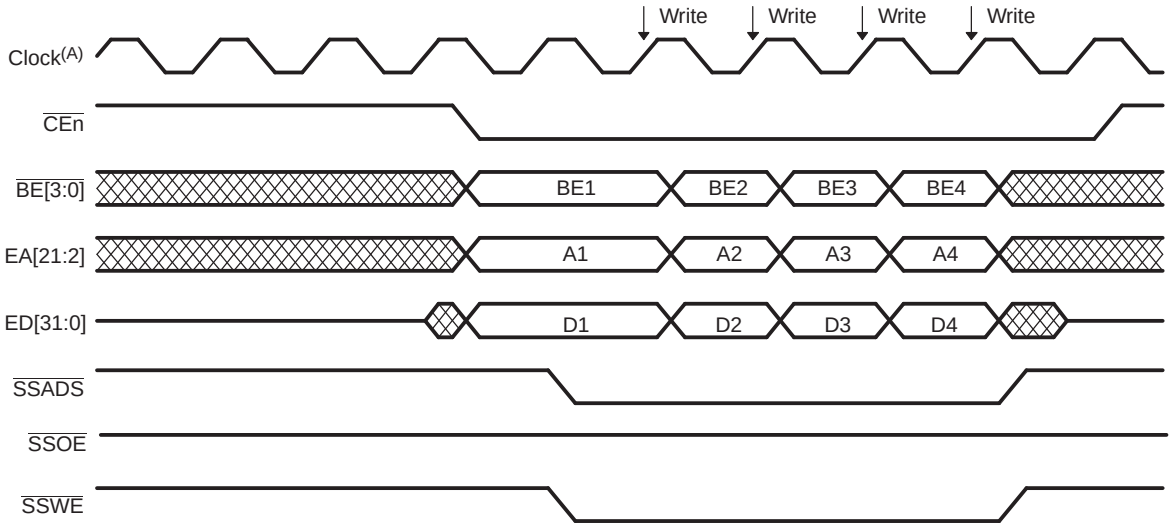


A Clock = SSCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.

2.5.2 SBSRAM Write

Figure 2-13 shows a four-word write to an SBSRAM. Every access strobes a new address into the SBSRAM. The first access requires an initial start-up penalty of two cycles; thereafter, all accesses can occur in a single EMIF clock cycle.

Figure 2-13. SBSRAM Four-Word Write Timing Diagram



A Clock = SSCLK for C6201/C6701 DSP.
= CLKOUT2 for all C620x/C670x DSP, except C6201/C6701 DSP.

2.6 ROM Access Modes

The C620x/C670x EMIF supports 8-bit-wide and 16-bit-wide ROM access modes that are selected by the MTYPE field in the CE space control register (CECTL). In reading data from these narrow memory spaces, the EMIF packs multiple reads into one 32-bit-wide value. This mode is primarily intended for word accesses to 8-bit and 16-bit ROM devices. The following restrictions apply:

- Read operations always read 32 bits, regardless of the access size or the memory width.
- The address is left-shifted appropriately to provide the correct address to the narrow memory. The shift amount is 1 bit for 16-bit ROM or 2 bits for 8-bit ROM. Thus, the high-address bits are shifted out, and accesses wrap around if the CE space spans the entire EA bus. Table 2-8 shows the address bits on the EA bus during an access to CE1 space for all possible asynchronous memory widths.
- The EMIF always reads the lower addresses first and packs these into the least-significant bytes. It packs subsequent accesses into the higher-order bytes. Thus, the expected packing format in ROM is always little-endian, regardless of the value of the LENDIAN bit.

Table 2-8. Byte Address to EA Mapping for Asynchronous Memory Widths

	EA Line																			
	21	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**
Width	**Logical Byte Address**																			
×32	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
×16	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
×8	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

2.6.1 8-Bit ROM Mode

In 8-bit ROM mode, the address is left-shifted by 2 bits to create a byte address on EA to access byte-wide ROM. The EMIF always packs four consecutive bytes aligned on a 4-byte boundary (byte address = 4N) into a word access, regardless of the access size. For example, a byte read results in the EMIF performing 4-byte accesses on the external bus, but only one byte is returned from the EMIF to the requestor. The bytes are fetched in the following address order: 4N, 4N + 1, 4N + 2, 4N + 3. Bytes are packed into the 32-bit word from MSByte to LSByte in the following little-endian order: 4N + 3, 4N + 2, 4N + 1, 4N.

2.6.2 16-Bit ROM Mode

In 16-bit ROM mode, the address is left-shifted by 1 bit to create a half-word address on EA to access 16-bit-wide ROM. The EMIF always packs two consecutive halfwords aligned on a 4-byte boundary (byte address = 4N) into a word access. The halfwords are fetched in the following address order: 4N, 4N + 2. Halfwords are packed into the 32-bit word from the most-significant halfword to the least-significant halfword in the following little-endian order: 4N + 2, 4N.

2.7 Memory Request Priority

The C620x/C670x EMIF has multiple requestors competing for the interface. Table 2-9 summarizes the priority scheme that the EMIF uses in the case of multiple pending requests. The priority scheme may change if the DMA channel that issues a request through the DMA controller is of high priority. This mode is set in the DMA controller by setting the PRI bit in the DMA channel primary control register.

Once a requester (in this instance, the refresh controller is considered a requester) is prioritized and chosen, the EMIF will not recognize any new requests until either the chosen requester stops making requests or a subsequent higher priority request occurs. In this case, all issued requests of the previous requester are allowed to finish while the new requester starts making its requests.

If the arbitration bit (RBTR8) of GBLCTL is set to 1 and if a higher priority requester needs the EMIF, the higher priority requester does not gain control until the current controller relinquishes control or until eight word requests have finished. If the arbitration bit is not set (RBTR8 = 0), a requester maintains control of the EMIF as long as it needs the EMIF or until a higher priority requester requests the EMIF. When the RBTR8 bit is not set, a higher priority requester will interrupt the current controller regardless of the number of requests that have occurred.

Table 2-9. EMIF Prioritization of Memory Requests

Priority	Requestor when PRI = 1	Requestor when PRI = 0
Highest	External hold	External hold
	Mode register set	Mode register set
	Urgent refresh	Urgent refresh
	DMA controller	DMC(1)
	DMC(1)	PMC(2)
	PMC(2)	DMA controller
Lowest	Trickle refresh	Trickle refresh

(1) DMC = Data Memory Controller.
(2) PMC = Program Memory Controller

2.8 EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through memory-mapped registers within the EMIF. Access to these registers requires the EMIF clock. Table 2-10 lists the memory-mapped registers and their memory addresses in the C620x/C670x DSP.

Table 2-10. EMIF Registers for C620x/C670x DSP

Acronym	Register Name	Hex Byte Address	Section
GBLCTL	EMIF global control register	0180 0000h	Section 2.8.1
CECTL0	EMIF CE0 space control register	0180 0008h	Section 2.8.2
CECTL1	EMIF CE1 space control register	0180 0004h	Section 2.8.2
CECTL2	EMIF CE2 space control register	0180 0010h	Section 2.8.2
CECTL3	EMIF CE3 space control register	0180 0014h	Section 2.8.2
SDCTL	EMIF SDRAM control register	0180 0018h	Section 2.8.3
SDTIM	EMIF SDRAM refresh control register	0180 001Ch	Section 2.8.4

2.8.1 EMIF Global Control Register (GBLCTL)

The EMIF global control register (GBLCTL) configures parameters common to all the CE spaces. The GBLCTL is shown in Figure 2-14 and and described in Figure 2-15.

In order to support as many common programming practices as possible between the C620x/C670x devices, the SSCEN and SDCEN fields are used to enable the memory interface clock, CLKOUT2. If SBSRAM is used in the system, as specified by the MTYPE field in the CE space control register (CECTL), SSCEN enables or disables CLKOUT2. If SDRAM is used, as specified by MTYPE, SDCEN enables or disables CLKOUT2.

Figure 2-14. EMIF Global Control Register (GBLCTL) (C6201/C6701 DSP)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R/W-0															

15	14	13	12	11	10	9	8
Reserved(A)				Reserved	ARDY	HOLD	HOLDA
R/W-0	R/W-0	R/W-1	R/W-1	R-x	R-x	R-x	R-x

7	6	5	4	3	2	1	0
NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R-x

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; -x = value is indeterminate after reset

(A) The reserved bit fields should always be written with their default values when modifying the GBLCTL. Writing a value other than the default value to these fields may cause improper operation.

Figure 2-15. EMIF Global Control Register (GBLCTL) (C6202/C6203/C6204/C6205 DSP)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R/W-0															

15	14	13	12	11	10	9	8
Reserved(A)				Reserved	ARDY	HOLD	HOLDA
R/W-0	R/W-0	R/W-1	R/W-1	R-x	R-x	R-x	R-x

7	6	5	4	3	2	1	0
NOHOLD	SDCEN	SSCEN	CLK1EN	Reserved(A)		RBTR8	MAP
R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R-x

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; -x = value is indeterminate after reset

(A) The reserved bit fields should always be written with their default values when modifying the GBLCTL. Writing a value other than the default value to these fields may cause improper operation.

Table 2-11. EMIF Global Control Register (GBLCTL) Field Descriptions

Bit	*field*	*symval*	Value	Description
31-11	Reserved	-	0	Reserved. A value written to this field has no effect.
10	ARDY			ARDY input bit.
		LOW	0	ARDY input is low. External device is not ready.
		HIGH	1	ARDY input is high. External device is ready.
9	HOLD			$\overline{\text{HOLD}}$ input bit.
		LOW	0	$\overline{\text{HOLD}}$ input is low. External device requesting EMIF.
		HIGH	1	$\overline{\text{HOLD}}$ input is high. No external request pending.
8	HOLDA			$\overline{\text{HOLDA}}$ output bit.
		LOW	0	$\overline{\text{HOLDA}}$ output is low. External device owns EMIF.
		HIGH	1	$\overline{\text{HOLDA}}$ output is high. External device does not own EMIF.
7	NOHOLD			External NOHOLD enable bit.
		DISABLE	0	No hold is disabled. Hold requests via the $\overline{\text{HOLD}}$ input are acknowledged via the HOLDA output at the earliest possible time.
		ENABLE	1	No hold is enabled. Hold requests via the $\overline{\text{HOLD}}$ input are ignored.
6	SDCEN			SDCLK enable bit. This bit enables CLKOUT2 if SDRAM is used in system (specified by the MTYPE field in in the CE space control register).
		DISABLE	0	SDCLK is held high.
		ENABLE	1	SDCLK is enabled to clock.
5	SSCEN			SSCLK enable bit. This bit enables CLKOUT2 if SBSRAM is used in the system (specified by the MTYPE field in in the CE space control register).
		DISABLE	0	SSCLK is held high.
		ENABLE	1	SSCLK is enabled to clock.
4	CLK1EN			CLKOUT1 enable bit.
		DISABLE	0	CLKOUT1 is held high.
		ENABLE	1	CLKOUT1 is enabled to clock.
3	CLK2EN			**For C6201/C6701 DSP:** CLKOUT2 is enabled/disabled using SSCEN/SDCEN bits.
		DISABLE	0	CLKOUT2 is held high.
		ENABLE	1	CLKOUT2 is enabled to clock.
2	SSCRT			**For C6201/C6701 DSP:** SBSRAM clock rate select bit.
		CPUOVR2	0	SSCLK runs at 1/2 CPU clock rate.
		CPU	1	SSCLK runs at CPU clock rate.
1	RBTR8			Requester arbitration mode bit.
		HPRI	0	The requester controls the EMIF until a high-priority request occurs.
		8ACC	1	The requester controls the EMIF for a minimum of eight accesses.
0	MAP			Map mode bit contains the value of the memory map mode of the device.
		MAP0	0	Map 0 is selected. External memory located at address 0.
		MAP1	1	Map 1 is selected. Internal memory located at address 0.

2.8.2 EMIF CE Space Control Registers (CECTL0-3)

The CE space control register (CECTL) is shown in and described in Table 2-12. These registers correspond to the CE memory spaces supported by the EMIF. There are four CE space control registers corresponding to the four external CE signals.

The MTYPE field identifies the memory type for the corresponding CE space. If the MTYPE field selects a synchronous memory type, the remaining register fields have no effect. If the MTYPE field selects an asynchronous type, the remaining register fields specify the shaping of the address and control signals for access to that space. These features are discussed in Section 1.5.

The MTYPE field should only be set once during system initialization, except when CE1 is used for ROM boot mode. In this mode, the CE space can be configured to another asynchronous memory type.

Except for C6201/C6701 DSPs, all other C620x/C670x DSPs support one synchronous memory type because these devices support SDRAM background refresh and they have shared synchronous memory control signals. The presence of both memory types could corrupt SBSRAM accesses during SDRAM refresh. Therefore, software must ensure that when a CE space is set up as a synchronous memory type, no other CE spaces are set up as a different synchronous memory type. For example, if a CE space is set as SBSRAM, then no other CE spaces should be set as SDRAM. Similarly, if a CE space is set as SDRAM, then no other CE spaces should be set as SBSRAM.

Figure 2-16. EMIF CE Space Control Register (CECTL)

31	28	27	22	21	20	19	16
WRSETUP		WRSTRB		WRHLD		RDSETUP	
R/W-1111		R/W-11 1111		R/W-11		R/W-1111	

15	14	13	8	7	6	4	3	2	1	0
Reserved		RDSTRB		—	MTYPE		Reserved		RDHLD	
R/W-0		R/W-11 1111		R/W-0	R/W-010		R/W-0		R/W-11	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2-12. EMIF CE Space Control Register (CECTL) Field Descriptions

Bit	*field*	*symval*	Value	Description
31-28	WRSETUP	OF(*value*)	0-Fh	Write setup width. Number of clock cycles of setup time for address (EA), chip enable ($\overline{CE}$), and byte enables ($\overline{BE}$) before write strobe falls. For asynchronous read accesses, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
27-22	WRSTRB	OF(*value*)	0-3Fh	Write strobe width. The width of write strobe ($\overline{AWE}$) in clock cycles.
21-20	WRHLD	OF(*value*)	0-3h	Write hold width. Number of clock cycles that address (EA) and byte strobes ($\overline{BE}$) are held after write strobe rises. For asynchronous read accesses, this is also the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.
19-16	RDSETUP	OF(*value*)	0-Fh	Read setup width. Number of clock cycles of setup time for address (EA), chip enable ($\overline{CE}$), and byte enables ($\overline{BE}$) before read strobe falls. For asynchronous read accesses, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
15-14	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
13-8	RDSTRB	OF(*value*)	0-3Fh	Read strobe width. The width of read strobe ($\overline{ARE}$) in clock cycles.
7	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.

Table 2-12. EMIF CE Space Control Register (CECTL) Field Descriptions (continued)

Bit	*field*	*symval*	Value	Description
6-4	MTYPE		0-7h	Memory type of the corresponding CE spaces.
		ASYNC8	0	8-bit wide asynchronous interface.
		ASYNC16	1h	16-bit-wide asynchronous interface.
		ASYNC32	2h	32-bit-wide asynchronous interface.
		SDRAM32	3h	32-bit-wide SDRAM.
		SBSRAM32	4h	32-bit-wide SBSRAM.
		-	5h-7h	Reserved.
3-2	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1-0	RDHLD	OF(*value*)	0-3h	Read hold width. Number of clock cycles that address (EA) and byte strobes ($\overline{BE}$) are held after read strobe rises. For asynchronous read accesses, this is also the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.

2.8.3 EMIF SDRAM Control Register (SDCTL)

The SDRAM control register (SDCTL) controls SDRAM parameters for all CE spaces that specify an SDRAM memory type in the MTYPE field of the associated CE space control register (CECTL). Because SDCTL controls all SDRAM spaces, each space must contain SDRAM with the same refresh, timing, and page characteristics. SDCTL should not be modified while accessing SDRAM. The SDCTL is shown in Figure 2-17 and described in Table 2-13.

Figure 2-17. EMIF SDRAM Control Register (SDCTL)

31	27	26	25	24	23	20	19	16
Reserved		SDWID	RFEN	INIT	TRCD		TRP	
R/W-0		R/W-0	R/W-1	R/W-1	R/W-1000		R/W-1000	

15	12	11	0
TRC		Reserved	
R/W-1111		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2-13. EMIF SDRAM Control Register (SDCTL) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31-27	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
26	SDWID			SDRAM column width select.
		4X8BIT	0	9 column address pins (512 elements per row).
		2X16BIT	1	8 column address pins (256 elements per row).
25	RFEN			Refresh enable bit. If SDRAM is not used, be sure RFEN = 0; otherwise, BUSREQ may become asserted when SDRAM timer counts down to 0.
		DISABLE	0	SDRAM refresh is disabled.
		ENABLE	1	SDRAM refresh is enabled.
24	INIT			Initialization bit. This bit forces initialization of all SDRAM present. Reading this bit returns an undefined value.
		NO	0	No effect.
		YES	1	Initialize SDRAM in each CE space configured for SDRAM. The CPU should initialize all of the CE space control registers before setting INIT = 1.
23-20	TRCD	OF(*value*)	0-Fh	Specifies the t_{RCD} value of the SDRAM in EMIF clock cycles.(2) TRCD = t_{RCD} / t_{cyc} - 1
19-16	TRP	OF(*value*)	0-Fh	Specifies the t_{RC} value of the SDRAM in EMIF clock cycles.(2) TRP = t_{RP} / t_{cyc} - 1
15-12	TRC	OF(*value*)	0-Fh	Specifies the t_{RC} value of the SDRAM in EMIF clock cycles.(2) TRC = t_{RC} / t_{cyc} - 1
11-0	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.

(1) For CSL implementation, use the notation EMIF_SDCTL_*field_symval.*
(2) t_{cyc} refers to the EMIF clock period, which is equal to CLKOUT2 period for C620x/C670x DSP.

2.8.4 EMIF SDRAM Timing Register (SDTIM)

The SDRAM timing register (SDTIM) controls the refresh period in terms of EMIF clock cycles. The SDTIM is shown in Figure 2-18 and described in Table 2-14. Optionally, the PERIOD field can send an interrupt to the CPU. Thus, this counter can be used as a general-purpose timer if SDRAM is not used by the system. The CPU can read the counter (CNTR) field. When the counter reaches 0, it is automatically reloaded with the period, and SDINT (synchronization event to EDMA and interrupt source to CPU) is asserted. See Section 2.4.4 and Section 1.3.3 for more information on SDRAM refresh.

Figure 2-18. EMIF SDRAM Timing Register (SDTIM)

31 24	23 12	11 0
Reserved	CNTR	PERIOD
R/W-0	R-080h	R/W-080h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2-14. EMIF SDRAM Timing Register (SDTIM) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31-24	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
23-12	CNTR	OF(*value)*	0-FFFh	Current value of the refresh counter.
11-0	PERIOD	OF(*value)*	0-FFFh	Refresh period in EMIF clock cycles. (2)

(1) For CSL implementation, use the notation EMIF_SDTIM_*field_symval.*
(2) EMIF clock cycles are in terms of CLKOUT2 period for C620x/C670x DSP.

TMS320C621x/C671x EMIF

This chapter describes the operation and registers of the EMIF in the TMS320C621x/C671x DSP. For operation and registers unique to the TMS320C620x/C670x EMIF, see Chapter 2. For operation and registers unique to the TMS320C64x™ EMIF, see Chapter 4.

Topic **Page**

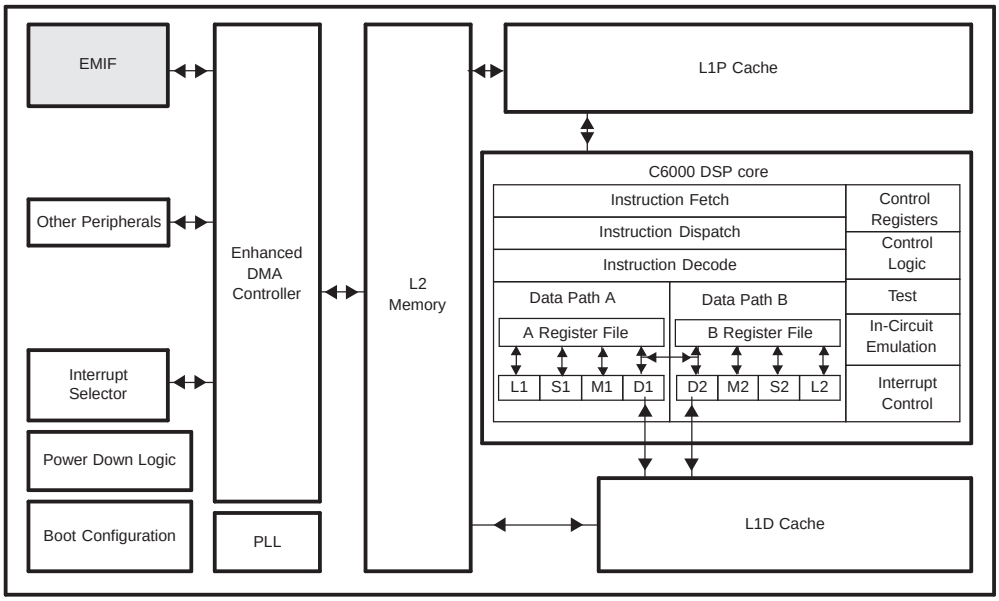
3.1 Overview

The C621x/C671x EMIF services requests of the external bus from two requestors:

- On-chip enhanced direct-memory access (EDMA) controller
- External shared-memory device controller

A block diagram of the C621x/C671x DSP is shown in Figure 3-1.

Figure 3-1. TMS320C621x/C671x DSP Block Diagram



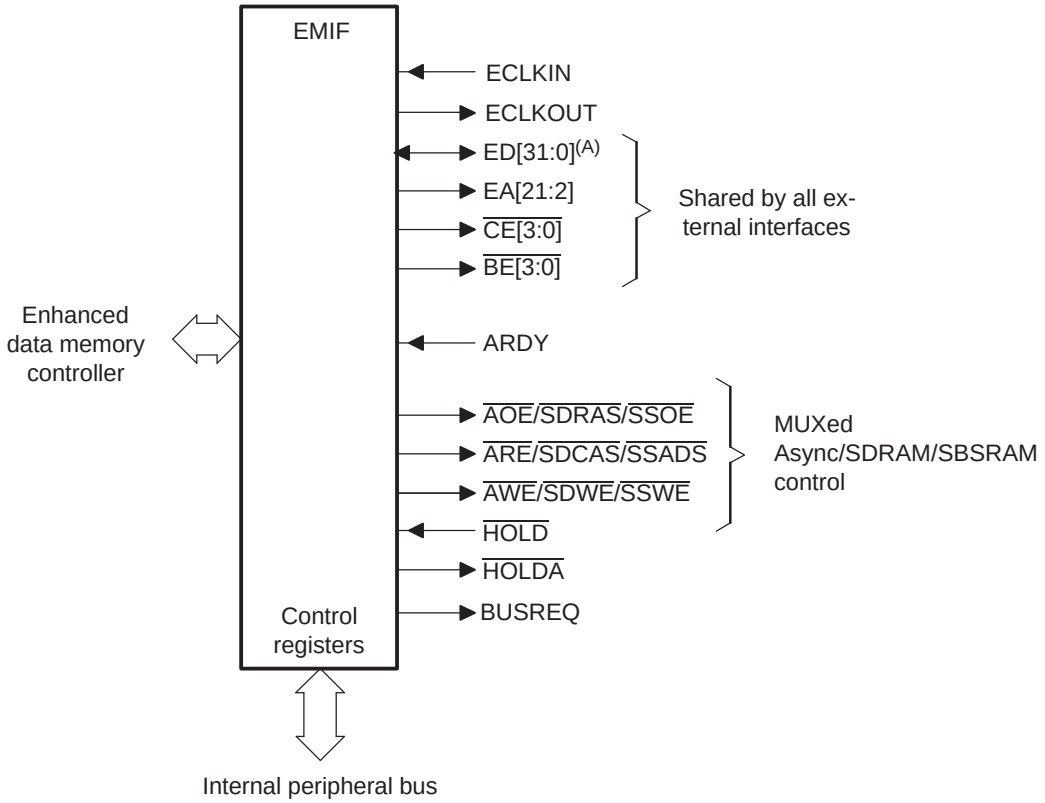
(1) Not all peripherals exist on all C621x/C671x devices. Refer to the device-specific datasheet for the peripheral set.

3.2 EMIF Interface Signals

The EMIF signals of the C621x/C671x DSP are shown in Figure 3-2 and described in Table 3-1. The C621x/C671x EMIF has the following features:

- All of the memories interfacing with the C621x/C671x EMIF should operate off of ECLKOUT (EMIF clock output). On the C6713 DSP, ECLKOUT runs at either ECLKIN or SYSCLK3, configurable using the EKSRC bit in DEVCFG. SYSCLK3 is an internally-generated divide-down clock with programmable divide ratio and PLL output as the reference clock. All other C621x/C671x devices require that the system provide an external clock source (ECLKIN). The ECLKOUT signal is produced internally based on ECLKIN or SYSCLK3 (C6713 DSP only). If desired, the CLKOUT2 output can be routed back to the ECLKIN input.
- The SDRAM, SBSRAM, and asynchronous signals are combined. A system can include all three memory types, since no background refresh is performed.
- Unlike the C620x/C670x EMIF, the C621x/C671x EMIF space CE1 supports all three types of memory.
- The synchronized memory interfaces use a four-word burst length that is optimized for the two-level cache architecture.
- The SDRAM interface is flexible, allowing interfaces to a wide range of SDRAM configurations.
- The SDA10 pin has been removed. Address pin EA[12] serves the function of the SDA10 pin for the SDRAM memories.

Figure 3-2. TMS320C621x/C671x EMIF Interface Signals



A C6712/C6712C DSP uses ED[15:0].

Table 3-1. TMS320C621x/C671x EMIF Interface Signal Descriptions

Pin	I/O/Z	Description
CLKOUT1	O	Clock output. Runs at the CPU clock rate.
CLKOUT2	O	Clock output. Runs at 1/2 the CPU clock rate.
ECLKIN	I	EMIF clock input. Must be provided by the system on C621x/C671x DSP.
ECLKOUT	O	EMIF clock output. Based on ECLKIN or SYSCLK3 (C6713 DSP only). All EMIF I/O are clocked relative to ECLKOUT.
ED[31:0]	I/O/Z	EMIF 32-bit data bus I/O (C6712 DSP has a 16-bit bus; therefore, ED[31:16] do not apply).
EA[21:2] (1)	O/Z	External address output. Drives bits 21-2 of the byte address. (Effectively a word address.)
$\overline{CE0}$	O/Z	Active-low chip select for memory space CE0.
$\overline{CE1}$	O/Z	Active-low chip select for memory space CE1.
$\overline{CE2}$	O/Z	Active-low chip select for memory space CE2.
$\overline{CE3}$	O/Z	Active-low chip select for memory space CE3.
$\overline{BE[3:0]}$	O/Z	Active-low byte enables. Individual bytes and halfwords can be selected for write cycles. For read cycles, all four byte-enables are active.
ARDY	I	Ready. Active-high asynchronous ready input used to insert wait states for slow memories and peripherals.
AOE	O/Z	Active-low output enable for asynchronous memory interface.
SDRAS	O/Z	Active-low row address strobe for SDRAM memory interface.
SSOE	O/Z	Active low output buffer enable for SBSRAM interface.
ARE	O/Z	Active-low read strobe for asynchronous memory interface.
SDCAS	O/Z	Active-low column address strobe for SDRAM memory interface.
SSADS	O/Z	Active-low address strobe/enable for SBSRAM interface.
AWE	O/Z	Active-low write strobe for asynchronous memory interface.
SDWE	O/Z	Active-low write enable for SDRAM memory interface.
SSWE	O/Z	Active-low write enable for SBSRAM interface.
HOLD	I	Active-low external bus hold (3-state) request.
HOLDA	O	Active-low external bus hold acknowledge.
BUSREQ	O	Active-high bus request signal. Indicates pending refresh or memory access.

(1) EMIF address numbering for the C6712/C6712C 16-bit EMIF begins with EA2 to maintain signal name compatibility with the C62x/C67x 32-bit EMIF.

3.3 Memory Width and Byte Alignment

The C621x/C671x EMIF supports memory widths of 8 bits, 16 bits, and 32 bits, including reads and writes of both big- and little-endian devices. The C6712 EMIF supports memory widths of 8 bits and 16 bits only. There is no distinction between ROM and asynchronous interface. For all memory types, the address is internally shifted to compensate for memory widths of less than 32 bits. The least-significant address bit is always output on external address pin EA2, regardless of the width of the device. Accesses to 8-bit memories have logical address bit 0 output on EA2. Table 3-2 summarizes the addressable memory ranges on the C621x/C671x device.

The EMIF automatically performs packing and unpacking for word accesses to external memories of less than 32 bits. For a 32-bit write to an 8-bit memory, The EMIF automatically unpacks the data into bytes such that the bytes are written to byte address N, N + 1, N + 2, then N + 3. Likewise, for 32-bit reads from a 16-bit memory, the EMIF takes the data from halfword address N, then N + 1, packed into a 32-bit word, then written to its destination. The byte lane used depends on the endianness of the system as shown in Figure 3-3, Figure 3-4, and Figure 3-5.

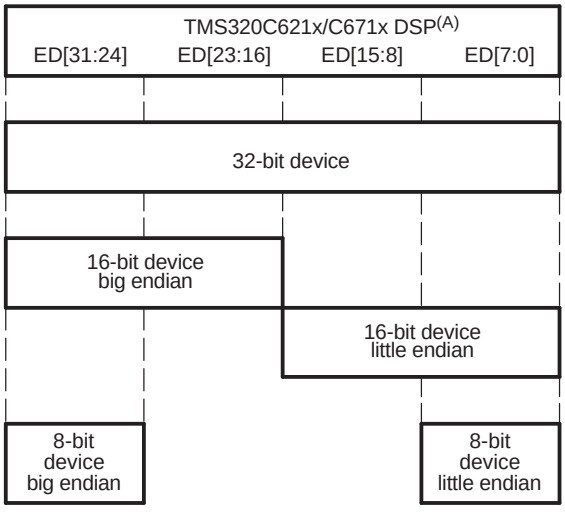
Figure 3-5 shows the C621x/C671x EMIF interface to 16-bit asynchronous SRAM in big-endian mode. Note that in big-endian mode, ED[31:16] are used instead of ED[15:0].

Table 3-2. Addressable Memory Ranges

Memory type	Memory width	Maximum addressable bytes per CE space	Address output on EA[21:2]	Represents
ASRAM		1M	A[19:0]	Byte address
	ı6	2M	A[20:1]	Halfword address
	‘2[(1)]	4M	A[21:2]	Word address
SBSRAM		1M	A[19:0]	Byte address
	ı6	2M	A[20:1]	Halfword address
	‘2[(1)]	4M	A[21:2]	Word address
SDRAM		32M	See Section 3.4	Byte address
	ı6	64M	See Section 3.4	Halfword address
	‘2[(1)]	128M	See Section 3.4	Word address

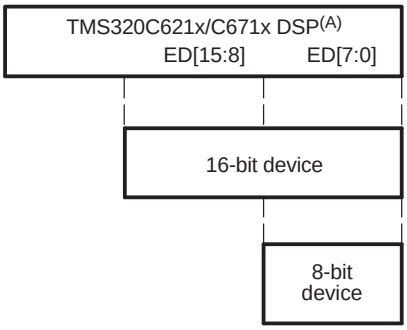
(1) 32-bit interface does not apply to C6712 DSP.

Figure 3-3. Byte Alignment by Endianess - 32-Bit



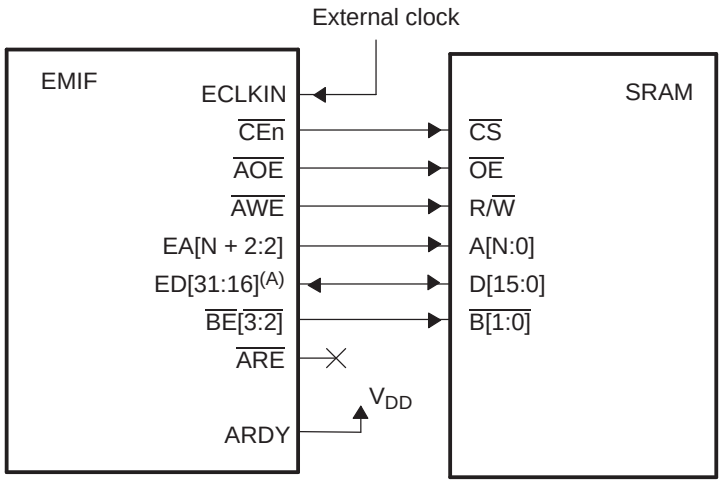
(A) C6712/C6712C DSP do not support big-endian byte alignment.

Figure 3-4. Byte Alignment by Endianess - 16-bit



A C6712/C6712 DSP do not support big-endian byte alignment.

Figure 3-5. TMS320C621x/C671x EMIF to 16-bit SRAM (Big Endian) Block Diagram



A Does not apply to C6712/C6712C DSP, because ED[31:16] do not exist on C6712/C6712C DSP.

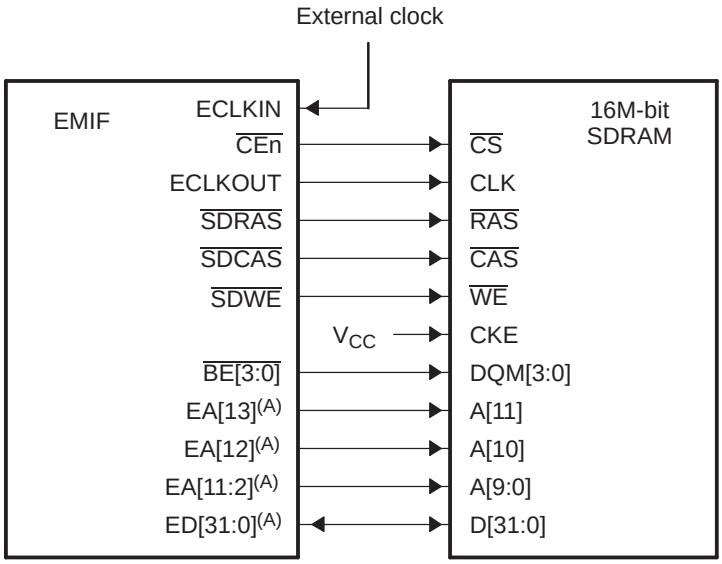
3.4 SDRAM Interface

The C621x/C671x EMIF supports SDRAM commands shown in Table 1-2 and Table 1-3 shows the signal truth table for the SDRAM commands. Table 1-4 summarizes the pin connection and related signals specific to SDRAM operation. Table 1-5 summarizes the similarities and differences on the C6000 SDRAM interface.

The 16M-bit SDRAM interface is shown in Figure 3-6. The C621x/C671x EMIF allows programming of the addressing characteristics of the SDRAM, including the number of column address bits (page size), row address bits (pages per bank), and banks (maximum number of pages that can be opened). The C621x/C671x EMIF can interface to any SDRAM that has 8 to 10 column address pins, 11 to 13 row address pins, and two or four banks. Table 3-3 lists some common SDRAM configurations that interface to the C621x/C671x DSP. Other SDRAM configurations are also possible, as long as they are subsets of the column, row, and bank bits supported by the C621x/C671x DSP.

The number of EMIF address registers limits the maximum number of open pages. Using this information, the C621x/C671x EMIF may open up to four pages of SDRAM simultaneously. The pages can all be in different banks of a single CE space or distributed across multiple CE spaces. Only one page can be open per bank at a time.

Figure 3-6. EMIF to 16M-Bit SDRAM Interface Block Diagram



(A) On C6712/C6712C DSP, EA[12:1] and ED[15:0] are used instead.

Table 3-3. TMS320C621x/C671x DSP Compatible SDRAM

SDRAM Size	B	W	D	Max Devices/ CE	Address-able space		Column Address	Row Address	Bank Select	Pre-charge
16M bit	2	″	2M	8	16M	SDRAM	A9-A0	A10-A0	A11	A10
						EMIF	EA11-EA2	EA12-EA2	EA13	EA12
	2		1M	4	8M	SDRAM	A8-A0	A10-A0	A11	A10
						EMIF	EA10-EA2	EA12-EA2	EA13	EA12
	2	‘16	512K	2	4M	SDRAM	A7-A0	A10-A0	A11	A10
						EMIF	EA9-EA2	EA12-EA2	EA13	EA12
64M bit	4	″	4M	8	64M	SDRAM	A9-A0	A11-A0	A13-A12	A10
						EMIF	EA11-EA2	EA13-EA2	EA15-EA14	EA12
	4		2M	4	32M	SDRAM	A8-A0	A11-A0	A13-A12	A10
						EMIF	EA10-EA2	EA13-EA2	EA15-EA14	EA12
	4	‘16	1M	2	16M	SDRAM	A7-A0	A11-A0	A13-A12	A10
						EMIF	EA9-EA2	EA13-EA2	EA15-EA14	EA12
	4	‘2[3]	512K	1	8M	SDRAM	A7-A0	A10-A0	A12-A11	A10
						EMIF	EA9-EA2	EA12-EA2	EA14-EA13	EA12
128M bit	4		4M	4	64M	SDRAM	A9-A0	A11-A0	A13-A12	A10
						EMIF	EA11-EA2	EA13-EA2	EA15-EA14	EA12
	4	‘16	2M	2	32M	SDRAM	A8-A0	A11-A0	A13-A12	A10
						EMIF	EA10-EA2	EA13-EA2	EA15-EA14	EA12
	4	‘2	1M	1	16M	SDRAM	A7-A0	A11-A0	A13-A12	A10
						EMIF	EA9-EA2	EA13-EA2	EA15-EA14	EA12
256M bit	4		8M	4	128M	SDRAM	A9-A0	A12-A0	A14-A13	A10
						EMIF	EA11-EA2	EA14-EA2	EA16-EA15	EA12
	4	‘16	4M	2	64M	SDRAM	A8-A0	A12-A0	A14-A13	A10
						EMIF	EA10-EA2	EA14-EA2	EA16-EA15	EA12

[1] **Legend:** B = Banks; W = Width; D = Depth

[2] Other SDRAM configurations are possible, if the number of column, row, and bank bits are supported by the C621x/C671x DSP.

[3] The ‘2 Width does not apply to C6712/C6712C DSP.

3.4.1 Monitoring Page Boundaries

The C621x/C671x EMIF can simultaneously open up to four pages of SDRAM. These pages can be within a single CE space, or spread over all CE spaces. For example, two pages can be open in CE0 and CE2, or four pages can be open in CE0. The combination controls, to which logical address bits are compared, determine if a page is open: SDCSZ (which controls NCB), SDRSZ (which controls the number of row address bits, or NRB), and SDBSZ (which controls the number of bank address bits, or NBB). Logical address bits above the bank address bit are not used as part of the page comparison, nor are they used when issuing the row/column commands to the external SDRAM. This implies that the specific configuration of SDRAM used limits the maximum addressable space.

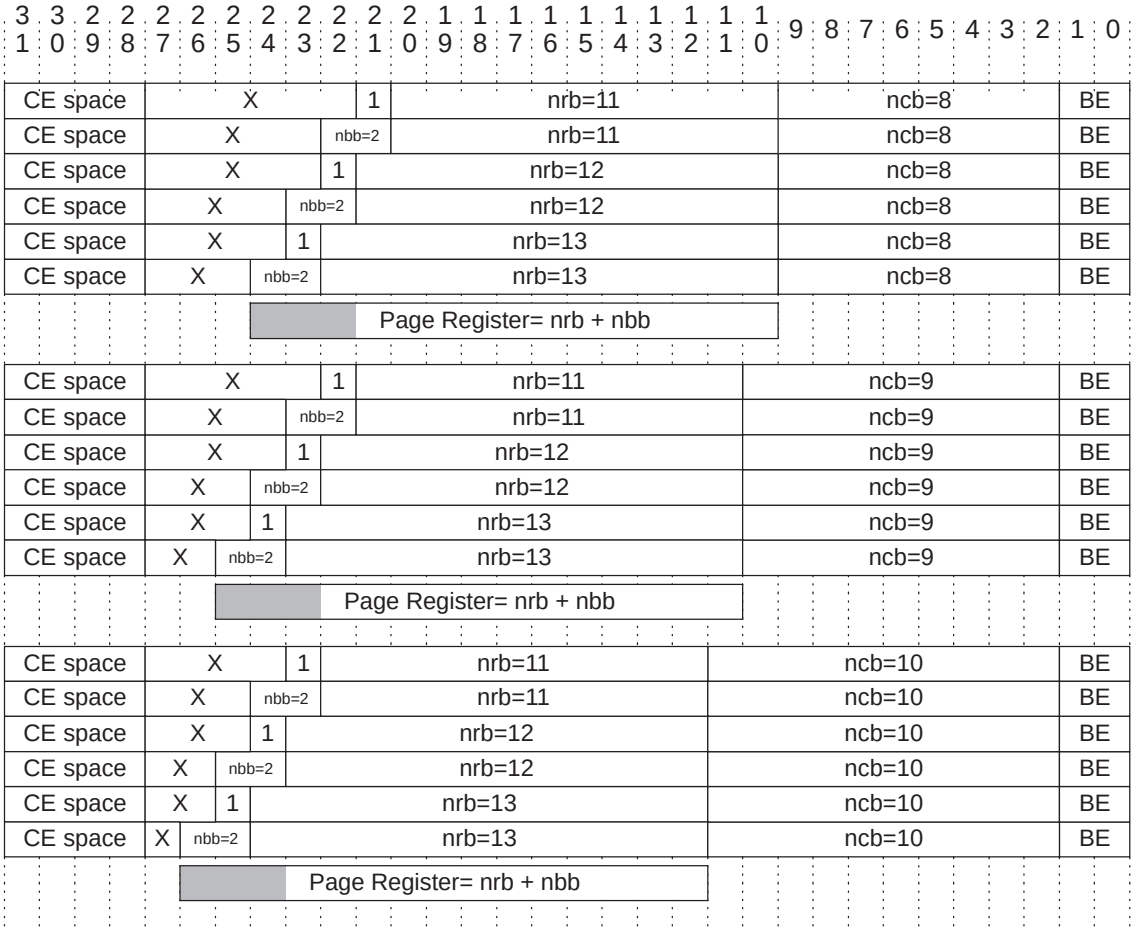
For example, a typical 2-bank ×512K ×16-bit SDRAM has settings of 8 column address bits, 11 row address bits, and 1 bank bit. With this configuration, the maximum amount of addressable space per CE space is $2^{(NCB + NRB + NBB2)}$, or 4 Mbytes.

Note: The + 2 term is appropriate for calculating the addressable space in terms of bytes for a 32 bit interface. If only 16 bits of the bus are populated then + *1* is used, and if only 8 bits of the bus are populated the +*0* is used.

Figure 3-7 details how a 32-bit logical address maps to the page register. For 16- or 8-bit interfaces, the BE portion of the logical address is reduced to 1 bit for 16-bit SDRAM and 0 bits for 8-bit SDRAM. The NCB/NRB/NBB (and page register) shift accordingly.

The C621x/C671x EMIF employs a random page replacement strategy when necessary. This occurs when the total number of external SDRAM banks (not devices) is greater than 4, since the EMIF only contains 4 page registers. This can occur when multiple CE spaces of SDRAM are used. When the number of total banks of SDRAM is less than or equal to 4, the page replacement strategy is fixed, since SDRAM requires that only 1 page can be open within a given bank. If the EMIF detects a page miss either during an access, where a different page was previously accessed in the same CE space (fixed replacement), or if a page must be closed within a different CE space to allow a page register to be assigned for the current access (random replacement), the EMIF performs a DEAC command and starts a new row access.

Figure 3-7. Logical Address-to-Page Register Mapping for 32-Bit Logical Address



(1) ncb = number of column address bits; nrb = number of row address bits; nbb = number of bank address bits.

3.4.2 Address Shift

The same EMIF pins determine the row and column address, thus the C621x/C671x EMIF interface appropriately shifts the address in row and column address selection. Table 3-4 describes the addressing for a 8-, 16-, and 32-bit-wide SDRAM interface. The address presented on the pins are shifted for 8-bit and 16-bit interfaces.

The following factors apply to the address shifting process:

- The address shift is controlled completely by the column size field (SDCSZ) and is unaffected by the bank and row size fields. The bank and row size are used internally to determine whether a page is opened.
- The address bits corresponding to the bank select bits are latched internally by the SDRAM controller during a RAS cycle. The bank select bits are:
  - EA[13 + n:13] for SDRSZ = 00b (11 row pins)
  - EA[14 + n:14] for SDRSZ = 01b (12 row pins)
  - EA[15 + n:15] for SDRSZ = 11b (13 row pins)

  where n = 0, when SDBSZ = 0; and n = 1, when SDBSZ = 1. This ensures that the SDRAM bank select inputs are correct during READ and WRT commands. Thus, the EMIF maintains these values as shown in both row and column addresses.
- EA12 is connected directly to A10 signal, instead of using a dedicated precharge pin SDA10.

Table 3-4. Byte Address-to-EA Mapping for 8-, 16-, and 32-Bit Interface

# of column address bits	Interface bus width	DRAM Cmd	E A [21:17][1]	EA 16	EA 15	EA 14	EA 13	EA 12	EA 11	EA 10	EA9	EA8	EA7	EA6	EA5	EA4	EA3	EA2
				A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8	8	$\overline{RAS}$		22[2]	21[2]	20[2]	19	18	17	16	15	14	13	12	11	10	9	8
		$\overline{CAS}$		Bank[2]				L[3]	L	L	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$		23[2]	22[2]	21[2]	20	19	18	17	16	15	14	13	12	11	10	9
		$\overline{CAS}$		Bank[2]				L[3]	L	L	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$		24[2]	23	22[2]	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$		Bank[2]				L[3]	L	L	9	8	7	6	5	4	3	2
9	8	$\overline{RAS}$		23[2]	22[2]	21[2]	20	19	18	17	16	15	14	13	12	11	10	9
		$\overline{CAS}$		Bank[2]				L[3]	L	8	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$		24[2]	23[2]	22[2]	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$		Bank[2]				L[3]	L	9	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$		25[2]	24[2]	23[2]	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$		Bank[2]				L[3]	L	10	9	8	7	6	5	4	3	2
10	8	$\overline{RAS}$		24[2]	23[2]	22[2]	21	20	19	18	17	16	15	14	13	12	11	10
		$\overline{CAS}$		Bank[2]				L[3]	9	8	7	6	5	4	3	2	1	0
	16	$\overline{RAS}$		25[2]	24[2]	23[2]	22	21	20	19	18	17	16	15	14	13	12	11
		$\overline{CAS}$		Bank[2]				L[3]	10	9	8	7	6	5	4	3	2	1
	32	$\overline{RAS}$		26[2]	25[2]	24[2]	23	22	21	20	19	18	17	16	15	14	13	12
		$\overline{CAS}$		Bank[2]				L[3]	11	10	9	8	7	6	5	4	3	2

(1) Reserved for future use. Undefined.
(2) Bit may not be driven. The number of address bits driven during a $\overline{RAS}$ cycle is equal to the number of (row bits + bank-select bits). During CAS cycle for READ or WRT command, only the bank select address bits (1 or 2 bits, controlled by SDBSZ) are driven to valid values. The address bit(s) used are determined by the number of row address bits and number of bank address bits.
(3) Bit is internally latched during an ACTV command. L = Low; EA12 is driven low during READ or WRT commands to disable autoprecharge.

3.4.3 SDRAM Refresh Mode

The RFEN bit in the SDRAM control register (SDCTL) enables the SDRAM refresh mode of the C621x/C671x EMIF. When RFEN = 0, all EMIF refreshes are disabled, and you must ensure that refreshes are implemented in an external device. When RFEN = 1, the EMIF performs refreshes of SDRAM.

The refresh command (REFR) enables all $\overline{CE}$ signals for all CE spaces selected to use SDRAM (with the MTYPE field of the CE space control register). REFR is automatically preceded by a deactivate (DCAB) command, this ensures that all CE spaces selected with SDRAM are deactivated. Following the DCAB command, the EMIF begins performing trickle refreshes at a rate defined by the PERIOD value in the SDRAM timing register (SDTIM), provided no other SDRAM access is pending.

The REFR requests are considered high priority, and no distinction exists between urgent and trickle refresh. The system allows transfers in progress to complete. The SDRAM refresh period has an extra bitfield, XRFR, in SDTIM that controls the number of extra refreshes performed when the counter reaches 0. This feature allows you to set the XRFR field to perform up to four extra refreshes when the refresh counter expires.

3.4.4 Mode Register Set (MRS)

The C621x/C671x EMIF uses a mode register value of either 0032h or 0022h. The register value and description are shown in and summarized in Table 3-5. Both values program a default burst length of four words for both reads and writes. The value programmed depends on the CAS latency parameter defined by the TCL field in the SDRAM extension register (SDEXT). If the CAS latency is three (TCL = 1), 0032h is written during the MRS cycle. If the CAS latency is two (TCL = 0), 0022h is written during the MRS cycle. Figure 3-9 shows the timing diagram during execution of the MRS command.

Figure 3-8. Mode Register Value

13	12	11	10	9	8	7
EA15	EA14	EA13	SDA10	EA11	EA10	EA9
Reserved				Write burst length	Reserved	
0000				0	00	

6	5	4	3	2	1	0
EA8	EA7	EA6	EA5	EA4	EA3	EA2
Read latency(A)			S/I	Burst length		
01x			0	010		

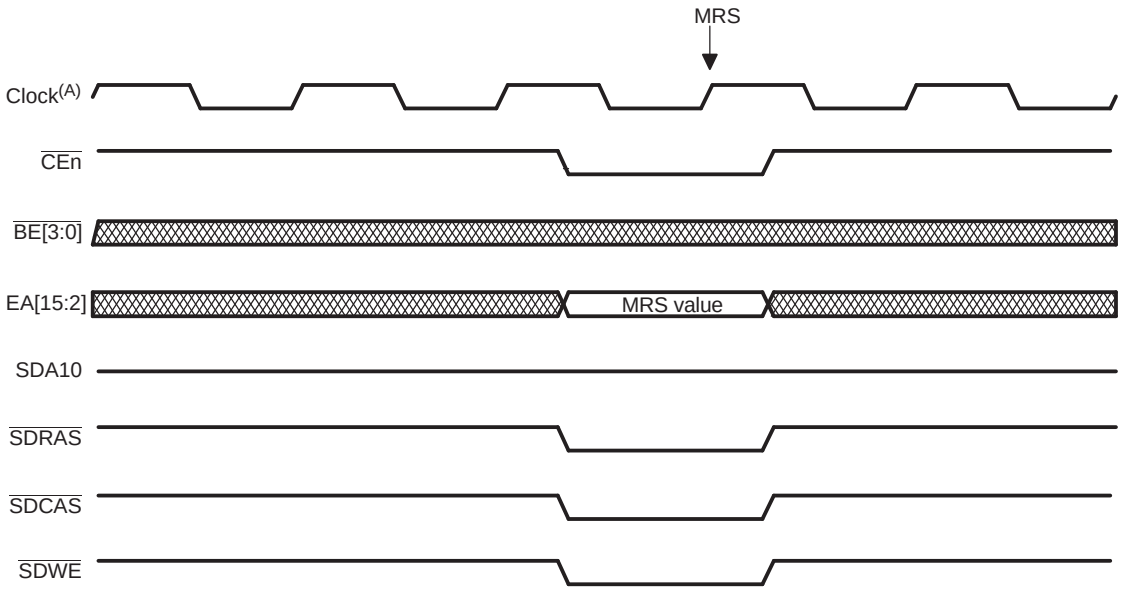
LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(A)If TCL = 0, bit 4 is 0; if TCL = 1, bit 4 is 1.

Table 3-5. Implied SDRAM Configuration by MRS Command

Bit	Field	Selection
9	Write burst length	4 words
6-4	Read latency	If TCL = 0, 2 cycles If TCL = 1, 3 cycles
3	Serial/interleave burst type	Serial
2-0	Burst length	4 words

Figure 3-9. SDRAM Mode Register Set: MRS Command Timing Diagram



A Clock = ECLKOUT.

3.4.5 Timing Requirements

Several SDRAM timing parameters decouple the EMIF from SDRAM speed limitations. The C621x/C671x EMIF has additional timing parameters that are programmable using the SDRAM control register (SDCTL) and the SDRAM extension register (SDEXT), as shown in Table 3-6. Consult the SDRAM data sheet for information on the appropriate parameters for the specific SDRAM.

The C621x/C671x EMIF also allows you to program other functional parameters of the SDRAM controller, listed in section Section 3.7.5. These parameters are not explicitly spelled out in the timing parameters of a data sheet, but you must ensure that the parameters are programmed to a valid value. Table 3-7 shows the recommended values for these SDRAM parameters.

Table 3-6. SDRAM Timing Parameters

Parameter	Description	Value in EMIF clock cycles[1]
t_{RC}	REFR command to ACTV, MRS, or subsequent REFR command	TRC + 1
t_{RCD}	ACTV command to READ or WRT command	TRCD + 1
t_{RP}	DCAB/DEAC command to ACTV, MRS, or REFR command	TRP + 1
t_{CL}	CAS latency of the SDRAM	TCL + 2
t_{RAS}	ACTV command to DEAC/DCAB command	TRAS + 1
t_{RRD}	ACTV bank A to ACTV bank B (same CE space)	TRRD + 2
t_{WR}	Write recovery, time from last data out of C6000 DSP (write data) to DEAC/DCAB command	TWR + 1
t_{HZP}	High Z from precharge, time from DEAC/DCAB to SDRAM outputs (read data) in high Z	THZP + 1

(1) EMIF clock cycles = ECLKOUT cycles.

Table 3-7. Recommended Values for Command-to-Command Parameters

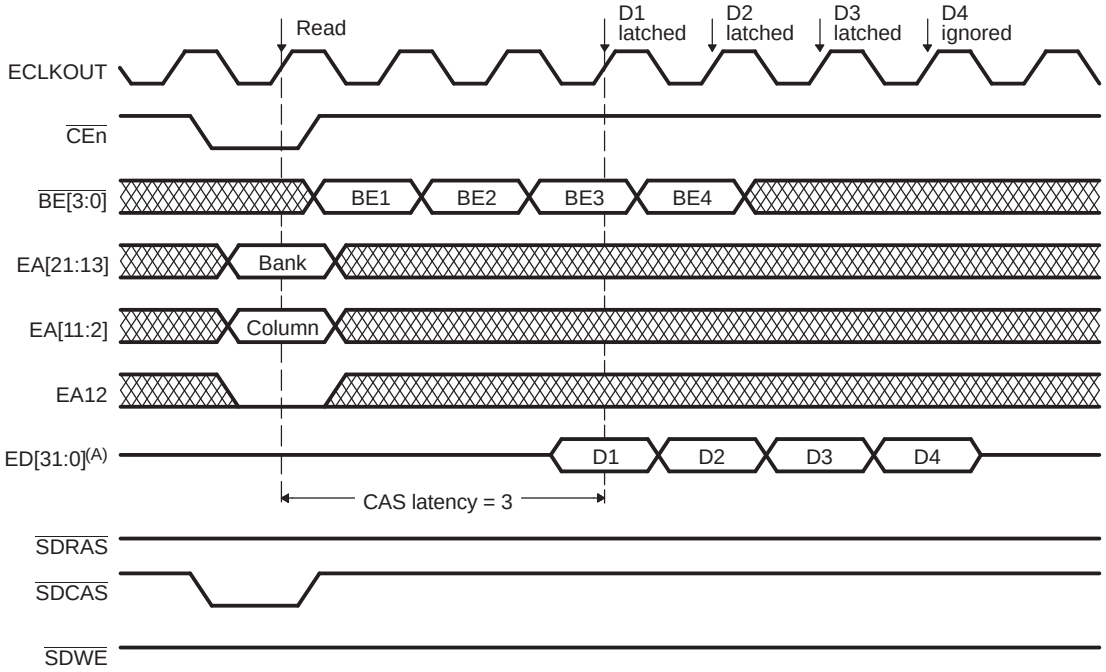
Parameter	Description	Value in EMIF clock cycles[1]	Suggested value for TCL = 0	Suggested value for TCL = 1
READ to READ	READ command to READ command. Used to interrupt a READ burst for random READ addresses.	RD2RD + 1	RD2RD = 0	RD2RD = 0
READ to DEAC	Used in conjunction with t_{HZP}. Specifies the minimum amount of time between READ command and DEAC/DCAB command.	RD2DEAC + 1	RD2DEAC = 1	RD2DEAC = 1
READ to WRITE	READ to WRITE command. The value programmed in this parameter depends on t_{CL}. READ to WRITE should be CAS latency plus 2 cycles (in EMIF clock cycles) to provide 1 turnaround cycle before WRITE command.	RD2WR + 1	RD2WR = 3	RD2WR = 4
BE*n* high before write interrupting read	Specifies the number of cycles that the BE*n* outputs should be high before a write is allowed to interrupt a read. This is related to READ to WRITE parameter.	R2WDQM + 1	R2WDQM = 1	R2WDQM = 2
WRITE to WRITE	Number of cycles between a WRITE interrupting a WRITE. Used for random WRITES.	WR2WR + 1	WR2WR = 0	WR2WR = 0
WRITE to DEAC	Number of cycles between a WRITE command and a DEAC/DCAB command.	WR2DEAC + 1	WR2DEAC = 1	WR2DEAC = 1
WRITE to READ	Number of cycles between a WRITE command and a READ command.	WR2RD + 1	WR2RD = 0	WR2RD = 0

(1) EMIF clock cycles = ECLKOUT cycles.

3.4.6 SDRAM Read

Figure 3-10 shows the C621x/C671x EMIF performing a three word read burst from SDRAM. The EMIF uses a burst length of four, and has a programmable CAS latency of either two or three cycles. The CAS latency is three cycles in this example (CASL = 1). Since the default burst length is four words, the SDRAM returns four pieces of data for every read command. If no additional accesses are pending to the EMIF, as in Figure 3-10, the read burst completes and the unneeded data is disregarded. If accesses are pending, the read burst can be interrupted with a new command (READ, WRT, DEAC, DCAB) controlled by the SDRAM extension register. If a new access is not pending, the system does not perform the DCAB/DEAC command until the page information becomes invalid.

Figure 3-10. SDRAM Three-Word Read Timing Diagram

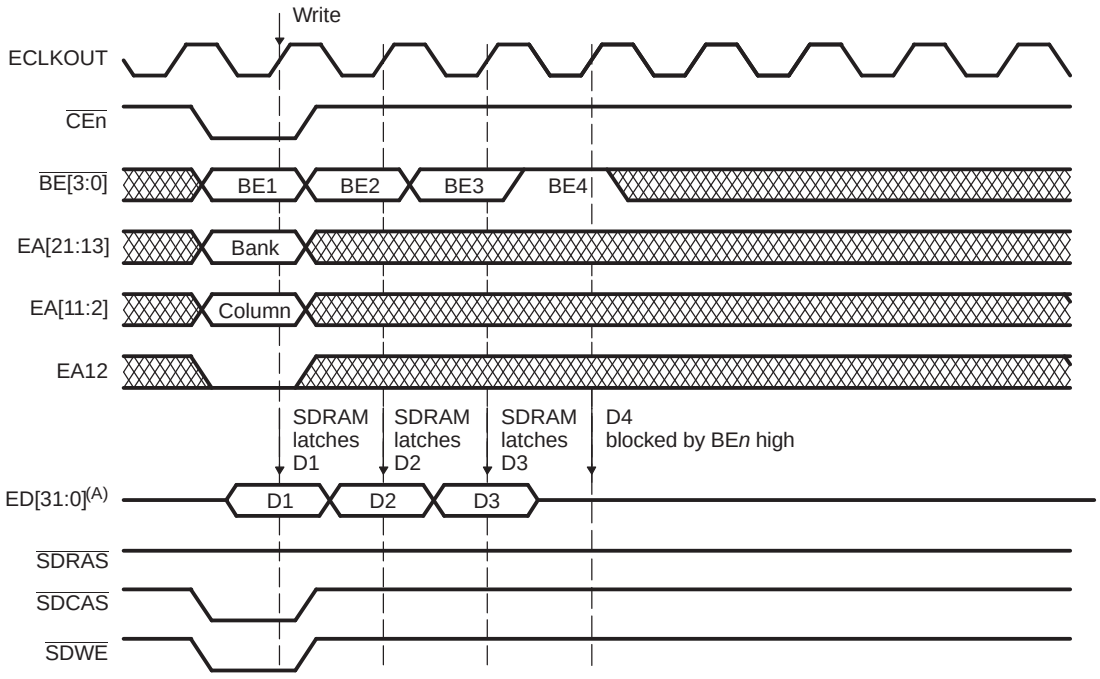


A ED[31:16] do not apply to C6712/C6712C DSP.

3.4.7 SDRAM Write

All SDRAM writes have a burst length of four on the C621x/C671x EMIF. The bank is activated with the row address during the ACTV command. Writes have no latency, so data is output on the same cycle as the column address. Writes to particular bytes are disabled using the appropriate DQM inputs; this feature allows for byte and halfword writes. Figure 3-11 shows the timing for a three-word write on the EMIF. Since the default write-burst length is four words, the last write is masked out using the byte enable signals. On the EMIF, idle cycles are inserted as controlled by the parameters of the SDRAM extension register fields (WR2RD, WR2DEAC, WR2WR, TWR). A DEAC command then deactivates the bank, and the memory interface can begin a new page access. If no new access is pending, the EMIF does not perform the DEAC command until the page information becomes invalid (see Section 3.4.1). The values on the bank select bits (see Section 3.4.2) during column accesses and during the DEAC command are the values latched during the ACTV command.

Figure 3-11. SDRAM Three-Word Write Timing Diagram

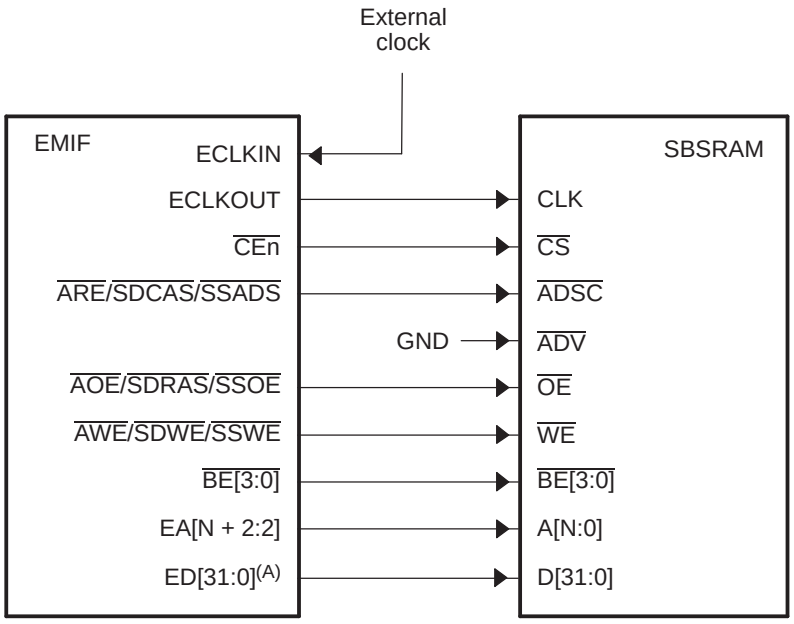


A ED[31:16] do not apply to C6712/C6712C DSP.

3.5 SBSRAM Interface

Figure 3-12 shows the SBSRAM interface on the C621x/C671x EMIF. The interface takes advantage of the internal advance counter of the SBSRAM. For this interface, the ADV signal is pulled low, so that every access to the SBSRAM from the C621x/C671x DSP is assumed to be a four-word burst. If a given access requires nonincrementing addressing, the C621x/C671x EMIF can override the burst feature of the SBSRAM and strobe a new command into the SBSRAM on every cycle, as done by the other C6000 devices. Table 3-8 shows the four-word burst sequencing of standard SBSRAMs in linear burst mode. In order to avoid the SBSRAM wrapping around to an unintended address (indicated in gray), the C621x/C671x EMIF strobes a new address into the SBSRAM. The EMIF also does this if the burst order should be nonincrementing or reverse order burst. After performing a read or write command, the C621x/C671x EMIF issues a deselect command to the SBSRAM if no accesses are pending to that CE space.

Figure 3-12. EMIF to SBSRAM Interface Block Diagram



A ED[31:16] do not apply to C6712/C6712C DSP.

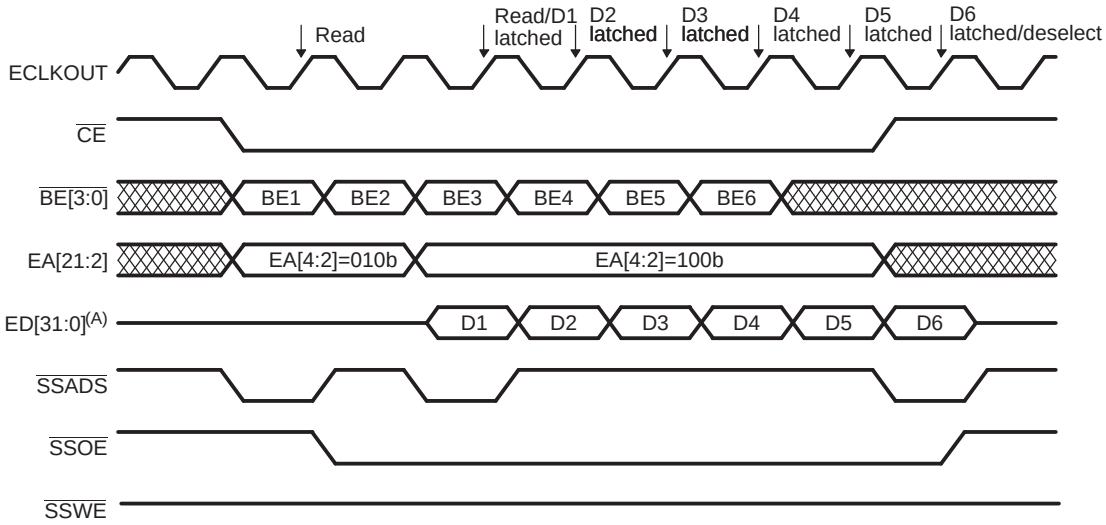
Table 3-8. SBSRAM in Linear Burst Mode

	Case 1	Case 2	Case 3	Case 4
SBSRAM address	A[1:0]	A[1:0]	A[1:0]	A[1:0]
EMIF address	EA[3:2]	EA[3:2]	EA[3:2]	EA[3:2]
First address	00	01	10	11
	01	10	11	00
	10	11	00	01
Fourth address	11	00	01	10

3.5.1 SBSRAM Read

Figure 3-13 shows a six-word read of an SBSRAM for the C621x/C671x EMIF. The address starts with EA[4:2] equal to 010b. The EMIF strobes a new address into the SBSRAM on the third cycle to prevent the internal burst counter from rolling over to 000b. The burst is terminated by deasserting the $\overline{CEn}$ signal while $\overline{SSADS}$ is strobed low.

Figure 3-13. SBSRAM Six-Word Read Timing Diagram



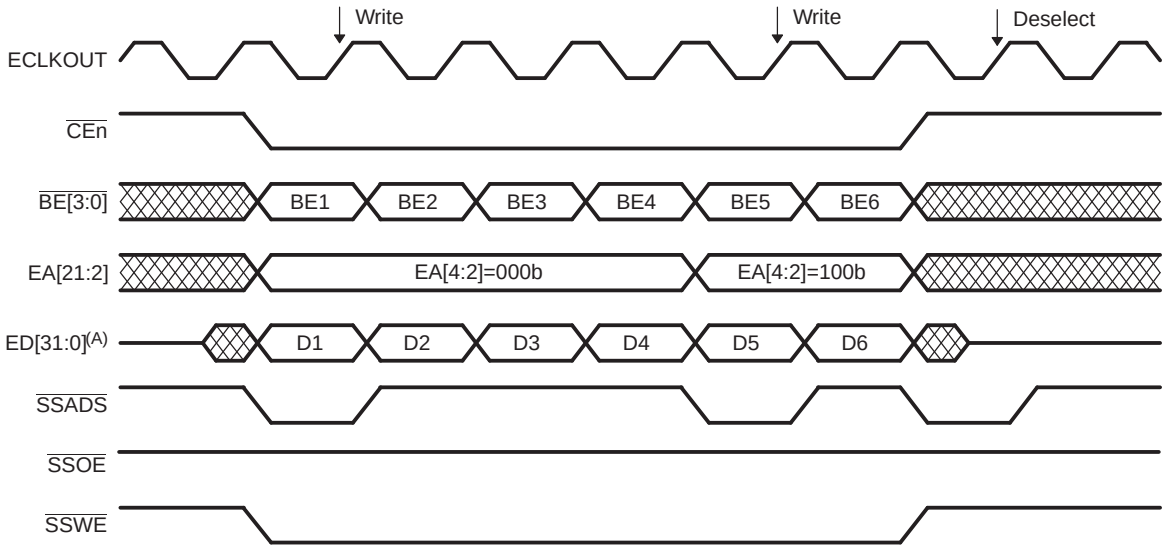
A ED[31:16] do not apply to C6712/C6712C DSP.

Gaps may occur within a read burst due to other DMA activities. The following specific condition also causes a gap in a read burst: when requesting a read from SBSRAM, a delay of one ECLKOUT cycle will be observed. This only happens when reading a burst of (N ɹ4) + 1 elements from SBSRAM; where N = 1, 2, 3, ... In this case, the read is split into two separate bursts. The first (N ɹ4) elements will burst continuously, followed by a delay of one ECLKOUT cycle, then followed by the last one element. For example, when requesting a 13-word read from SBSRAM, the first 12 words will arrive in a burst, followed by one ECLKOUT delay, then followed by the arrival of the thirteenth word. This behavior only affects (N ɹnbsp;4) + 1 element reads from SBSRAM.

3.5.2 SBSRAM Write

Figure 3-14 shows a six-word write to an SBSRAM. The new address is strobed into SBSRAM on the fifth cycle to prevent the SBSRAMs internal burst counter from rolling over to 000b.

Figure 3-14. SBSRAM Six-Word Write Timing Diagram



A ED[31:16] do not apply to C6712/C6712C DSP.

3.6 Memory Request Priority

The C621x/C671x EMIF has multiple requestors competing for the interface. Table 3-9 summarizes the priority scheme that the EMIF uses in the case of multiple pending requests. The C621x/C671x EMIF has fewer interface requestors than the C620x/C670x EMIF because the enhanced DMA (EDMA) controller processes the data memory controller (DMC), program memory controller (PMC), and EDMA transactions. Other requestors include the hold interface and internal EMIF operations, such as mode register set (MRS) and refresh (REFR).

Table 3-9. EMIF Prioritization of Memory Requests

Priority	Requestor
Highest	External hold
	Mode register set
	Refresh
Lowest	Enhanced DMA[(1)]

(1) Refer to *TMS320C6000 DSP Enhanced DMA (EDMA) Controller Reference Guide* (SPRU234)for details on prioritization within the EDMA.

3.7 EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through memory-mapped registers within the EMIF. Access to these registers requires the EMIF clock. Table 3-10 lists the memory-mapped registers in the C621x/C671x DSP. See the device-specific datasheet for the memory address of these registers.

Table 3-10. EMIF Registers for C621x/C671x DSP

Acronym	Register Name	Section
GBLCTL	EMIF global control register	Section 3.7.1
CECTL0-3	EMIF CE space control registers	Section 3.7.2
SDCTL	EMIF SDRAM control register	Section 3.7.3
SDTIM	EMIF SDRAM refresh control register	Section 3.7.4
SDEXT	EMIF SDRAM extension register	Section 3.7.5

3.7.1 EMIF Global Control Register (GBLCTL)

The EMIF global control register (GBLCTL) configures parameters common to all the CE spaces. The GBLCTL is shown in and described in Table 3-11.

Figure 3-15. EMIF Global Control Register (GBLCTL)

31							16
Reserved							
R/W-0							
15			12	11	10	9	8
Reserved(A)				BUSREQ	ARDY	HOLD	HOLDA
R/W-0	R/W-0	R-1	R/W-1	R-0	R-0	R-0	R-0
7	6	5	4	3	2		0
NOHOLD	Reserved	EKEN(B)	CLK1EN(C)	CLK2EN	Reserved		
R/W-0	R-1	R/W-1	R/W-1(C)	R/W-1	R/W-0		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(A) The reserved bit fields should always be written with their default values when modifying the GBLCTL. Writing a value other than the default value to these fields may cause improper operation.

(B) Available on C6713, C6712C, and C6711C devices only; on other C621x/C671x devices, this field is reserved with R/W-1.

(C) This bit is reserved on C6713, C6712C, and C6711C devices with R/W-0. Writing a value other than 0 to this bit may cause improper operation.

Table 3-11. EMIF Global Control Register (GBLCTL) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31-12	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
11	BUSREQ			Bus request (BUSREQ) output bit indicates if the EMIF has an access/refresh pending or in progress.
		LOW	0	BUSREQ output is low. No access/refresh pending.
		HIGH	1	BUSREQ output is high. Access/refresh pending or in progress.
10	ARDY			ARDY input bit.
		LOW	0	ARDY input is low. External device is not ready.
		HIGH	1	ARDY input is high. External device is ready.
9	HOLD			$\overline{\text{HOLD}}$ input bit.
		LOW	0	$\overline{\text{HOLD}}$ input is low. External device requesting EMIF.
		HIGH	1	$\overline{\text{HOLD}}$ input is high. No external request pending.
8	HOLDA			$\overline{\text{HOLDA}}$ output bit.
		LOW	0	$\overline{\text{HOLDA}}$ output is low. External device owns EMIF.
		HIGH	1	$\overline{\text{HOLDA}}$ output is high. External device does not own EMIF.
7	NOHOLD			External NOHOLD enable bit.
		DISABLE	0	No hold is disabled. Hold requests via the $\overline{\text{HOLD}}$ input are acknowledged via the HOLDA output at the earliest possible time.
		ENABLE	1	No hold is enabled. Hold requests via the $\overline{\text{HOLD}}$ input are ignored.
6	Reserved	-	1	Reserved. The reserved bit location is always read as 1. A value written to this field has no effect.
5	EKEN (2)			**For C6713, C6712C, and C6711C DSP:** ECLKOUT enable bit.
			0	ECLKOUT is held low.
			1	ECLKOUT is enabled to clock (default).

(1) For CSL implementation, use the notation EMIF_GBLCTL_*field_symval*.
(2) ECLKOUT does not turn off/on glitch free via EKEN. See Section 1.9.

Table 3-11. EMIF Global Control Register (GBLCTL) Field Descriptions (continued)

Bit	*field* [1]	*symval* [1]	Value	Description
4	CLK1EN			**Not on C6713, C6712C, and C6711C DSP:** CLKOUT1 enable bit.On C6713, C6712C, and C6711C DSP, this bit must be programmed to 0 for proper operation.
		DISABLE	0	CLKOUT1 is held high.
		ENABLE	1	CLKOUT1 is enabled to clock.
3	CLK2EN			CLKOUT2 is enabled/disabled using SSCEN/SDCEN bits.
		DISABLE	0	CLKOUT2 is held high.
		ENABLE	1	CLKOUT2 is enabled to clock.
2-0	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.

3.7.2 EMIF CE Space Control Registers (CECTL0-3)

The CE space control register (CECTL) is shown in and described in Table 3-12. These registers correspond to the CE memory spaces supported by the EMIF. There are four CE space control registers corresponding to the four external CE signals.

The MTYPE field identifies the memory type for the corresponding CE space. If the MTYPE field selects a synchronous memory type, the remaining register fields have no effect. If the MTYPE field selects an asynchronous type, the remaining register fields specify the shaping of the address and control signals for access to that space. These features are discussed in Section 1.5.

The MTYPE field should only be set once during system initialization, except when CE1 is used for ROM boot mode. In this mode, the CE space can be configured to another asynchronous memory type.

Figure 3-16. EMIF CE Space Control Register (CECTL)

31–28	27–22	21–20	19–16
WRSETUP	WRSTRB	WRHLD	RDSETUP
R/W-1111	R/W-11 1111	R/W-11	R/W-1111

15	14	13–8	7–4	3	2–0
TA		RDSTRB	MTYPE	Reserved	RDHLD
R/W-11		R/W-11 1111	R/W-0010	R-0	R/W-011

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3-12. EMIF CE Space Control Register (CECTL) Field Descriptions

Bit	*field* [1]	*symval* [1]	Value	Description
31-28	WRSETUP	OF(*value*)	0-Fh	Write setup width. Number of clock cycles[2] of setup time for address (EA), chip enable ($\overline{CE}$), and byte enables ($\overline{BE}$) before write strobe falls. For asynchronous read accesses, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
27-22	WRSTRB	OF(*value*)	0-3Fh	Write strobe width. The width of write strobe ($\overline{AWE}$) in clock cycles.[2]
21-20	WRHLD	OF(*value*)	0-3h	Write hold width. Number of clock cycles[2] that address (EA) and byte strobes ($\overline{BE}$) are held after write strobe rises. For asynchronous read accesses, this is also the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.
19-16	RDSETUP	OF(*value*)	0-Fh	Read setup width. Number of clock cycles[2] of setup time for address (EA), chip enable ($\overline{CE}$), and byte enables ($\overline{BE}$) before read strobe falls. For asynchronous read accesses, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
15-14	TA	OF(*value*)	0-3h	Minimum Turn-Around time. Turn-around time controls the minimum number of ECLKOUT cycles[2] between a read followed by a write (same or different CE spaces), or between reads from different CE spaces. Applies only to asynchronous memory types.
13-8	RDSTRB	OF(*value*)	0-3Fh	Read strobe width. The width of read strobe ($\overline{ARE}$) in clock cycles[2]
7-4	MTYPE[3]		0-Fh	Memory type of the corresponding CE spaces.
		ASYNC8	0	8-bit-wide asynchronous interface.
		ASYNC16	1h	16-bit-wide asynchronous interface.
		ASYNC32	2h	32-bit-wide asynchronous interface.
		SDRAM32	3h	32-bit-wide SDRAM.
		SBSRAM32	4h	32-bit-wide SBSRAM.
		-	5h-7h	Reserved.
		SDRAM8	8h	8-bit-wide SDRAM.
		SDRAM16	9h	16-bit-wide SDRAM.
		SBSRAM8	Ah	8-bit-wide SBSRAM.
		SBSRAM16	Bh	16-bit-wide SBSRAM.
		-	Ch-Fh	Reserved.
3	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
2-0	RDHLD	OF(*value*)	0-7h	Read hold width. Number of clock cycles[2] that address (EA) and byte strobes ($\overline{BE}$) are held after read strobe rises. For asynchronous read accesses, this is also the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.

(1) For CSL implementation, use the notation EMIF_CECTL_*field_symval.*
(2) Clock cycles are in terms of ECLKOUT for C621x/C671x DSP.
(3) 32-bit interfaces (MTYPE=0010b, 0011b, 0100b) do not apply to C6712 DSP.

3.7.3 EMIF SDRAM Control Register (SDCTL)

The SDRAM control register (SDCTL) controls SDRAM parameters for all CE spaces that specify an SDRAM memory type in the MTYPE field of the associated CE space control register (CECTL). Because SDCTL controls all SDRAM spaces, each space must contain SDRAM with the same refresh, timing, and page characteristics. SDCTL should not be modified while accessing SDRAM. The SDCTL is shown in Figure 3-17 and described in Table 3-13.

Figure 3-17. EMIF SDRAM Control Register (SDCTL)

31	30	29 28	27 26	25	24	23 20	19 16
Reserved	SDBSZ	SDRSZ	SDCSZ	RFEN	INIT	TRCD	TRP
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0100	R/W-1000

15 12	11 0
TRC	Reserved
R/W-1111	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3-13. EMIF SDRAM Control Register (SDCTL) Field Descriptions

Bit	*field* [1]	*symval* [1]	Value	Description
31	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
30	SDBSZ			SDRAM bank size bit.
		2BANKS	0	One bank-select pin (two banks).
		4BANKS	1	Two bank-select pins (four banks).
29-28	SDRSZ		0-3h	SDRAM row size bits.
		11ROW	0	11 row address pins (2048 rows per bank).
		12ROW	1h	12 row address pins (4096 rows per bank).
		13ROW	2h	13 row address pins (8192 rows per bank).
		-	3h	Reserved.
27-26	SDCSZ		0-3h	SDRAM column size bits.
		9COL	0	9 column address pins (512 elements per row).
		8COL	1h	8 column address pins (256 elements per row).
		10COL	2h	10 column address pins (1024 elements per row).
		-	3h	Reserved.
25	RFEN			Refresh enable bit. If SDRAM is not used, be sure RFEN = 0; otherwise, BUSREQ may become asserted when SDRAM timer counts down to 0.
		DISABLE	0	SDRAM refresh is disabled.
		ENABLE	1	SDRAM refresh is enabled.
24	INIT			Initialization bit. This bit forces initialization of all SDRAM present. Reading this bit returns an undefined value.
		NO	0	No effect.
		YES	1	Initialize SDRAM in each CE space configured for SDRAM. The CPU should initialize all of the CE space control registers and SDRAM extension register before setting INIT = 1.
23-20	TRCD	OF(*value*)	0-Fh	Specifies the t_{RCD} value of the SDRAM in EMIF clock cycles.[2] TRCD = t_{RCD} / t_{cyc} - 1
19-16	TRP	OF(*value*)	0-Fh	Specifies the t_{RC} value of the SDRAM in EMIF clock cycles.[2] TRP = t_{RP} / t_{cyc} - 1
15-12	TRC	OF(*value*)	0-Fh	Specifies the t_{RC} value of the SDRAM in EMIF clock cycles.[2] TRC = t_{RC} / t_{cyc} - 1
11-0	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.

(1) For CSL implementation, use the notation EMIF_SDCTL_*field_symval*.
(2) t_{cyc} refers to the EMIF clock period, which is equal to ECLKOUT period for C621x/C671x DSP.

3.7.4 EMIF SDRAM Timing Register (SDTIM)

The SDRAM timing register (SDTIM) controls the refresh period in terms of EMIF clock cycles. The SDTIM is shown in Figure 3-18 and described in Table 3-14. Optionally, the PERIOD field can send an interrupt to the CPU. Thus, this counter can be used as a general-purpose timer if SDRAM is not used by the system. The CPU can read the counter (CNTR) field. When the counter reaches 0, it is automatically reloaded with the period, and SDINT (synchronization event to EDMA and interrupt source to CPU) is asserted. See Section 3.4.3 and Section 1.3.3 for more information on SDRAM refresh.

The XRFR field controls the number of refreshes performed when the refresh counter reaches 0. Up to four refreshes can be performed when the refresh counter expires. For example, since all banks must be deactivated to perform a refresh, it might be desirable to perform two refreshes half as often.

The system considers all refresh requests as high priority. When it is time to refresh, the refresh is performed immediately (though transfers in progress are allowed to complete). All banks are deactivated before a refresh command is issued. When the refresh command is complete, the banks are not restored to their state before refresh.

The initial value for the CNTR field and the PERIOD field is 5DCh (1500 clock cycles). With a 10-ns EMIF cycle time, there is a 15-s time between refresh operations. SDRAMs typically require 15.625 s per refresh.

Figure 3-18. EMIF SDRAM Timing Register (SDTIM)

31 26	25 24	23 12	11 0
Reserved	XRFR	CNTR	PERIOD
R/W-0	R/W-0	R-5DCh	R/W-5DCh

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3-14. EMIF SDRAM Timing Register (SDTIM) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31-26	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
25-24	XRFR	OF(*value*)	0-3h	Extra refreshes controls the number of refreshes performed to SDRAM when the refresh counter expires.
			0	1 refresh.
			1h	2 refreshes.
			2h	3 refreshes.
			3h	4 refreshes.
23-12	CNTR	OF(*value*)	0-FFFh	Current value of the refresh counter.
11-0	PERIOD	OF(*value*)	0-FFFh	Refresh period in EMIF clock cycles. (2)

(1) For CSL implementation, use the notation EMIF_SDTIM_*field_symval.*
(2) EMIF clock cycles are in terms of ECLKOUT for C621x/C671x DSP.

3.7.5 EMIF SDRAM Extension Register (SDEXT)

The SDRAM extension register (SDEXT) allows programming of many parameters of SDRAM. The SDEXT is shown in and described in Table 3-15. This programmability offers two distinct advantages:

- Allows an interface to a wide variety of SDRAMs and is not limited to a few configurations or speed characteristics.
- Allows the EMIF to maintain seamless data transfer from external SDRAM due to features like hidden precharge and multiple open banks.

It should be noted that the SDRAM control register (SDCTL) must be set after configuring SDEXT.

Figure 3-19. EMIF SDRAM Extension Register (SDEXT)

31	21	20	19	18	17	16	15	14	12
Reserved		WR2RD	WR2DEAC		WR2WR	R2WDQM		RD2WR	
R/W-0		R/W-1	R/W-10		R/W-1	R/W-11		R/W-101	

11	10	9	8	7	6	5	4	3	1	0
RD2DEAC		RD2RD	THZP		TWR		TRRD	TRAS		TCL
R/W-11		R/W-1	R/W-10		R/W-01		R/W-1	R/W-111		R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3-15. EMIF SDRAM Extension Register (SDEXT) Field Descriptions

Bit	*field* [1]	*symval* [1]	Value	Description
31-21	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
20	WR2RD	OF(*value*)	0-1	Specifies minimum number of cycles between WRITE to READ command of the SDRAM in ECLKOUT cycles.[2] WR2RD = (# of cycles WRITE to READ) - 1
19-18	WR2DEAC	OF(*value*)	0-3h	Specifies minimum number of cycles between WRITE to DEAC/DCAB command of the SDRAM in ECLKOUT cycles.[2] WR2DEAC = (# of cycles WRITE to DEAC/DCAB) - 1
17	WR2WR	OF(*value*)	0-1	Specifies minimum number of cycles between WRITE to WRITE command of the SDRAM in ECLKOUT cycles.[2] WR2WR = (# of cycles WRITE to WRITE) - 1
16-15	R2WDQM	OF(*value*)	0-3h	Specifies number of of cycles that BEx signals must be high preceding a WRITE interrupting a READ. R2WDQM = (# of cycles BEx high) - 1
14-12	RD2WR	OF(*value*)	0-7h	Specifies number of cycles between READ to WRITE command of the SDRAM in ECLKOUT cycles.[2] RD2WR = (# of cycles READ to WRITE) - 1
11-10	RD2DEAC	OF(*value*)	0-3h	Specifies number of cycles between READ to DEAC/DCAB of the SDRAM in ECLKOUT cycles.[2] RD2DEAC = (# of cycles READ to DEAC/DCAB) - 1
9	RD2RD	OF(*value*)		Specifies number of cycles between READ to READ command (same CE space) of the SDRAM in ECLKOUT cycles.[2]
			0	READ to READ = 1 ECLKOUT cycle.
			1	READ to READ = 2 ECLKOUT cycle.
8-7	THZP	OF(*value*)	0-3h	Specifies t_{HZP} (also known as t_{ROH}) value of the SDRAM in ECLKOUT cycles.[2] THZP = t_{HZP} / t_{cyc} - 1[3]
6-5	TWR	OF(*value*)	0-3h	Specifies t_{WR} value of the SDRAM in ECLKOUT cycles.[2] TWR = t_{WR} / t_{cyc} - 1[3]
4	TRRD	OF(*value*)		Specifies t_{RRD} value of the SDRAM in ECLKOUT cycles.[2]
			0	T_{RRD} = 2 ECLKOUT cycles.
			1	T_{RRD} = 3 ECLKOUT cycles.
3-1	TRAS	OF(*value*)	0-7h	Specifies t_{RAS} value of the SDRAM in ECLKOUT cycles.[2] TRAS = t_{RAS} / t_{cyc} - 1[3]
0	TCL	OF(*value*)		Specified CAS latency of the SDRAM in ECLKOUT cycles.[2]
			0	CAS latency = 2 ECLKOUT cycles.
			1	CAS latency = 3 ECLKOUT cycles.

(1) For CSL implementation, use the notation EMIF_SDEXT_*field_symval.*
(2) EMIF clock cycles are in terms of ECLKOUT for C621x/C671x DSP.
(3) t_{cyc} refers to the EMIF clock period, which is equal to ECLKOUT period for C621x/C671x DSP.

TMS320C64x EMIF

This chapter describes the operation and registers of the EMIF in the TMS320C64x™ DSP. For operation and registers unique to the TMS320C620x/C670x EMIF, see Chapter 2. For operation and registers unique to the TMS320C621x/C671x EMIF, see Chapter 3.

Topic **Page**

4.1 Overview

The C64x EMIF services requests of the external bus from two requestors:

- On-chip enhanced direct-memory access (EDMA) controller
- External shared-memory device controller

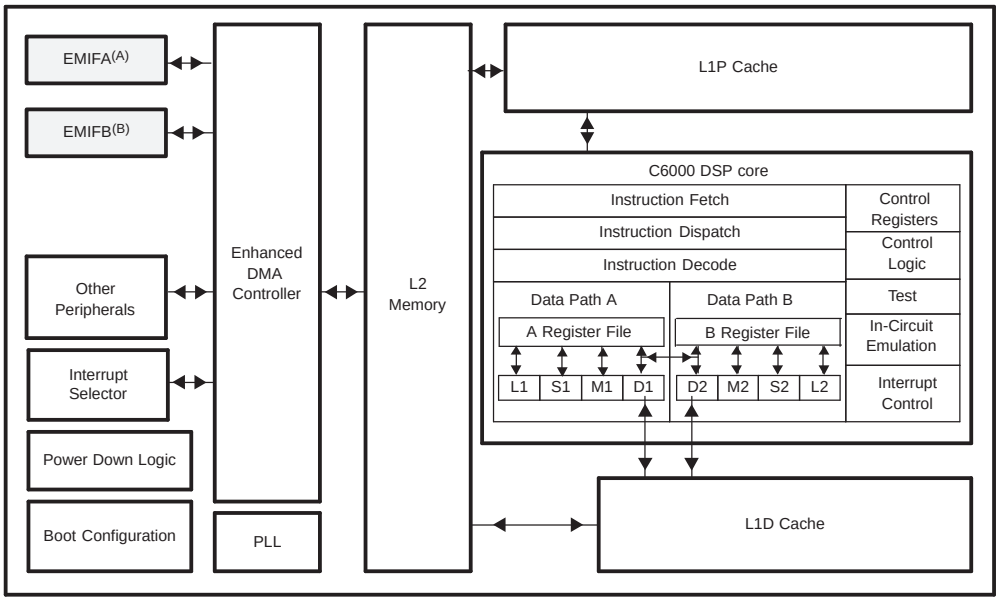
A block diagram of the C64x™ DSP is shown in Figure 4-1. The C64x EMIF offers additional flexibility by replacing the SBSRAM mode with a programmable synchronous mode, which supports glueless interfaces to the following:

- ZBT (zero bus turnaround) SRAM
- Synchronous FIFOs
- Pipeline and flow-through SBSRAM

The C64x DSP may have up to two EMIFs, EMIFA and EMIFB.

- EMIFA: Data bus width is device specific. See Table 4-1.
- EMIFB: 16-bit data bus interface.

Figure 4-1. TMS320C64x DSP Block Diagram



A Not all peripherals exist on all C64x devices. Refer to the device-specific datasheet for the peripheral set.

B Check the device-specific datasheet for the availability of EMIFA and/or EMIFB.

Table 4-1. TMS320C64x EMIFA Bus Widths

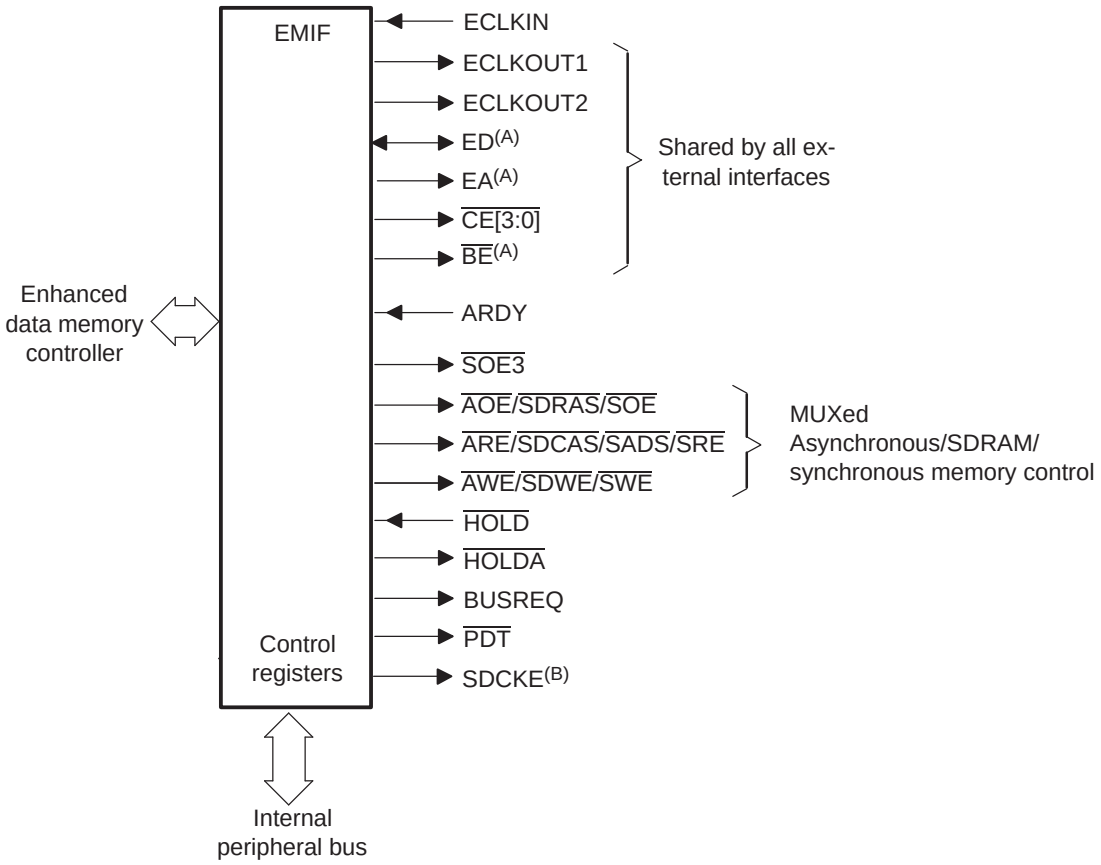
Feature	C6416/15/14/12, DM642/643	C6411, DM640/641
EMIFA bus width	64-bit	32-bit

4.2 EMIF Interface Signals

The EMIF signals of the C64x DSP are shown in Figure 4-2 and described in Table 4-2. These signals apply to both EMIFA and EMIFB with the exception of the SDCKE signal, which applies to EMIFA only. The C64x EMIF is an enhanced version of the C621x EMIF. It includes all the C621x/C671x EMIF features plus the following new features:

- The data bus on EMIFA is either 64-bits or 32-bits wide (see Table 4-1). The data bus on EMIFB is 16-bits wide.
- The EMIF clocks ECLKOUT*n* are generated internally based on the EMIF input clock. At device reset, you can configure one of the following three clocks as the EMIF input clock: internal CPU clock rate divide by 4, internal CPU clock rate divide by 6, or external ECLKIN. All of the memories interfacing with the C64x EMIF should operate off of ECLKOUT*n* (EMIF clock cycle). The ECLKOUT1 frequency equals to EMIF input clock frequency. The ECLKOUT2 frequency is programmable to be EMIF input clock frequency divided by 1, 2, or 4.
- A more flexible programmable synchronous memory controller replaces the SBSRAM controller. Synchronous control pins replace the SBSRAM control pins.
- The $\overline{\text{PDT}}$ pin provides external-to-external transfer support.

Figure 4-2. TMS320C64x EMIFA and EMIFB Interface Signals



A See Table 4-2 for ED, EA, $\overline{\text{CE}}$, and $\overline{\text{BE}}$ pins on EMIFA and EMIFB.

B SDCKE applies to EMIFA only.

Table 4-2. TMS320C64x EMIF Interface Signal Descriptions

Pin	I/O/Z	Description
CLKOUT4	O/Z	Clock output. Runs at 1/4 the CPU clock rate. CLKOUT4 pin is MUXed with the GP1 (general-purpose input/output 1 pin); by default, this pin functions as CLKOUT4.
CLKOUT6	O/Z	Clock output. Runs at 1/6 the CPU clock rate. CLKOUT6 pin is MUXed with the GP2 (general-purpose input/output 2 pin); by default, this pin functions as CLKOUT6.
ECLKIN	I	EMIF clock input.
ECLKOUT1	O/Z	EMIF output clock at EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) frequency.
ECLKOUT2	O/Z	EMIF output clock at EMIF input clock (ECLKIN, CLKOUT4, or CLKOUT6) frequency divided by 1, 2, or 4.
ED[63:0] (1)	I/O/Z	EMIFA 64-bit data bus I/O.
ED[31:0] (1)	I/O/Z	EMIFA 32-bit data bus I/O.
ED[15:0] (2)	I/O/Z	EMIFB 16-bit data bus I/O.
EA[22:3] (1) (3)	O/Z	External address output for EMIFA. Drives bits 22-3 of the byte address.
EA[20:1] (2)	O/Z	External address output for EMIFB. Drives bits 20-1 of the byte address.
$\overline{CE0}$	O/Z	Active-low chip select for memory space CE0.
$\overline{CE1}$	O/Z	Active-low chip select for memory space CE1.
$\overline{CE2}$	O/Z	Active-low chip select for memory space CE2.
$\overline{CE3}$	O/Z	Active-low chip select for memory space CE3.
$\overline{BE[7:0]}$ (1)	O/Z	Active-low byte enables for 64-bit EMIFA. Byte enables go active for only the appropriate byte lane for both writes and reads.
$\overline{BE[3:0]}$ (1)	O/Z	Active-low byte enables for 32-bit EMIFA. Byte enables go active for only the appropriate byte lane for both writes and reads.
$\overline{BE[1:0]}$ (2)	O/Z	Active-low byte enables for EMIFB. Byte enables go active for only the appropriate byte lane for both writes and reads.
ARDY	I	Ready. Active-high asynchronous ready input used to insert wait states for slow memories and peripherals.
$\overline{SOE3}$	O/Z	Synchronous memory output enable for $\overline{CE3}$ (intended for glueless FIFO interface).
$\overline{AOE}$	O/Z	Active-low output enable for asynchronous memory interface.
$\overline{SDRAS}$	O/Z	Active-low row address strobe for SDRAM memory interface.
$\overline{SOE}$	O/Z	Synchronous memory output enable.
$\overline{ARE}$	O/Z	Active-low read strobe for asynchronous memory interface.
$\overline{SDCAS}$	O/Z	Active-low column address strobe for SDRAM memory interface.
$\overline{SADS/SRE}$	O/Z	Synchronous memory address strobe or read enable (selected by RENEN in CE space secondary control register).
$\overline{AWE}$	O/Z	Active-low write strobe for asynchronous memory interface.
$\overline{SDWE}$	O/Z	Active-low write enable for SDRAM memory interface.
$\overline{SWE}$	O/Z	Synchronous memory write enable.
$\overline{HOLD}$	I	Active-low external bus hold (3-state) request.
$\overline{HOLDA}$	O	Active-low external bus hold acknowledge.
BUSREQ	O	Active-high bus request signal. Indicates pending refresh or memory access.
$\overline{PDT}$	O/Z	Peripheral data transfer data. This signal is active during the data phase of PDT transfers.
SDCKE (1)	O/Z	SDRAM clock enable (used for self-refresh mode). If SDRAM is not in the system, SDCKE can be used as a general-purpose output.

(1) On EMIFA. The data bus width of EMIFA is device specific, either 64-bit (ED[63:0], $\overline{BE[7:0]}$) or 32-bit (ED[31:0], $\overline{BE[3:0]}$).
(2) On EMIFB.
(3) EMIF address numbering for the C64x 32-bit EMIFA begins with EA3 to maintain signal name compatibility with the C64x 64-bit EMIFA.

4.3 Memory Width and Byte Alignment

The C64x DSP has two EMIFs: EMIFA and EMIFB. EMIFA supports memory widths of 8 bits, 16 bits, 32 bits, and 64 bits. EMIFB supports memory widths of 8 bits and 16 bits. Table 4-3 summarizes the addressable memory ranges on the C64x device. Both big and little-endian formats are supported.

Similar to the C621x/C671x EMIF, the C64x EMIF automatically performs packing and unpacking for accesses to external memories of less than the requested transfer length.

Figure 4-3, Figure 4-4, and Figure 4-5 shows the byte lane used on C64x EMIF. The external memory is always right aligned to the ED[7:0] side of the bus. The endianness mode determines whether byte lane 0 (ED[7:0]) is accessed as byte address 0 (little endian) or as byte address N (big endian), where 2^N is memory width in bytes. Similarly, byte lane N is addressed as either byte address 0 (big endian) or as byte address N (little endian).

Table 4-3. Addressable Memory Ranges

Memory type	Memory width[1][2]	Maximum addressable bytes per CE space	Address output on EA[22:3] (EMIFA)[1] EA[20:1] (EMIFB)[2]	Represents
ASRAM	x8	1M	A[19:0]	Byte address
	x16	2M	A[20:1]	Halfword address
	x32	4M	A[21:2]	Word address
	x64	8M	A[22:3]	Doubleword address
Programmable Sync Memory	x8	1M	A[19:0]	Byte address
	x16	2M	A[20:1]	Halfword address
	x32	4M	A[21:2]	Word address
	x64	8M	A[22:3]	Doubleword address
SDRAM	x8	32M	See Section 4.4	Byte address
	x16	64M	See Section 4.4	Halfword address
	x32	128M	See Section 4.4	Word address
	x64	256M	See Section 4.4	Doubleword address

(1) The x64 interface does not apply to the 32-bit EMIFA.
(2) The x32 and x64 interfaces do not apply to EMIFB.

Figure 4-3. Byte Alignment by Endianness - 64-bit

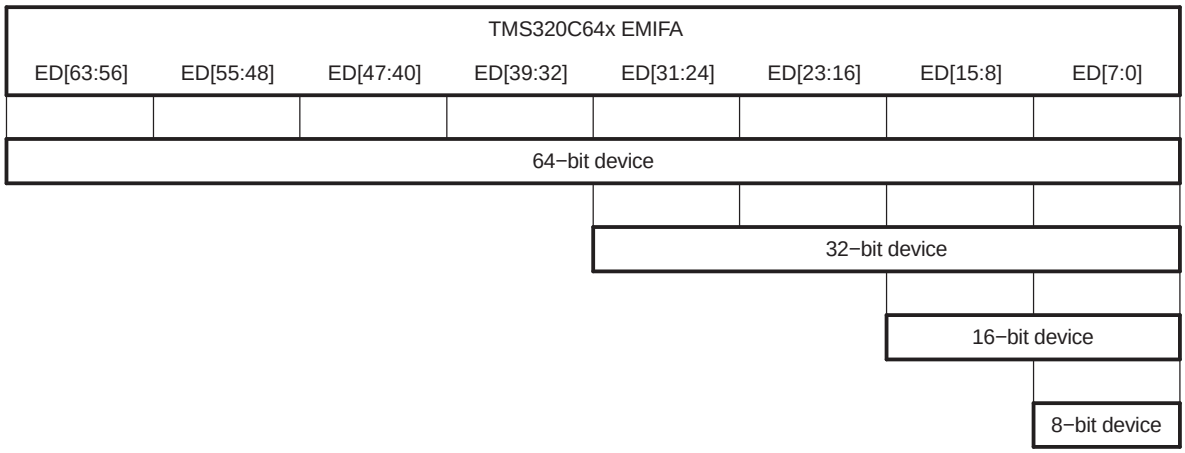


Figure 4-4. Byte Alignment by Endianess - 32-bit

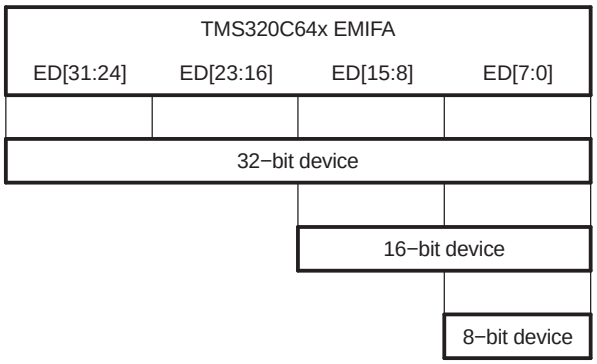
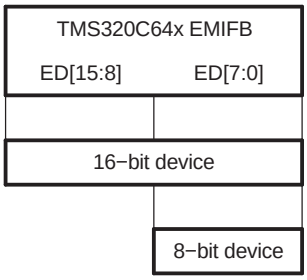


Figure 4-5. Byte Alignment by Endianess - 16-bit



4.4 SDRAM Interface

The C64x EMIF supports SDRAM commands shown in Table 1-2 and Table 1-3 shows the signal truth table for the SDRAM commands. Table 1-4 summarizes the pin connection and related signals specific to SDRAM operation. Table 1-5 summarizes the similarities and differences on the C6000 SDRAM interface.

The 64M-bit SDRAM interface is shown in Figure 4-6. The C64x EMIF allows programming of the addressing characteristics of the SDRAM, including the number of column address bits (page size), row address bits (pages per bank), and banks (maximum number of pages that can be opened). The C64x EMIF can interface to any SDRAM that has 8 to 10 column address pins, 11 to 13 row address pins, and two or four banks. Table 4-4 lists some common SDRAM configurations that interface to the C64x DSP. Other SDRAM configurations are also possible, as long as they are subsets of the column, row, and bank bits supported by the C64x DSP.

The number of EMIF address registers limits the maximum number of open pages. Using this information, the C64x EMIF may simultaneously open up to four pages of SDRAM. The pages can all be in different banks of a single CE space or distributed across multiple CE spaces. Only one page can be open per bank at a time.

In addition, the C64x EMIF supports the SDRAM self-refresh mode, and supports the least recently used (LRU) page replacement strategy instead of random replacement strategy for better performance. See Section 4.4.4 and Section 1.3.2 for details.

Figure 4-6. EMIFA to 64M-Bit SDRAM Interface Block Diagram

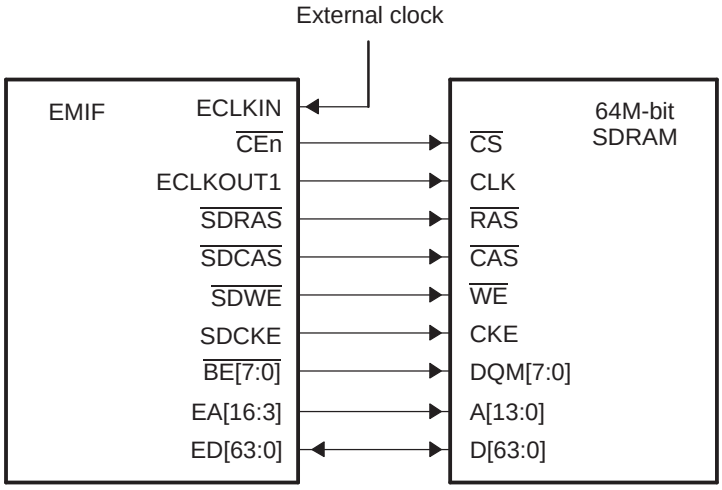


Table 4-4. TMS320C64x DSP Compatible SDRAM

SDRAM Size	B	W	D	Max Devices /CE	Address-able space		Column Address	Row Address	Bank Select	Pre-charge
16M bit	2	″	2M	16	32M	SDRAM	A9-A0	A10-A0	A11	A10
						EMIFA	EA12-EA3	EA13-EA3	EA14	EA13
						EMIFB	EA10-EA1	EA11-EA1	EA12	EA11
	2		1M	8	16M	SDRAM	A8-A0	A10-A0	A11	A10
						EMIFA	EA11-EA3	EA13-EA3	EA14	EA13
						EMIFB	EA9-EA1	EA11-EA1	EA12	EA11
	2	ıı6	512K	4	8M	SDRAM	A7-A0	A10-A0	A11	A10
						EMIFA	EA10-EA3	EA13-EA3	EA14	EA13
						EMIFB	EA8-EA1	EA11-EA1	EA12	EA11
64M bit	4	″	4M	16	128M	SDRAM	A9-A0	A11-A0	A13-A12	A10
						EMIFA	EA12-EA3	EA14-EA3	EA16-EA15	EA13
						EMIFB	EA10-EA1	EA12-EA1	EA14-EA13	EA11
	4		2M	8	64M	SDRAM	A8-A0	A11-A0	A13-A12	A10
						EMIFA	EA11-EA3	EA14-EA3	EA16-EA15	EA13
						EMIFB	EA9-EA1	EA12-EA1	EA14-EA13	EA11
	4	ıı6	1M	4	32M	SDRAM	A7-A0	A11-A0	A13-A12	A10
						EMIFA	EA10-EA3	EA14-EA3	EA16-EA15	EA13
						EMIFB	EA8-EA1	EA12-EA1	EA14-EA13	EA11
	4	′2	512K	2	16M	SDRAM	A7-A0	A10-A0	A12-A11	A10
						EMIFA	EA10-EA3	EA13-EA3	EA15-EA14	EA13
						EMIFB	—	—	—	—
128M bit	4		4M	8	128M	SDRAM	A9-A0	A11-A0	A13-A12	A10
						EMIFA	EA12-EA3	EA14-EA3	EA16-EA15	EA13
						EMIFB	EA10-EA1	EA12-EA1	EA14-EA13	EA11
	4	ıı6	2M	4	64M	SDRAM	A8-A0	A11-A0	A13-A12	A10
						EMIFA	EA11-EA3	EA14-EA3	EA16-EA15	EA13
						EMIFB	EA9-EA1	EA12-EA1	EA14-EA13	EA11
	4	′2	1M	2	32M	SDRAM	A7-A0	A11-A0	A13-A12	A10
						EMIFA	EA10-EA3	EA14-EA3	EA16-EA15	EA13
						EMIFB	—	—	—	—
256M bit	4		8M	8	256M	SDRAM	A9-A0	A12-A0	A14-A13	A10
						EMIFA	EA12-EA3	EA15-EA3	EA17-EA16	EA13
						EMIFB	EA10-EA1	EA13-EA1	EA15-EA14	EA11
	4	ıı6	4M	4	128M	SDRAM	A8-A0	A12-A0	A14-A13	A10
						EMIFA	EA11-EA3	EA15-EA3	EA17-EA16	EA13
						EMIFB	EA9-EA1	EA13-EA1	EA15-EA14	EA11
	4	′2	2M	2	64M	SDRAM	A8-A0	A11-A0	A13-A12	A10
						EMIFA	EA11-EA3	EA14-EA3	EA16-EA15	EA13
						EMIFB	—	—	—	—

Legend: B = Banks; W = Width; D = Depth

Note: Other SDRAM configurations are possible, if the number of column, row, and bank bits are supported by the C64x DSP.

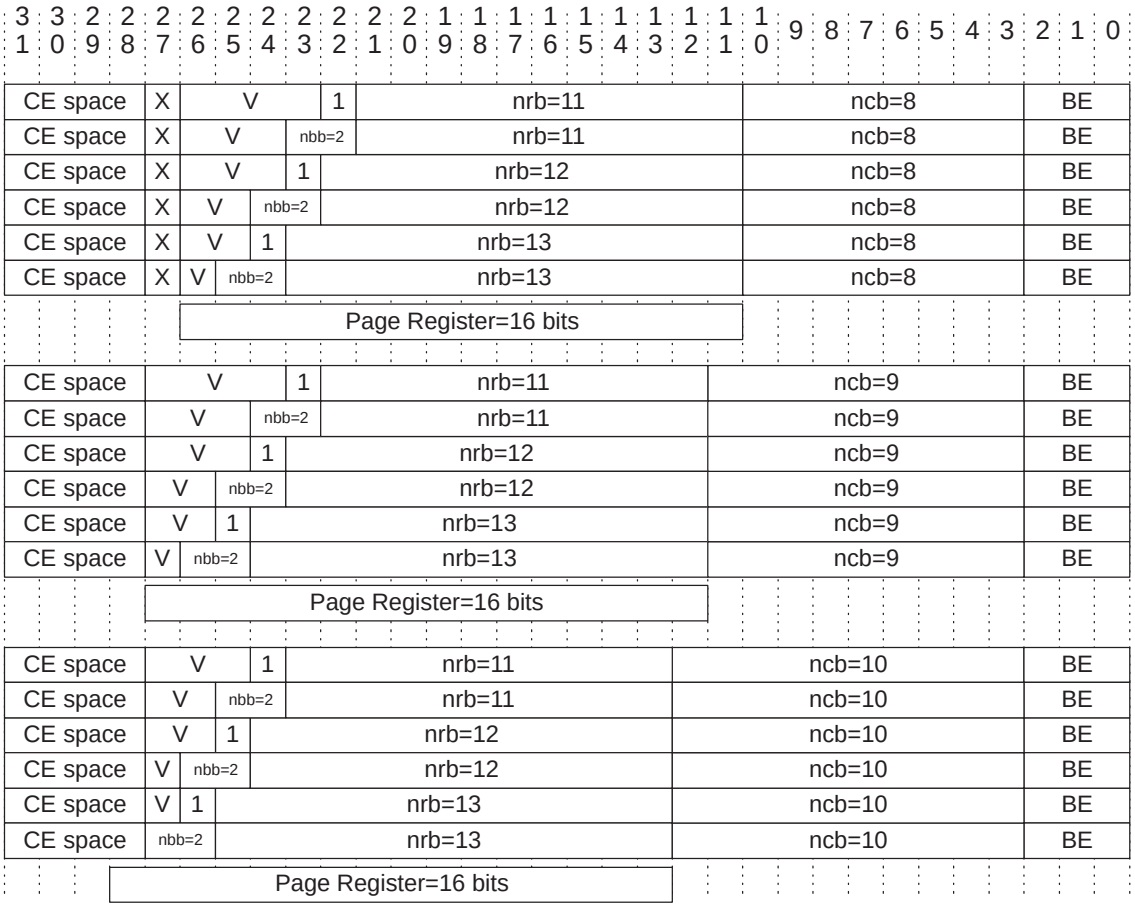
4.4.1 Monitoring Page Boundaries

Similar to the C621x/C671x EMIF, up to four pages of SDRAM can be opened simultaneously with the C64x EMIF SDRAM paging scheme. This can be all in one CE space, or spread across multiple CE spaces. However, the page register always stores 16 bits of address (instead of being limited by the number of row address bits plus the number of bank address bits (NRB + NBB)). Therefore, logical address bits above the bank address bit are used as part of the page comparison. Also, address bits above the bank bits are used when issuing the row/column commands to the external SDRAM. This allows more flexible designs and external visibility into the internal address aliasing. For 32-, 16-, or 8-bit interfaces on EMIFA, the BE portion of the logical address is reduced to 2 bits for 32-bit SDRAM, 1 bit for 16-bit SDRAM, and 0 bits for 8-bit SDRAM. The NCB/NRB/NBB (and page register) shift accordingly.

The C64x EMIF employs a least recently used (LRU) page replacement strategy when necessary. This occurs when the total number of external SDRAM banks (not devices) is greater than 4, since the EMIF only contains four page registers. This can occur when multiple CE spaces of SDRAM are used. When the number of total banks of SDRAM is less than or equal to 4, then the page replacement strategy is fixed since SDRAM requires that only 1 page can be open within a given bank. If the EMIF detects a page miss either during an access where a different page was previously accessed in the same CE space (fixed replacement) or if a page must be closed within a different CE space to allow a page register to be assigned for the current access (LRU replacement), the EMIF performs a DEAC command and starts a new row access.

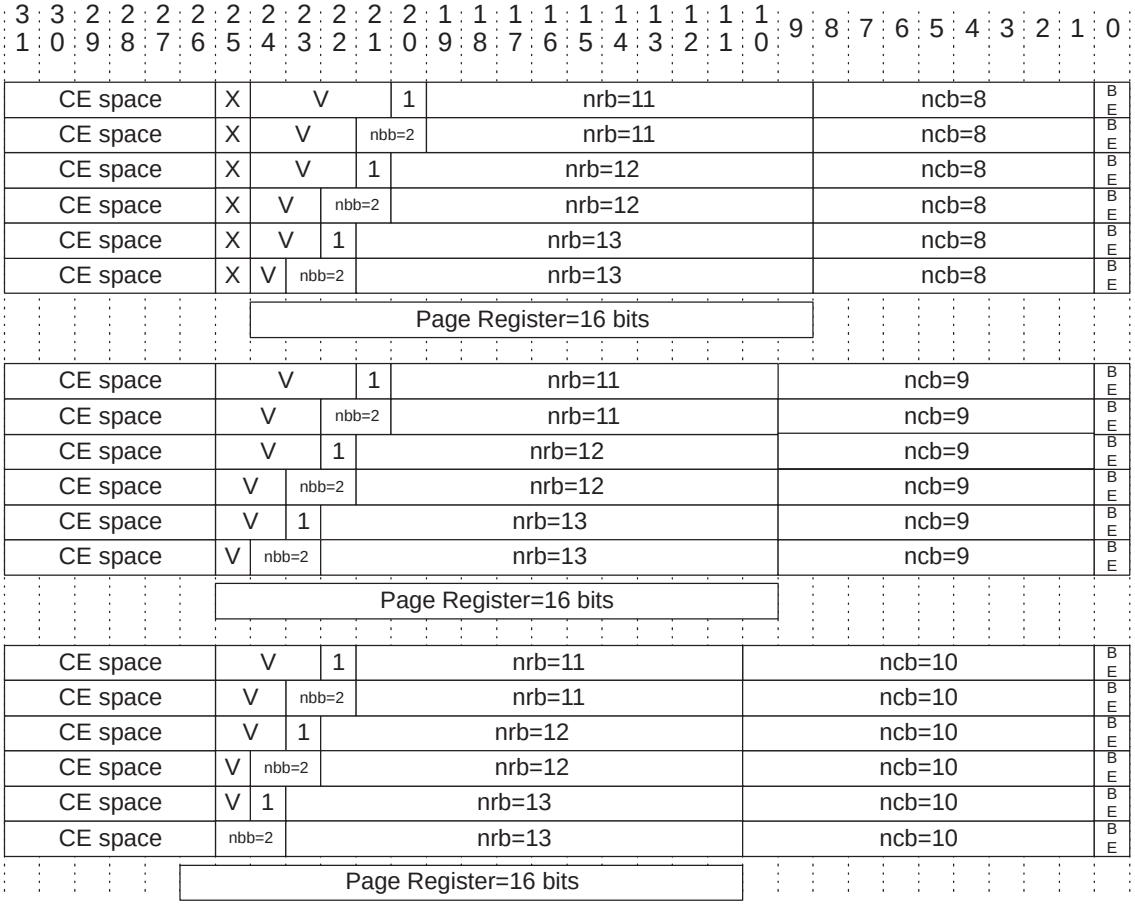
Figure 4-7 details how a 64-bit logical address maps to the page register for EMIFA. Figure 4-8 details how a 16-bit logical address maps to the page register for EMIFB.

Figure 4-7. Logical Address-to-Page Register Mapping for EMIFA



(1) ncb = number of column address bits; nrb = number of row address bits; nbb = number of bank address bits.

Figure 4-8. Logical Address-to-Page Register Mapping for EMIFB



(1) ncb = number of column address bits; nrb = number of row address bits; nbb = number of bank address bits.

4.4.2 Address Shift

The same EMIF pins determine the row and column address, thus the C64x EMIF interface appropriately shifts the address in row and column address selection. Table 4-5 describes the addressing for a 8-, 16-, 32-, and 64-bit-wide SDRAM interface. The 32-bit and 64-bit SDRAM interfaces do not apply to EMIFB.

The following factors apply to the address shifting process:

- The address shift is controlled completely by the column size field (SDCSZ) and is unaffected by the bank and row size fields. The address bits above the bank select bits are used internally to determine whether a page is opened.
- The address bits above the precharge bit (EA[18:14] on EMIFA, and EA[16:12] on EMIFB) are latched internally by the SDRAM controller during a RAS cycle. This ensures that the SDRAM bank select inputs are correct during READ and WRT commands. Thus, the EMIF maintains these values as shown in both row and column addresses.
- EA13 is the precharge pin for EMIFA. EA11 is the precharge pin for EMIFB.

Table 4-5. Byte Address-to-EA Mapping for 8-, 16-, 32-, 64-Bit Interface

			EMIFB																				
			EA 20	EA 19	EA 18	EA 17[1]	EA 16	EA 15	EA 14	EA 13	EA 12	EA 11	EA 10	EA 9	EA 8	EA 7	EA 6	EA 5	EA 4	EA 3	EA 2	EA 1
			EMIFA																				
# of column address bits	Interface bus width	DRAM Cmd	EA 22	EA 21	EA 20	EA 19[1]	EA 18	EA 17	EA 16	EA 15	EA 14	EA 13	EA 12	EA 11	EA 10	EA 9	EA 8	EA 7	EA 6	EA 5	EA 4	EA 3	EA 2	EA 1	EA 0
			A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	A 10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
8	8	$\overline{RAS}$	L	L	L	H/L	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8		
		$\overline{CAS}$	L	L	L	H/L	23[2]	22[2]	21[2]	20[2]	19[2]	L[3]	L	L	7	6	5	4	3	2	1	0		
	16	$\overline{RAS}$	L	L	L	H/L	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9		
		$\overline{CAS}$	L	L	L	H/L	24[2]	23[2]	22[2]	21[2]	20[2]	L[3]	L	L	8	7	6	5	4	3	2	1		
	32	$\overline{RAS}$	L	L	L	H/L	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10		
		$\overline{CAS}$	L	L	L	H/L	25[2]	24[2]	23[2]	22[2]	21[2]	L[3]	L	L	9	8	7	6	5	4	3	2		
	64	$\overline{RAS}$	L	L	L	H/L	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11		
		$\overline{CAS}$	L	L	L	H/L	26[2]	25[2]	24[2]	23[2]	22[2]	L[3]	L	L	10	9	8	7	6	5	4	3		
9	8	$\overline{RAS}$	L	L	L	H/L	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9		
		$\overline{CAS}$	L	L	L	H/L	24[2]	23[2]	22[2]	21[2]	20[2]	L[3]	L	8	7	6	5	4	3	2	1	0		
	16	$\overline{RAS}$	L	L	L	H/L	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10		
		$\overline{CAS}$	L	L	L	H/L	25[2]	24[2]	23[2]	22[2]	21[2]	L[3]	L	9	8	7	6	5	4	3	2	1		
	32	$\overline{RAS}$	L	L	L	H/L	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11		
		$\overline{CAS}$	L	L	L	H/L	26[2]	25[2]	24[2]	23[2]	22[2]	L[3]	L	10	9	8	7	6	5	4	3	2		
	64	$\overline{RAS}$	L	L	L	H/L	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12		
		$\overline{CAS}$	L	L	L	H/L	27[2]	26[2]	25[2]	24[2]	23[2]	L[3]	L	11	10	9	8	7	6	5	4	3		
10	8	$\overline{RAS}$	L	L	L	H/L	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10		
		$\overline{CAS}$	L	L	L	H/L	25[2]	24[2]	23[2]	22[2]	21[2]	L[3]	9	8	7	6	5	4	3	2	1	0		
	16	$\overline{RAS}$	L	L	L	H/L	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11		
		$\overline{CAS}$	L	L	L	H/L	26[2]	25[2]	24[2]	23[2]	22[2]	L[3]	10	9	8	7	6	5	4	3	2	1		
	32	$\overline{RAS}$	L	L	L	H/L	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12		
		$\overline{CAS}$	L	L	L	H/L	27[2]	26[2]	25[2]	24[2]	23[2]	L[3]	11	10	9	8	7	6	5	4	3	2		
	64	$\overline{RAS}$	L	L	L	H/L	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13		
		$\overline{CAS}$	L	L	L	H/L	28[2]	27[2]	26[2]	25[2]	24[2]	L[3]	12	11	10	9	8	7	6	5	4	3		

(1) EA19(EMIFA) and EA17 (EMIFB) are used during ACTV to indicate non-PDT vs. PDT access. For non-PDT access, this bit is 1. For PDT access, this bit is 0 during ACTV.
(2) Bit is internally latched during an ACTV command.
(3) L=Low; logical address A10 is driven low during READ or WRT commands to disable autoprecharge.

4.4.3 SDRAM Refresh Mode

The RFEN bit in the SDRAM control register (SDCTL) enables the SDRAM refresh mode of the C64x EMIF. When RFEN = 0, all EMIF refreshes are disabled, and you must ensure that refreshes are implemented in an external device. When RFEN = 1, the EMIF performs refreshes of SDRAM.

The refresh command (REFR) enables all $\overline{CE}$ signals for all CE spaces selected to use SDRAM (with the MTYPE field of the CE space control register). REFR is automatically preceded by a deactivate (DCAB) command, this ensures that all CE spaces selected with SDRAM are deactivated. Following the DCAB command, the EMIF begins performing trickle refreshes at a rate defined by the PERIOD value in the SDRAM timing register (SDTIM), provided no other SDRAM access is pending.

The system considers REFR requests as high priority, and no distinction exists between urgent and trickle refresh. Transfers in progress are allowed to complete. The SDRAM refresh period has an extra bitfield, XRFR, in SDTIM that controls the number of extra refreshes performed when the counter reaches 0. This feature allows the XRFR field to be set to perform up to four extra refreshes when the refresh counter expires.

4.4.4 SDRAM Self-Refresh Mode

The SLFRFR bit in the SDRAM control register (SDCTL) forces the C64x EMIF to place the external SDRAM in a low-power mode (self refresh), in which the SDRAM maintains valid data while consuming a minimal amount of power. It enters this mode when a 1 is written to the SLFRFR bit and SDRAM exists in the system. When the SLFRFR bit is set, the refresh enable bit (RFEN) in SDCTL must be written with a 0 simultaneously. When the SLFRFR bit is asserted, all open pages of SDRAM are closed (DCAB issued to all CE spaces). In addition, a REFRESH command is issued on the same cycle that the SDCKE signal is driven low.

It is your responsibility to ensure that the SLFRFR bit is turned on/off at appropriate times. To exit SLFRFR mode, write a 0 to the SLFRFR bit and then immediately read back before performing other accesses. As long as SLFRFR = 1, you should ensure that no SDRAM accesses are performed.

During self-refresh mode, the SDRAM clock (ECLKOUT1) can be turned off, if the system does not use the Hold interface or if ECLKOUT1 is not used elsewhere in the system. ECLKOUT1 must be reenabled before exiting self-refresh mode. The EMIF ensures that the SDRAM is in the self-refresh state for at least TRAS cycles, where TRAS is defined in SDEXT. In addition, the EMIF ensures the time from SDCKE high to the next ACTV command is at least 16 ECLKOUT1 cycles.

If SDRAM is not in use in the system, the SDCKE pin can be used as a general-purpose output. The inverse of SLFRFR bit is driven on the SDCKE pin.

If the EMIF detects a Hold request, the EMIF asserts the SDCKE output (as long as TRAS requirement has been met) and clears the SLFRFR bit to wake the SDRAM from reset, before acknowledging this request with HOLDA. If SDRAM is not in use by the system, then Hold has no effect on the state of the SDCKE output or the SLFRFR field.

The effects of the SLFRFR bit with an SDRAM in the system are summarized as follows:

- Write to SLFRFR while not in Hold causes self-refresh mode entry/exit.
- Write to SLFRFR while in Hold: write to SLFRFR is ignored, bit is not written.
- If HOLD request occurs while SLFRFR = 1, the EMIF ensures that the device has been in self-refresh mode at least TRAS cycles. Then the EMIF exits self-refresh mode (deasserts SLFRFR). After 16 ECLKOUT1 cycles, the EMIF acknowledges the HOLD request.

Note: The EMIF SDCKE signal must be connected to the SDRAM CKE signal for proper SLFRFR operation.

4.4.5 Mode Register Set (MRS)

The C64x EMIF uses a mode register value of either 0032h or 0022h. The register value and description are shown in and summarized in Table 4-6. Both values program a default burst length of four words for both reads and writes. The value programmed depends on the CAS latency parameter defined by the TCL field in the SDRAM extension register (SDEXT). If the CAS latency is three (TCL = 1), 0032h is written during the MRS cycle. If the CAS latency is two (TCL = 0), 0022h is written during the MRS cycle. Figure 4-10 shows the timing diagram during execution of the MRS command.

Figure 4-9. Mode Register Value(A)

13	12	11	10	9	8	7
EA16	EA15	EA14	SDA10	EA12	EA11	EA10
Reserved				Write burst length	Reserved	
0000				0	00	

6	5	4	3	2	1	0
EA9	EA8	EA7	EA6	EA5	EA4	EA3
Read latency(B)			S/I	Burst length		
01x			0	010		

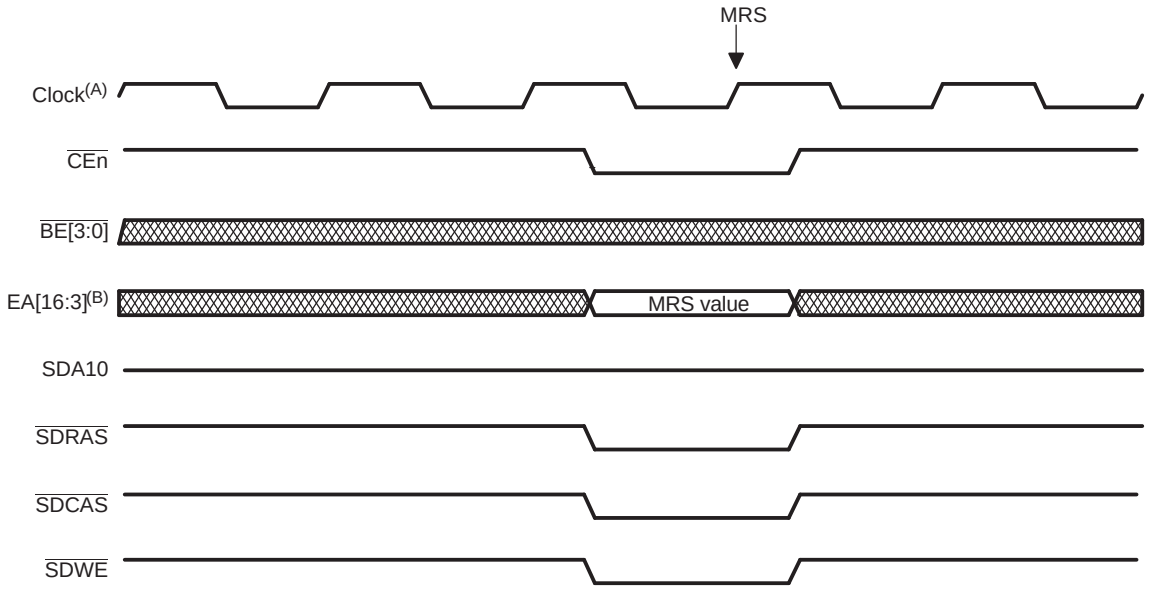
(A) For EMIFB, EA[14:1] are used.

(B) If TCL = 0, bit 4 is 0; if TCL = 1, bit 4 is 1.

Table 4-6. Implied SDRAM Configuration by MRS Command

Bit	Field	Selection
9	Write burst length	4 words
6-4	Read latency	If TCL = 0, 2 cycles If TCL = 1, 3 cycles
3	Serial/interleave burst type	Serial
2-0	Burst length	4 words

Figure 4-10. SDRAM Mode Register Set: MRS Command Timing Diagram



A Clock = ECLKOUT1.

B For EMIFB, EA[14:1] are used.

4.4.6 Timing Requirements

Several SDRAM timing parameters decouple the EMIF from SDRAM speed limitations. The C64x EMIF has additional timing parameters that are programmable using the SDRAM control register (SDCTL) and the SDRAM extension register (SDEXT), as shown in Table 4-7. Consult the SDRAM data sheet for information on the appropriate parameters for a specific SDRAM.

The C64x EMIF also allows you to program other functional parameters of the SDRAM controller, listed in Section 4.8.6. These parameters are not explicitly spelled out in the timing parameters of a data sheet, but you must ensure that the parameters are programmed to a valid value. Table 4-8 shows the recommended values for these SDRAM parameters.

Table 4-7. SDRAM Timing Parameters

Parameter	Description	Value in EMIF clock cycles[1]
t_{RC}	REFR command to ACTV, MRS, or subsequent REFR command	TRC + 1
t_{RCD}	ACTV command to READ or WRT command	TRCD + 1
t_{RP}	DCAB/DEAC command to ACTV, MRS, or REFR command	TRP + 1
t_{CL}	CAS latency of the SDRAM	TCL + 2
t_{RAS}	ACTV command to DEAC/DCAB command	TRAS + 1
t_{RRD}	ACTV bank A to ACTV bank B (same CE space)	TRRD + 2
t_{WR}	Write recovery, time from last data out of C6000 DSP (write data) to DEAC/DCAB command	TWR + 1
t_{HZP}	High Z from precharge, time from DEAC/DCAB to SDRAM outputs (read data) in high Z	THZP + 1

(1) EMIF clock cycles = ECLKOUT1 cycles.

Table 4-8. Recommended Values for Command-to-Command Parameters

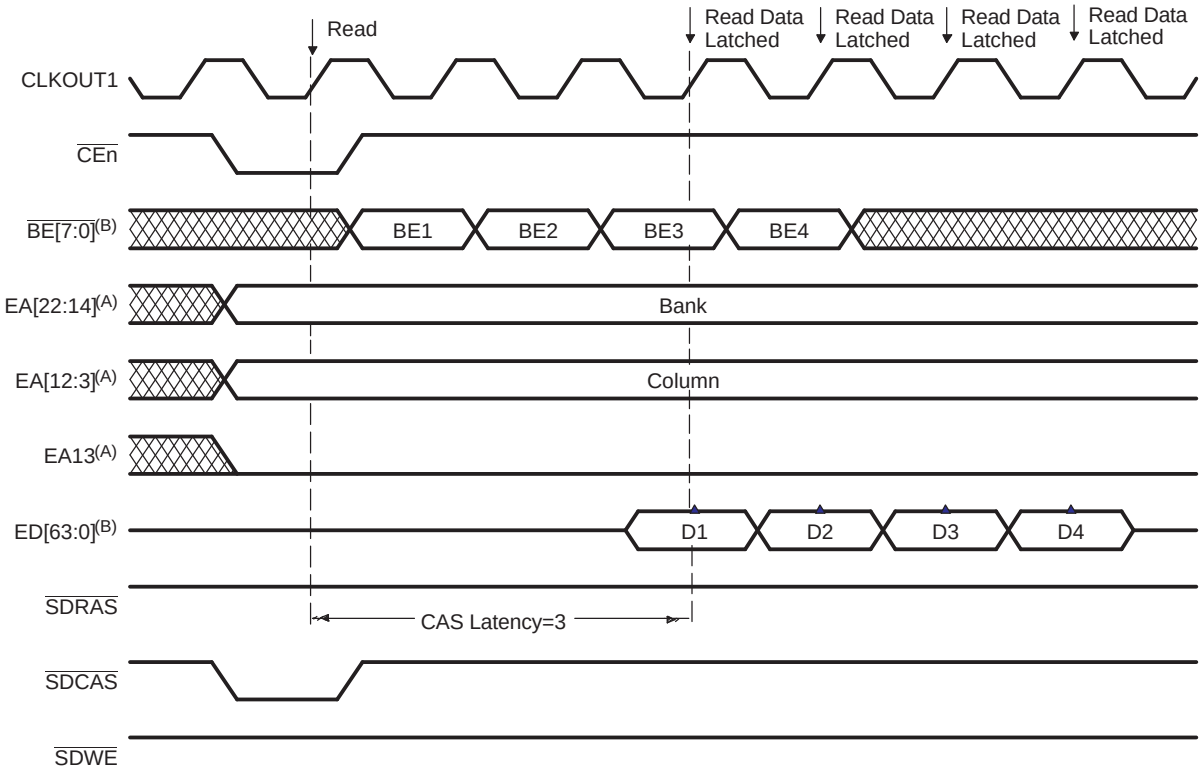
Parameter	Description	Value in EMIF clock cycles[1]	Suggested value for TCL = 0	Suggested value for TCL = 1
READ to READ	READ command to READ command. Used to interrupt a READ burst for random READ addresses.	RD2RD + 1	RD2RD = 0	RD2RD = 0
READ to DEAC	Used in conjunction with t_{HZP}. Specifies the minimum amount of time between READ command and DEAC/DCAB command.	RD2DEAC + 1	RD2DEAC = 1	RD2DEAC = 1
READ to WRITE	READ to WRITE command. The value programmed in this parameter depends on t_{CL}. READ to WRITE should be CAS latency plus 2 cycles (in EMIF clock cycles) to provide 1 turnaround cycle before WRITE command.	RD2WR + 1	RD2WR = 3	RD2WR = 4
BEx high before write interrupting read	Specifies the number of cycles that the BEx outputs should be high before a write is allowed to interrupt a read. This is related to READ to WRITE parameter.	R2WDQM + 1	R2WDQM = 1	R2WDQM = 2
WRITE to WRITE	Number of cycles between a WRITE interrupting a WRITE. Used for random WRITES.	WR2WR + 1	WR2WR = 0	WR2WR = 0
WRITE to DEAC	Number of cycles between a WRITE command and a DEAC/DCAB command.	WR2DEAC + 1	WR2DEAC = 1	WR2DEAC = 1
WRITE to READ	Number of cycles between a WRITE command and a READ command.	WR2RD + 1	WR2RD = 0	WR2RD = 0

(1) EMIF clock cycles = ECLKOUT1 cycles.

4.4.7 SDRAM Read

Figure 4-11 shows the C64x EMIF performing a three doubleword (EMIFA) or halfword (EMIFB) read burst from SDRAM. The EMIF uses a burst length of four, and has a programmable $\overline{CAS}$ latency of either two or three cycles. The CAS latency is three cycles in this example (CASL = 1). Since the default burst length is four words, the SDRAM returns four pieces of data for every read command. If no additional accesses are pending to the EMIF, as in Figure 4-11, the read burst completes and the unneeded data is disregarded. If accesses are pending, the read burst can be interrupted with a new command (READ, WRT, DEAC, DCAB) controlled by the SDRAM extension register. If a new access is not pending, the system does not perform the DCAB/DEAC command until the page information becomes invalid.

Figure 4-11. SDRAM Read Timing Diagram



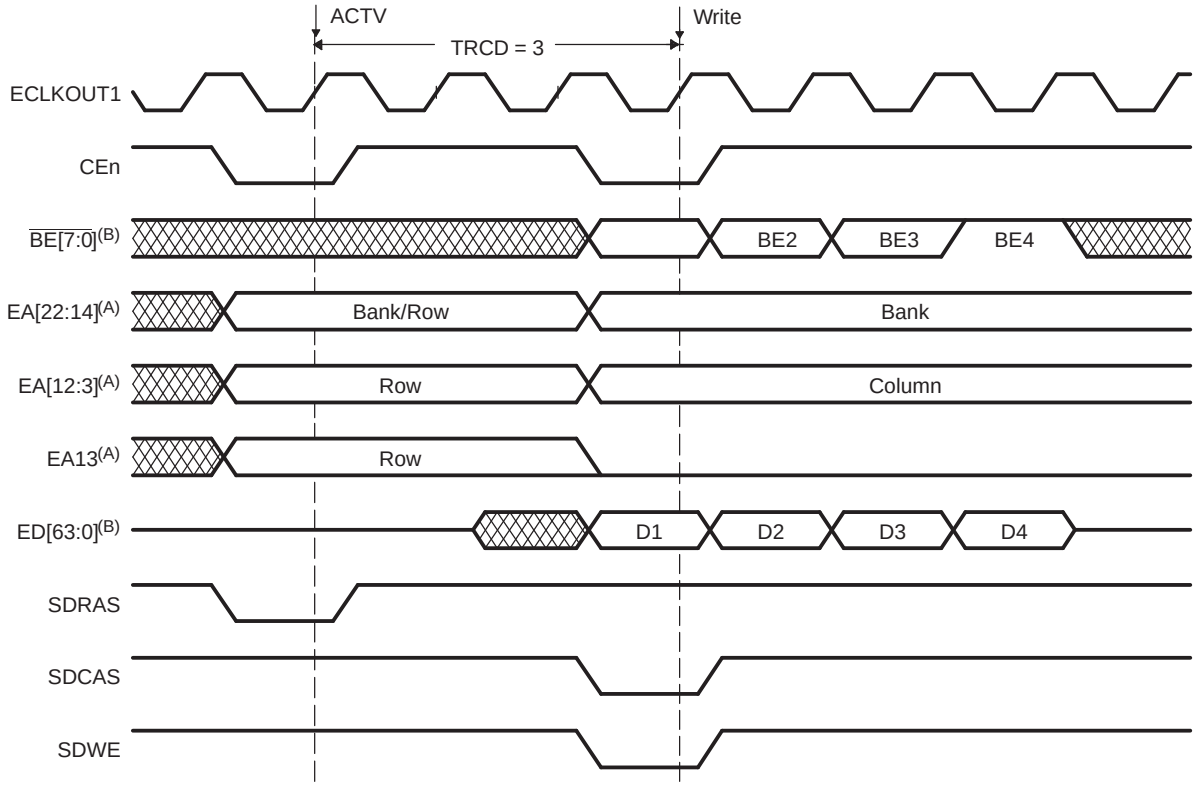
A For EMIFB: $\overline{BE[1:0]}$, EA[20:12], EA[10:1], EA11, and ED[15:0] are used.

B For 32-bit EMIFA: $\overline{BE[3:0]}$ and ED[31:0] are used.

4.4.8 SDRAM Write

All SDRAM writes have a burst length of four on the C64x EMIF. The bank is activated with the row address during the ACTV command. Writes have no latency, so data is output on the same cycle as the column address. Writes to particular bytes are disabled using the appropriate DQM inputs; this feature allows for byte and halfword writes. Figure 4-12 shows the timing for a three doubleword (EMIFA) or halfword (EMIFB) write on the C64x EMIF. Since the default write-burst length is four words, the last write is masked out using the byte enable signals. On the EMIF, idle cycles are inserted as controlled by the parameters of the SDRAM extension register fields (WR2RD, WR2DEAC, WR2WR, TWR). A DEAC command then deactivates the bank, and the memory interface can begin a new page access. If no new access is pending, the EMIF does not perform the DEAC command until the page information becomes invalid (see Section 4.4.1). The values on the bank select bits (see Section 4.4.2) during column accesses and during the DEAC command are the values latched during the ACTV command.

Figure 4-12. SDRAM Write Timing Diagram



A For EMIFB: $\overline{BE[1:0]}$, EA[20:12], EA[10:1], EA11, and ED[15:0] are used.

B For 32-bit EMIFA:$\overline{BE[3:0]}$ and ED[31:0] are used.

4.5 Programmable Synchronous Interface

The C64x EMIF offers additional flexibility by replacing the SBSRAM interface with a programmable synchronous interface. The programmable synchronous interface supports glueless interfaces to the following devices:

- Pipelined and flow-through SBSRAM
- Zero bus turnaround (ZBT) synchronous pipeline SRAM
- Synchronous FIFOs in standard and first word fall through (FWFT) mode

The programmable synchronous interface is configured by the CE space secondary control register (CESEC). The bit fields in CESEC control the cycle timing and the clock used for programmable synchronous interface synchronization. SeeSection 4.8.3 for a description of CESEC.

Table 4-9 shows the programmable synchronous interface pins.

Table 4-9. Programmable Synchronous Pins

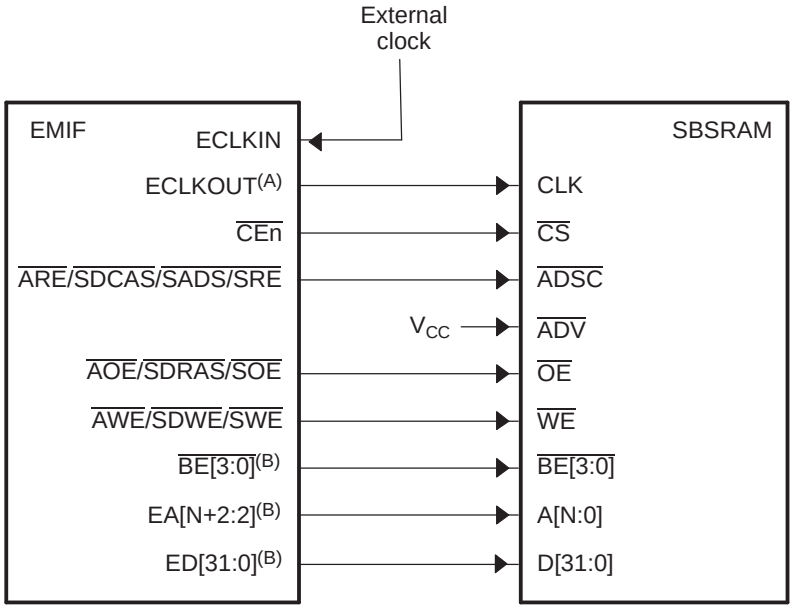
EMIF Signal	Signal Function
$\overline{\text{SADS}}$/$\overline{\text{SRE}}$	Address strobe/read enable (selected by RENEN).
$\overline{\text{SOE}}$	Output enable.
$\overline{\text{SOE3}}$	Output enable for $\overline{\text{CE3}}$. The $\overline{\text{SOE3}}$ pin is not muxed with other signals. (useful for glueless FIFO interface)
$\overline{\text{SWE}}$	Write enable.
ECLKOUT1	Synchronous interface clock, runs at 1ıEMIF input clock rate.
ECLKOUT2	Synchronous interface clock, runs at 1 1/2 or 1/4ıEMIF input clock rate.

4.5.1 SBSRAM Interface

The programmable synchronous mode supports SBSRAM interface, shown in Figure 4-13. In order to support different synchronous memory types, the C64x SBSRAM interface combines the C620x/C670x EMIF and C621x/C671x EMIF interfaces. The C64x interface does not explicitly make use of the burst mode of the SBSRAM. Instead, the C64x EMIF performs SBSRAM bursts by issuing a new command every cycle (similar to the C620x/C670x EMIF). At the end of a burst where no accesses are pending in that CE space, the C64x EMIF issues a deselect cycle (similar to the C621x/C671x EMIF). The RENEN field in CESEC should be cleared to 0 for SBSRAM interface to enable the $\overline{\text{SADS}}$ signal.

The EMIF also supports programmable read and write latency to allow a flexible interface to different types of synchronous memories.

Figure 4-13. EMIF to SBSRAM Interface Block Diagram



A ECLKOUTn used is selected by the SNCCLK bit in CESEC.

B For interface to a 64-bit data bus: $\overline{\text{BE[7:0]}}$, EA[all], and ED[63:0] are used.
For interface to a 32-bit data bus: $\overline{\text{BE[3:0]}}$, EA[all], and ED[31:0] are used.
For interface to a 16-bit data bus: $\overline{\text{BE[1:0]}}$, EA[all], and ED[15:0] are used.

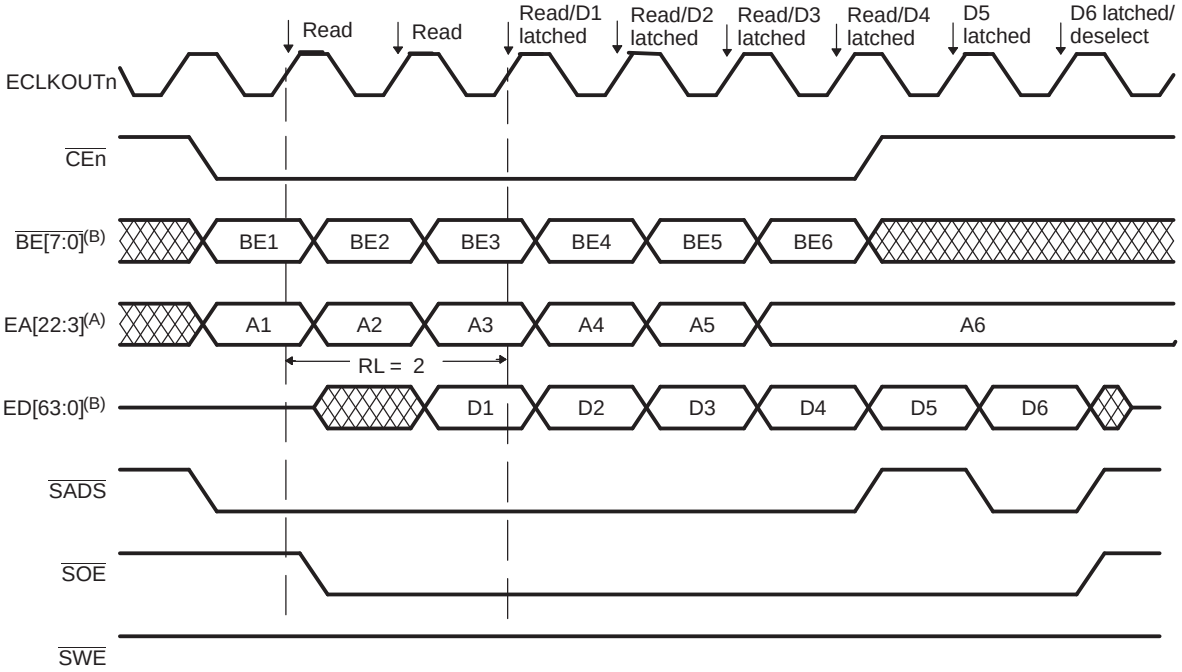
4.5.1.1 SBSRAM Read

Figure 4-14 shows a six-element (doubleword for EMIFA, halfword for EMIFB) read with a two-cycle read latency of an SBSRAM for the C64x EMIF. Every access strobes a new address into the SBSRAM, indicated by the $\overline{\text{SADS}}$ strobe low. The EMIF issues a deselect cycle at the end of the burst transfer.

For the standard SBSRAM interface, the following fields in CESEC must be set to their default state:

- SYNCRL = 10b; 2 cycle read latency
- SYNCWL = 00b; 0 cycle write latency
- CEEXT = 0; CE goes inactive after the final command has been issued
- RENEN = 0; $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ signal acts as $\overline{\text{SADS}}$ signal

Figure 4-14. SBSRAM Six-Element Read Timing Diagram



A For EMIFB: $\overline{\text{BE[1:0]}}$, EA[20:1], and ED[15:0] are used.

B For 32-bit EMIFA: $\overline{\text{BE[3:0]}}$ and ED[31:0] are used.

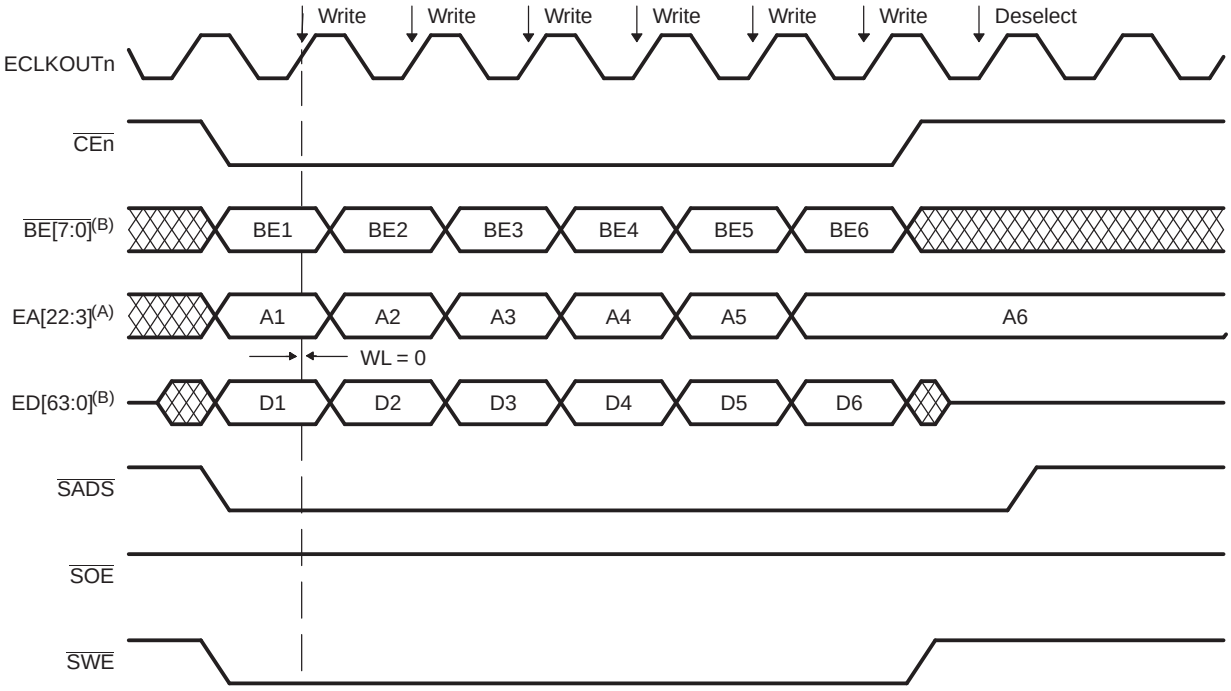
4.5.1.2 SBSRAM Write

Figure 4-15 shows a six-element (doubleword for EMIFA, halfword for EMIFB) write to SBSRAM. Every access strobes a new address into the SBSRAM. The C64x EMIF issues a deselect cycle at the end of the burst transfer.

For the standard SBSRAM interface, the following fields in CESEC must be set to their default state:

- SYNCRL = 10b; 2 cycle read latency
- SYNCWL = 00b; 0 cycle write latency
- CEEXT = 0; CE goes inactive after the final command has been issued
- RENEN = 0; $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ signal acts as $\overline{\text{SADS}}$ signal

Figure 4-15. SBSRAM Six-Element Write Timing Diagram



A For EMIFB, $\overline{\text{BE[1:0]}}$, EA[20:1], and ED[15:0], respectively, are used instead.

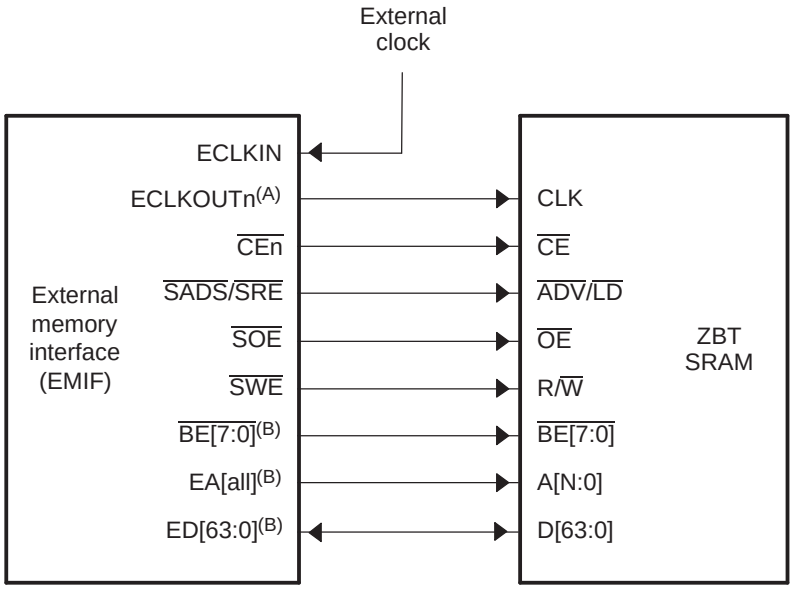
B For 32-bit EMIFA: $\overline{\text{BE[3:0]}}$ and ED[31:0] are used.

4.5.2 Zero Bus Turnaround (ZBT) SRAM Interface

The programmable synchronous mode supports zero bus turnaround (ZBT) SRAM interface shown in Figure 4-16. For ZBT SRAM interface, the following fields in CESEC must be set:

- SYNCRL = 10b; 2 cycle read latency
- SYNCWL = 10b; 2 cycle write latency
- CEEXT = 0; CE goes inactive after the final command has been issued
- RENEN = 0; $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ signal acts as $\overline{\text{SADS}}$ signal.

Figure 4-16. EMIF to Zero Bus Turnaround (ZBT) SRAM Interface Block Diagram



A ECLKOUT*n* used is selected by the SNCCLK bit in the CESEC*n* register.

B The MTYPE field selects the interface to be 8-, 16-, 32-, or 64-bits wide.
For 32-bit interface, $\overline{\text{BE}}$[3:0], EA[all], and ED[31:0] are used.
For 16-bit interface, $\overline{\text{BE}}$[1:0], EA[all], and ED[15:0] are used.

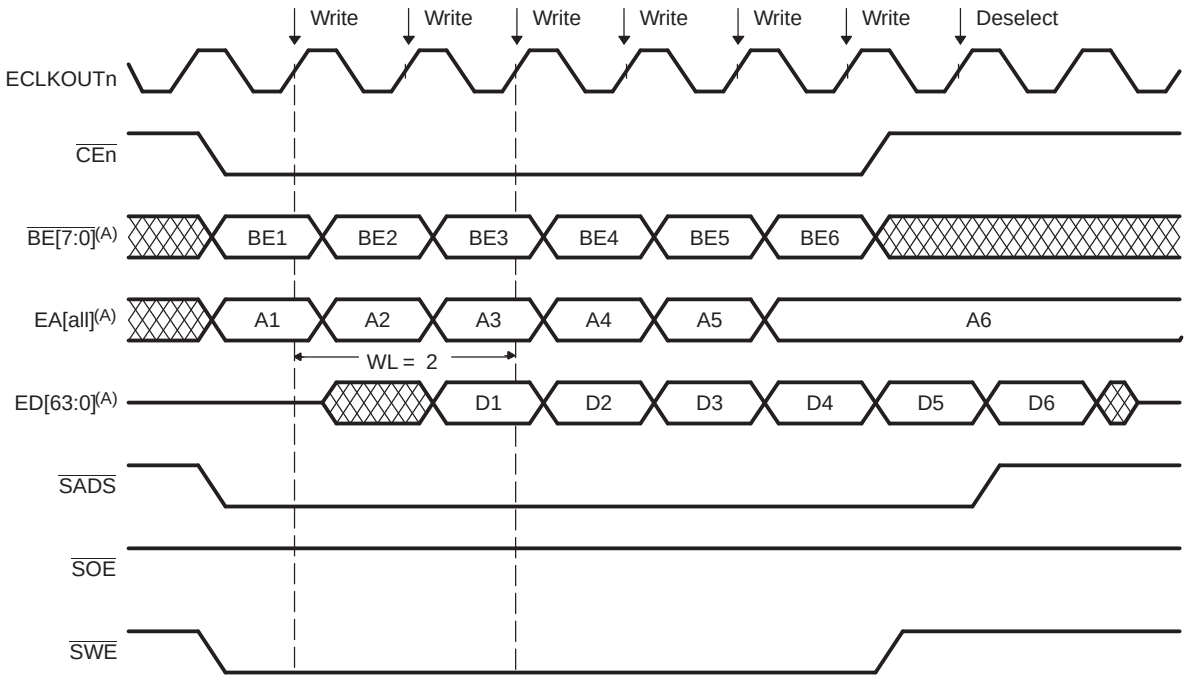
4.5.2.1 ZBT SRAM Read

The ZBT SRAM read waveforms are identical to the SBSRAM read waveforms, since the register settings corresponding to the reads are the same. Refer to Section 4.5.1.1 for details.

4.5.2.2 ZBT SRAM Write

For ZBT SRAM writes, the control signal waveforms are exactly the same as standard SRAM writes. The write data, however, is delayed by two cycles, as controlled by SYNCWL = 10b. Figure 4-17 shows the ZBT SRAM write timing.

Figure 4-17. Zero Bus Turnaround (ZBT) SRAM Six-Element Write Timing Diagram



A Figure shows 64-bit interface. The MTYPE field selects the interface type to be 8-, 16-, 32-, or 64-bits wide.
For 32-bit interface, BE[3:0], EA[all], and ED[31:0] are used.
For 16-bit interface, BE[1:0], EA[all], and ED[15:0] are used.

4.5.3 Synchronous FIFO Interface

The programmable synchronous mode supports both standard timing synchronous FIFO interface and first word fall through (FWFT) FIFO interface. For synchronous FIFO interface, set the following field in CESEC:

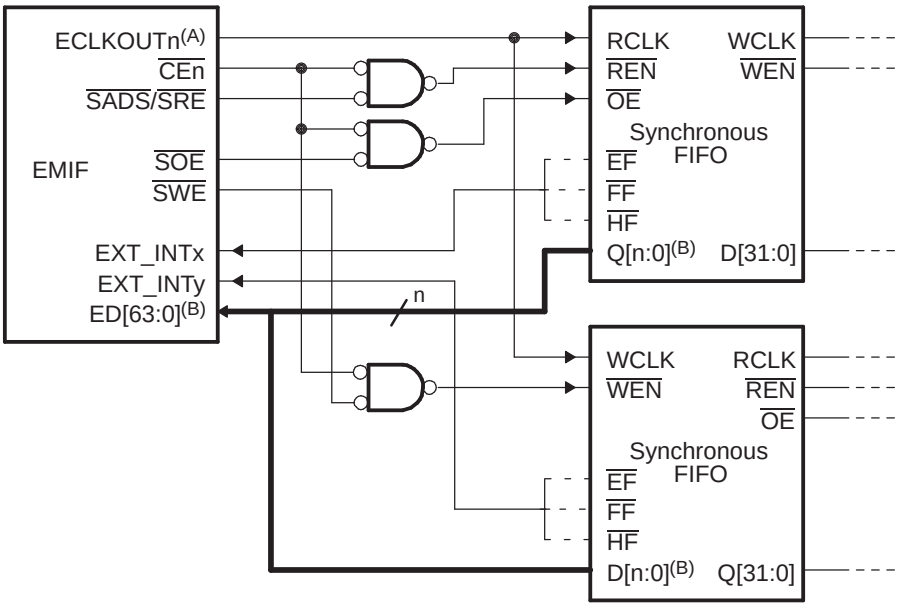
- RENEN = 1; $\overline{\text{SADS}}/\overline{\text{SRE}}$ signal acts as $\overline{\text{SRE}}$ signal

Figure 4-18 shows the synchronous FIFO interface with glue. Figure 4-19 and Figure 4-20 show the glueless synchronous FIFO interface at CE3 space, using the dedicated $\overline{\text{SOE3}}$ pin.

Care must be taken when implementing glueless synchronous FIFO interface:

- For glueless synchronous FIFO read interface in CE3 space (Figure 4-19), writes to CE3 must not be performed. Internally, $\overline{\text{SOE3}}$ = $\overline{\text{CE3}}$ OR $\overline{\text{SOE}}$. Performing a write causes $\overline{\text{CE3}}$ and $\overline{\text{SOE3}}$ to go active, hence $\overline{\text{REN}}$ and $\overline{\text{OE}}$ will be active. Data contention will occur on the ED bus since both DSP and FIFO will be driving data at the same time.
- For glueless synchronous FIFO write interface in any CE space (Figure 4-20), reads must not be performed. Reads cause $\overline{\text{CEn}}$ signal to go active; therefore, FIFO data corruption will occur since FIFO expects data from DSP.

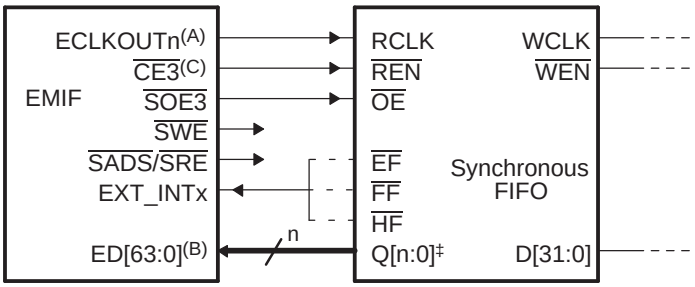
Figure 4-18. Read and Write Synchronous FIFO Interface With Glue Block Diagram



A ECLKOUT used is selected by the SNCCLK bit in CESEC.

B The MTYPE field selects the interface to be 8-, 16-, 32-, or 64-bits wide. For EMIFB, only 8-bit and 16-bit interfaces are available; therefore, only ED[15:0] is used. For 32-bit EMIFA, only 8-bit, 16-bit, and 32-bit interfaces are available; therefore, only ED[31:0] is used.

Figure 4-19. Glueless Synchronous FIFO Read Interface in CE3 Space Block Diagram

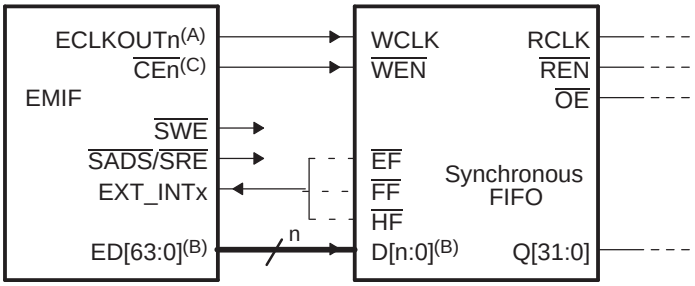


A ECLKOUT used is selected by the SNCCLK bit in CESEC.

B The MTYPE field selects the interface to be 8-, 16-, 32-, or 64-bits wide. For EMIFB, only 8-bit and 16-bit interfaces are available, therefore, only ED[15:0] is used. For 32-bit EMIFA, only 8-bit, 16-bit, and 32-bit interfaces are available; therefore, only ED[31:0] is used.

C Do not perform writes to CE3 in this interface, because writes to CE3 will also cause CE3 to go active, causing data contention.

Figure 4-20. Glueless Synchronous FIFO Write Interface Block Diagram



A ECLKOUT used is selected by the SNCCLK bit in CESEC.

B The MTYPE field selects the interface to be 8-, 16-, 32-, or 64-bits wide. For EMIFB, only 8- and 16-bit interfaces are available. Therefore only ED[15:0] is used. For 32-bit EMIFA, only 8-bit, 16-bit, and 32-bit interfaces are available; therefore, only ED[31:0] is used.

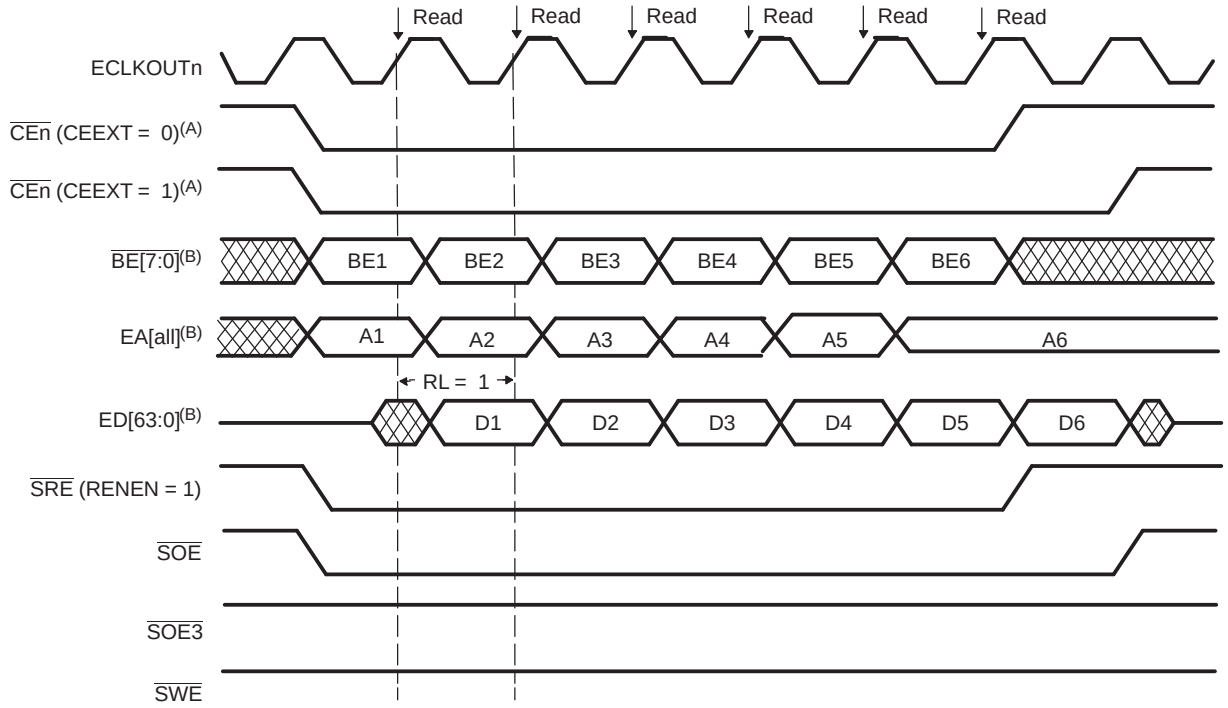
C Do not perform reads to CEn in this interface, because reads cause $\overline{\text{CEn}}$ to go active, causing FIFO data corruption.

4.5.3.1 Standard Synchronous FIFO Read

Figure 4-21 and Figure 4-22 show a six-word read from a standard synchronous FIFO. The CESEC settings are:

- SYNCRL = 01b; one cycle read latency
- RENEN = 1; $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ signal acts as $\overline{\text{SRE}}$ signal
- CEEXT = 0; used for glueless FIFO interface
  CEEXT = 1; used for FIFO interface with glue

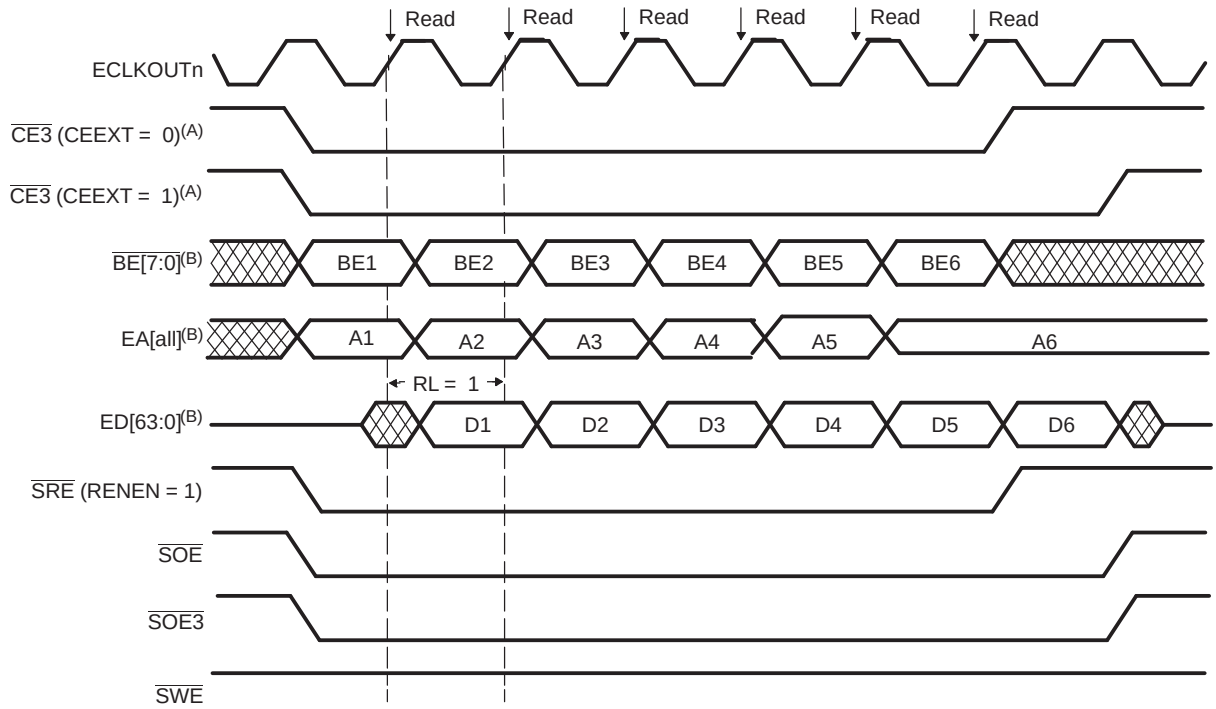
Figure 4-21. Standard Synchronous FIFO Read Timing Diagram (CE0, CE1, or CE2)



A CEEXT = 0 for glueless synchronous FIFO interface. CEEXT = 1 for interface with glue.

B Figure shows 64-bit interface. The MTYPE field selects the interface type to be 8-, 16-, 32-, or 64-bits wide.
For 32-bit interface, $\overline{\text{BE}}$[3:0], EA[all], and ED[31:0] are used.
For 16-bit interface, $\overline{\text{BE}}$[1:0] , EA[all], and ED[15:0] are used.

Figure 4-22. Standard Synchronous FIFO Read Timing Diagram (CE3 only)



A CEEXT = 0 for glueless synchronous FIFO interface. CEEXT = 1 for interface with glue.

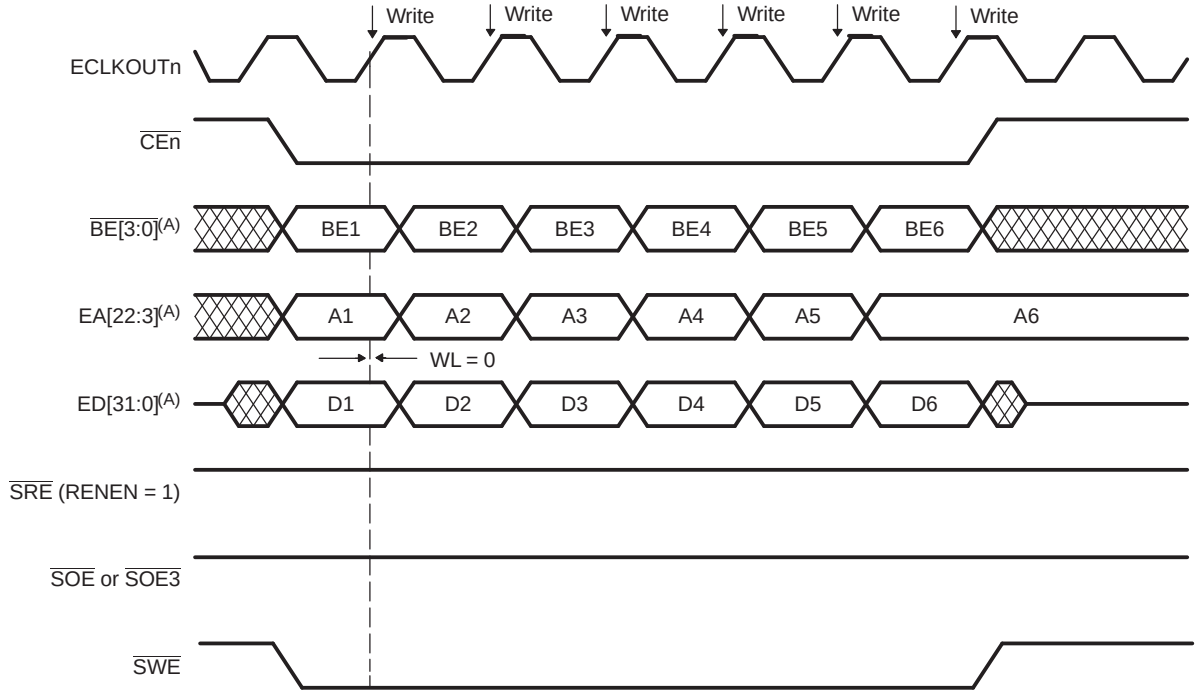
B Figure shows 64-bit interface. The MTYPE field selects the interface type to be 8-, 16-, 32-, or 64-bits wide.
For 32-bit interface, $\overline{BE[3:0]}$, EA[all], and ED[31:0] are used.
For 16-bit interface, $\overline{BE[1:0]}$, EA[all], and ED[15:0] are used.

4.5.3.2 Standard Synchronous FIFO Write

Figure 4-23 shows a six-word write to a standard synchronous FIFO. The CESEC settings are:

- SYNCWL = 00b; zero cycle write latency
- RENEN = 1; $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ signal acts as $\overline{\text{SRE}}$ signal

Figure 4-23. Standard Synchronous FIFO Write Timing Diagram



A For EMIFB:$\overline{\text{BE[1:0]}}$, EA[21:1], and ED[15:0] are used.

4.5.3.3 First Word Fall Through (FWFT) Synchronous FIFO Write

The first word fall through (FWFT) synchronous FIFO write timing is identical to the standard synchronous FIFO write timing, see Section 4.5.3.2.

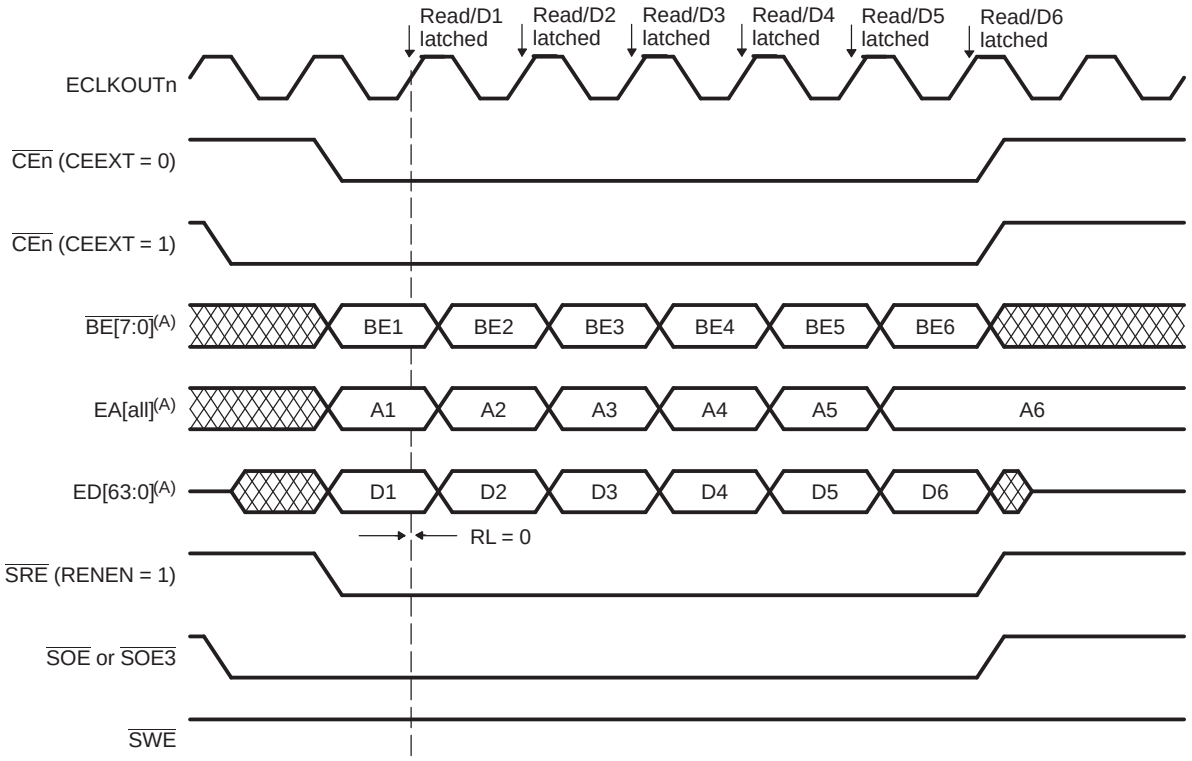
4.5.3.4 First Word Fall Through (FWFT) Synchronous FIFO Read

Figure 4-24 shows a six-word read from a first word fall through (FWFT) synchronous FIFO. The CESEC settings are:

- SYNCRL = 00b; zero cycle read latency
- RENEN = 1; $\overline{\text{SADS}}$/$\overline{\text{SRE}}$ signal acts as $\overline{\text{SRE}}$ signal
- CEEXT = 0; used for glueless FIFO interface
  CEEXT = 1; used for FIFO interface with glue

SYNCRL = 0 causes the $\overline{\text{SOE}}$ (or $\overline{\text{SOE3}}$) signal active a cycle before the read command begins. If CEEXT = 1, the $\overline{\text{CE}}$ signal goes active at the same time as the $\overline{\text{SOE}}$ signal.

Figure 4-24. First Word Fall Through (FWFT) Synchronous FIFO Read Timing Diagram



A For EMIFB: [$\overline{\text{BE[1:0]}}$, EA[21:1], and ED[15:0] are used.
This figure shows a 64-bit interface. The MTYPE field selects the interface type to be 8-, 16-, 32-, or 64-bits wide.
For 32-bit interface, $\overline{\text{BE[3:0]}}$, EA[all], and ED[31:0] are used.
For 16-bit interface, $\overline{\text{BE[1:0]}}$, EA[all], and ED[15:0] are used.

4.6 Peripheral Device Transfer (PDT)

To perform a peripheral device transfer (PDT), the PDTS or PDTD bits in the EDMA options parameter must be appropriately set (see the *TMS320C6000 DSP Enhanced DMA (EDMA) Controller Reference Guide* (SPRU234) for details). A PDT allows you to directly transfer data from an external peripheral (such as a FIFO) to another external memory (such as SDRAM), and conversely. Normally, this type of transfer would require an EMIF read of a peripheral followed by an EMIF write to memory, or an EMIF read of a memory followed by an EMIF write to a peripheral.

In a typical system, however, both the peripheral and memory are connected to the same physical data pins, and thus can be optimized. In a PDT write transfer, the peripheral directly drives the data, and writes it to the memory in the same bus transaction. In a PDT read transfer, the memory directly drives the data, and writes it to the peripheral in the same bus transaction. Typically, the memory device will be mapped to an addressable location via a $\overline{\text{CE}}$n signal. Normally, the peripheral device is not memory mapped (it does not use a $\overline{\text{CE}}$n signal). It is activated with the PDT signal and, optionally, a combination of other control signals (via external logic).

PDT transfers are classified in terms of the memory on the EMIF. A PDT write is a transfer from a peripheral to memory (memory is physically written). A PDT read is a transfer from memory to a peripheral (memory is physically read). For a PDT read, the EMIF ignores the read data on the external bus. For a PDT write, the EMIF data bus is placed in a high-impedance state during the transaction to allow the external peripheral or memory to drive the data bus. A PDT transfer is only supported when the external memory is SDRAM (specified by the MTYPE field in the CE space control register). PDT transfers should not be performed to non-SDRAM CE spaces.

In a PDT transaction, the EMIF:

1. Generates normal SDRAM read bus cycles for a PDT read, or generates normal SDRAM write bus cycles for a PDT write. For example, for a PDT read from CE0 configured as SDRAM, the EMIF asserts CE0 and generates the SDRAM read control signals. The EMIF does not explicitly generate the control signals to the destination peripheral in a PDT read. For a PDT write to CE0 with an SDRAM, the EMIF asserts CE0 and generates the SDRAM write control signals. The EMIF does not explicitly generate the control signals to the source in a PDT write.
2. Generates PDT control signal ($\overline{\text{PDT}}$) and the PDT address pins. $\overline{\text{PDT}}$ is asserted low 0, 1, 2, or 3 cycles prior to the data phase of the transaction. The PDTWL and PDTRL fields in the PDT control register (PDTCTL) control the latency of the $\overline{\text{PDT}}$ signal for write and read transfers, respectively (see Section 4.8.7).
3. In addition to the direct control provided by the $\overline{\text{PDT}}$ signal, the EMIF uses two upper-address pins ($\overline{\text{PDTA}}$ and PDTDIR) during a PDT transfer. Table 4-10 describes each of these signals, listing their appropriate EMIF and SDRAM pin and their function.
4. Drives EMIF data outputs (ED pins) to a high-impedance state.

Table 4-10. Peripheral Device Transfer (PDT) Signal Description

	EMIFA		EMIFB		
Pin Name	**64-bit[1]**	**32-bit[1]**	**16-bit[1]**	**SDRAM**	**Function**
$\overline{\text{PDTA}}$	EA19	EA18	EA17	A16	PDT access
PDTDIR	EA20	EA19	EA18	A17	PDT read, not write
$\overline{\text{PDT}}$	$\overline{\text{PDT}}$	$\overline{\text{PDT}}$	$\overline{\text{PDT}}$	-	PDT data

(1) Refers to the maximum bus width of the EMIF and not the size of the transfer.

During a PDT transfer, the EMIF drives $\overline{\text{PDTA}}$ active and PDTDIR to its appropriate state. Activation of $\overline{\text{PDTA}}$ signals that a PDT transfer controls the bus, while the state of the PDTDIR denotes the type of transfer, either a read (high) or write (low) to memory.

For a non-PDT transfer to SDRAM:

- $\overline{\text{PDT}}$ is inactive
- $\overline{\text{PDTA}}$ is high
- PDTDIR is not used

For a non-PDT transfer to asynchronous or programmable synchronous memory:

- $\overline{\text{PDT}}$ is inactive
- $\overline{\text{PDTA}}$ functions as an address bit
- PDTDIR functions as an address bit

4.6.1 PDT Write

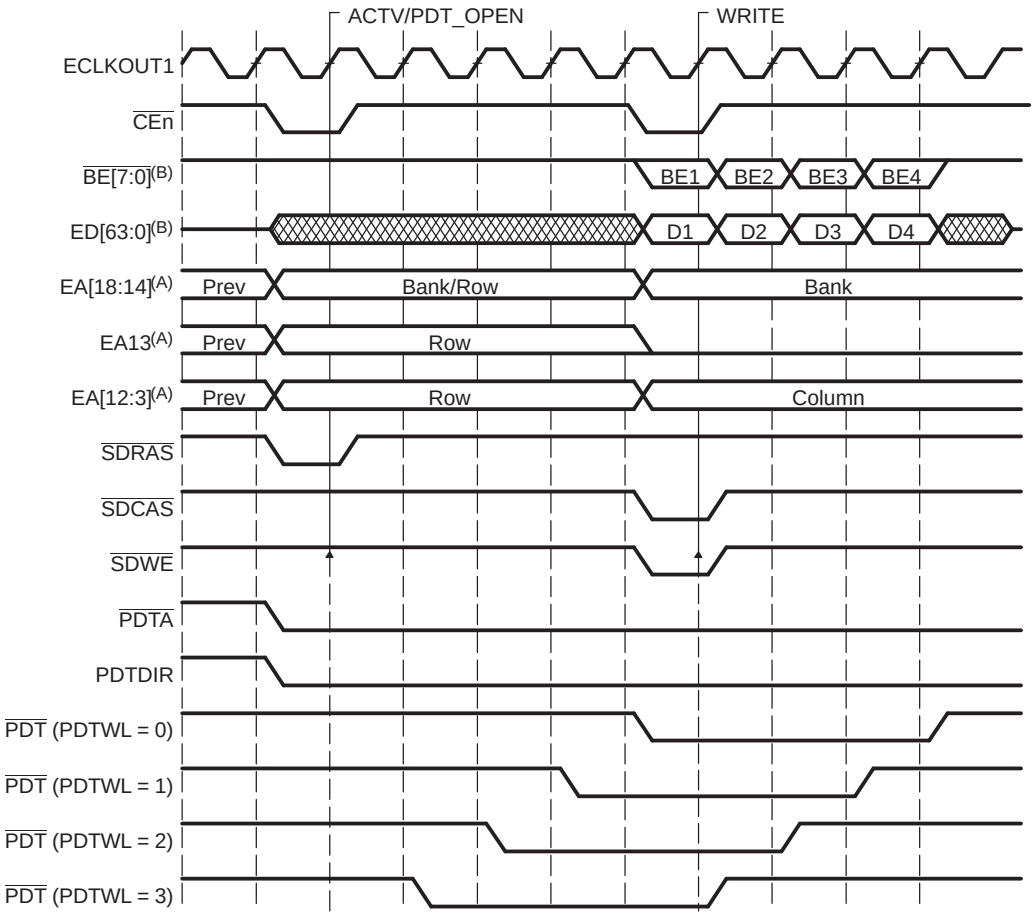
A PDT write transfer refers to a transfer from a peripheral to memory, in which the memory is physically written. To enable a PDT write transfer, set the PDTD bit in the EDMA options field to 1. The assertion/deassertion of the PDT address pins ($\overline{\text{PDTA}}$ and PDTDIR) and the PDT pin are timed according to the destination memory clock. Since the destination memory is SDRAM, ECLKOUT1 is used.

A PDT write transfer procedure is as follows:

1. The destination address is to a CE space set as SDRAM:
   - The PDT access bit (PDTA) and the PDT direction (PDTDIR) are used to give the system advance warning that a PDT transaction is pending. The system may then activate bus switches or other external logic that controls the actual PDT transfer.
   - If the access is to a closed page, then during the ACTV cycle, $\overline{\text{PDTA}}$ is low, and PDTDIR is low to indicate a write access.
   - If the access is to an open page previously accessed without a PDT operation, then the page will be closed and reopened, with the PDT address pins asserted low during the ACTV cycle.
   - If the access is to an open page previously accessed with a PDT operation, then the access goes directly to the data phase.
2. Normal write control signals are generated to the appropriate CE space.
3. The write transaction proceeds as normal except:
   - EMIF data outputs remain in a high-impedance state. Therefore, the memory latches data from the peripheral device, instead of data from the EMIF.
   - $\overline{\text{PDT}}$ is asserted low PDTWL cycles prior to the destination device latching the data. This implies that the peripheral must drive valid data PDTWL cycles after $\overline{\text{PDT}}$ is active.

Figure 4-25 displays the timing diagram for a PDT write transaction.

Figure 4-25. PDT Write Transaction Timing Diagram



A For EMIFB, BE[1:0], EA[16:12], EA[10:1], EA11, and ED[15:0], respectively, are used.

B For 32-bit EMIFA:BE[3:0] and ED[31:0] are used.

4.6.1.1 PDT Write Examples

Both the standard synchronous (STD) FIFO interface and the first word fall through (FWFT) FIFO interface support PDT write transactions. Table 4-11 gives an overview of the supported systems. Figure 4-26 through Figure 4-31 describe the various systems where PDT write transfers are supported. The examples can extend to other external peripherals.

Table 4-11. Supported Set Ups for PDT Write Transfers

Case	System Description
A	Glueless PDT write transfer to either FWFT FIFO or standard FIFO. PDTWL should be programmed accordingly with respect to the FIFO interface selected. Limited to SDRAM only in the system.
B	PDT write transfer from a FWFT FIFO with glue. PDTWL programmed to 1 cycle latency.
C	PDT write transfer from a standard FIFO with glue. PDTWL programmed to 1 cycle latency.

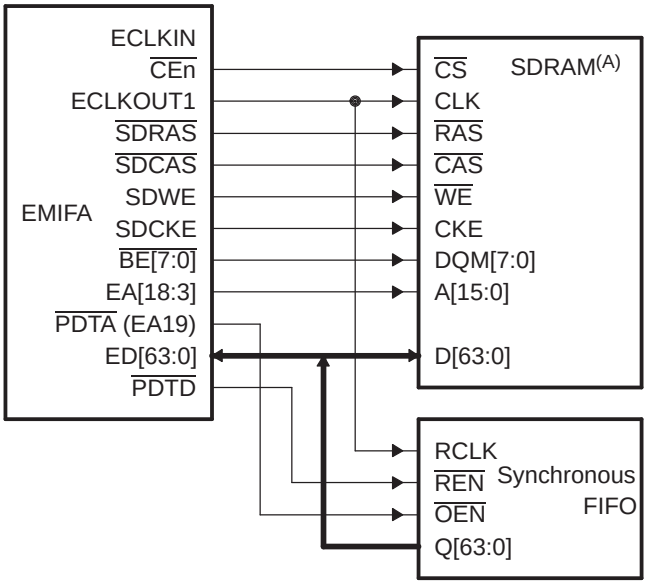
Figure 4-26 shows the glueless synchronous FIFO interface for a PDT write transaction. When the glueless interface is implemented, SDRAM must be the only memory type present in the system. This is because the glueless interface uses PDTA to generate the output enable (OE) to the FIFO. If the system includes a memory type other than SDRAM, the upper EMIF address bit used to generate PDTA (EA17, EA18, or EA19 depending on the EMIF data bus interface), will be utilized (see Table 4-3, page Table 4-3). In this setup, PDT generates the read enable (REN) to the FIFO. Program PDT latency as follows:

- FWFT FIFO: PDTWL = 0
- Standard FIFO: PDTWL = 1

Figure 4-27 shows the timing diagram for a glueless PDT write transaction to a synchronous FIFO. Note, the PDT and REN waveforms differ between the standard FIFO interface and the FWFT FIFO interface.

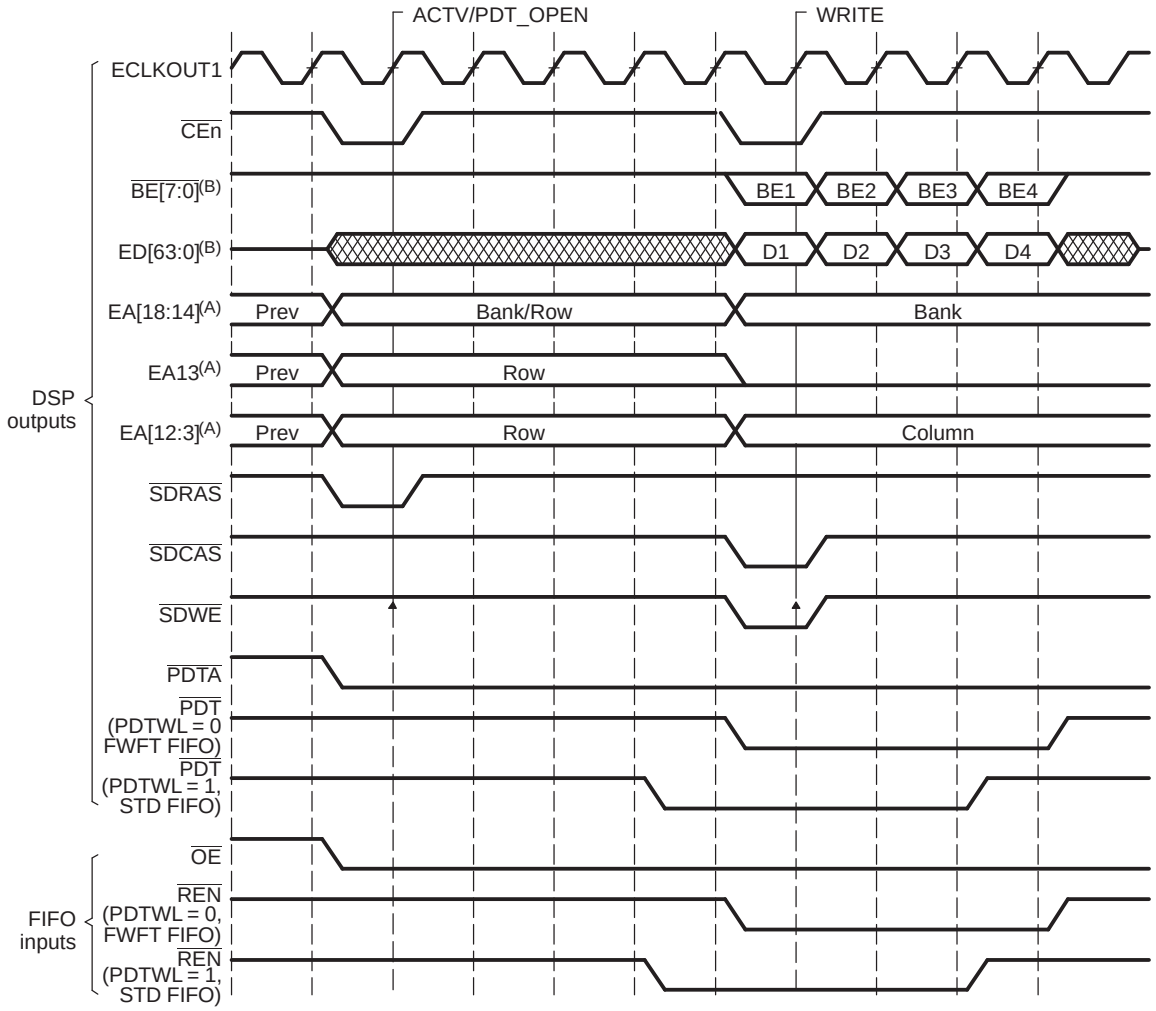
Figure 4-28 and Figure 4-29 show a PDT write interface with glue to a FWFT FIFO. Figure 4-30 and Figure 4-31 show a PDT write interface with glue to a standard FIFO. Each of these systems uses external logic to shape the PDT signal to generate the appropriate control inputs to the FIFOs. For both systems, PDTWL should be programmed to 1. These systems are not restricted to SDRAM only, any combination of memory types is allowed.

Figure 4-26. Case A: Glueless PDT Write Interface From Synchronous FIFO Block Diagram



A SDRAM must be the only memory type present in the system.

Figure 4-27. Case A: Glueless PDT Write Transfer From Synchronous FIFO Timing Diagram



A For EMIFB, BE[1:0], EA[16:12], EA[10:1], EA11, and ED[15:0], respectively, are used.

B For 32-bit EMIFA: BE[3:0] and ED[31:0] are used.

Figure 4-28. Case B: PDT Write Interface From FWFT FIFO With Glue Block Diagram

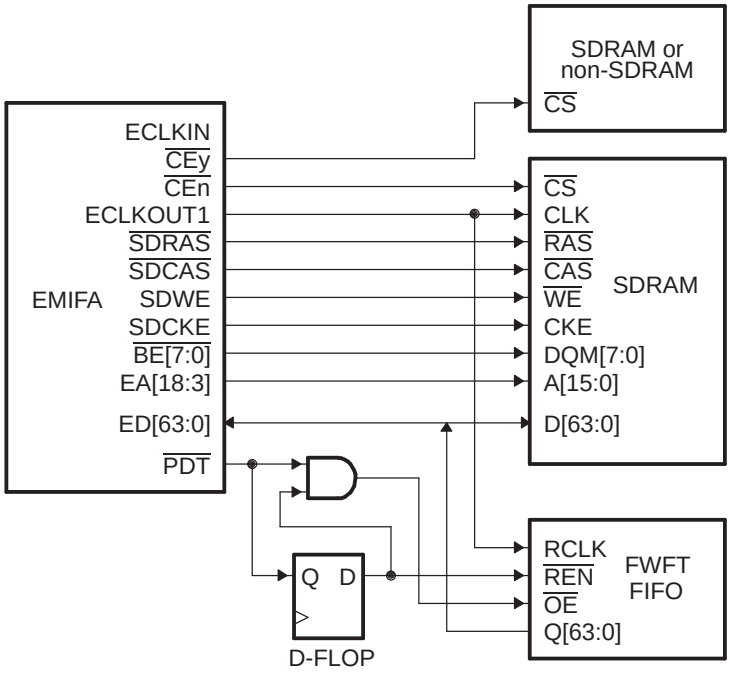
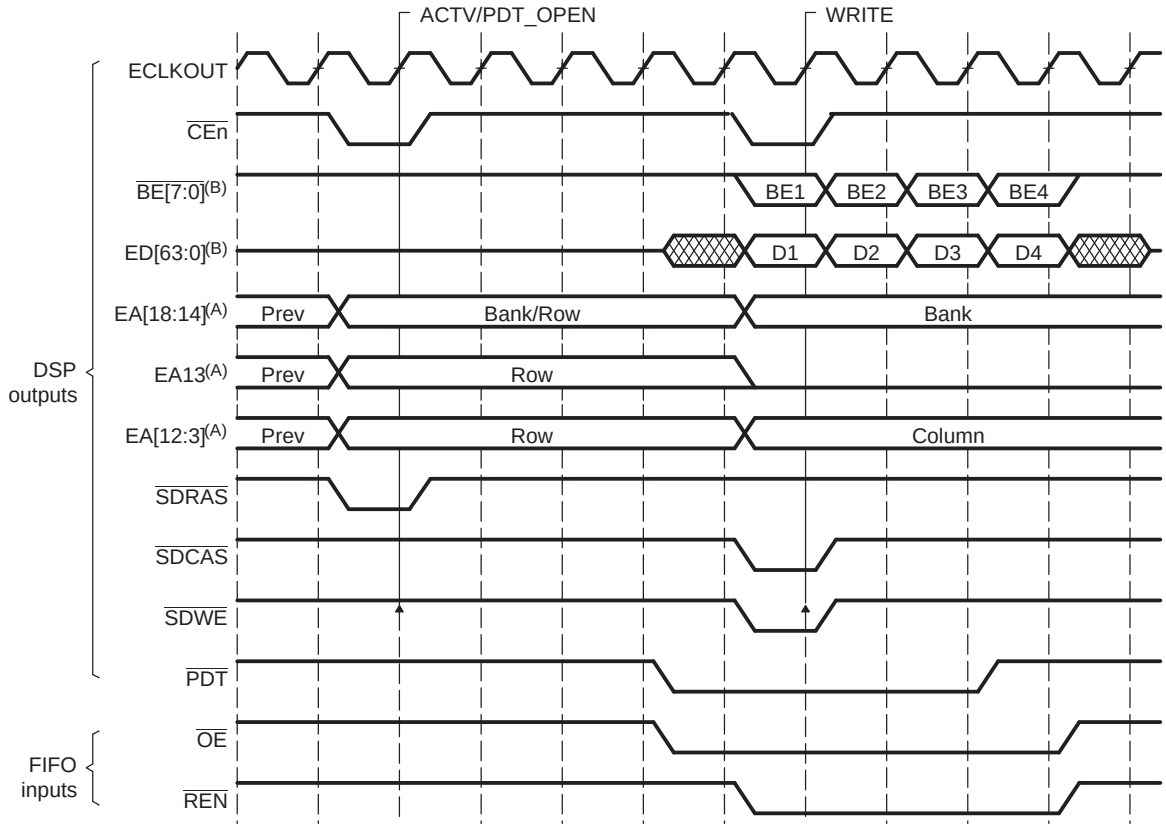


Figure 4-29. Case B: PDT Write Transfer From FWFT FIFO With Glue Timing Diagram



A For EMIFB, BE[1:0], EA[16:12], EA[10:1], EA11, and ED[15:0], respectively, are used.

B For 32-bit EMIFA:BE[3:0] and ED[31:0] are used.

Figure 4-30. Case C: PDT Write Interface From Standard FIFO With Glue Block Diagram

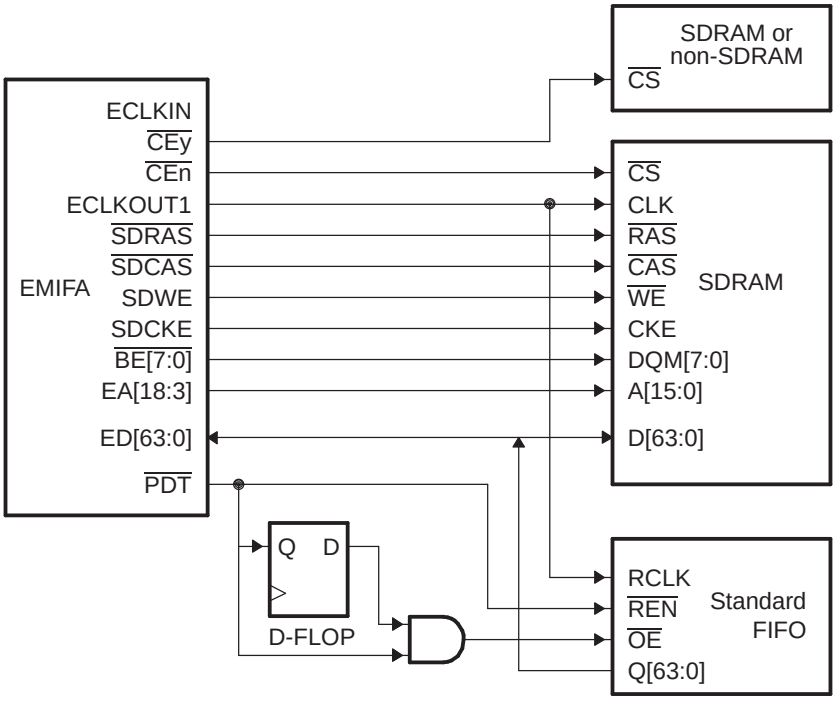
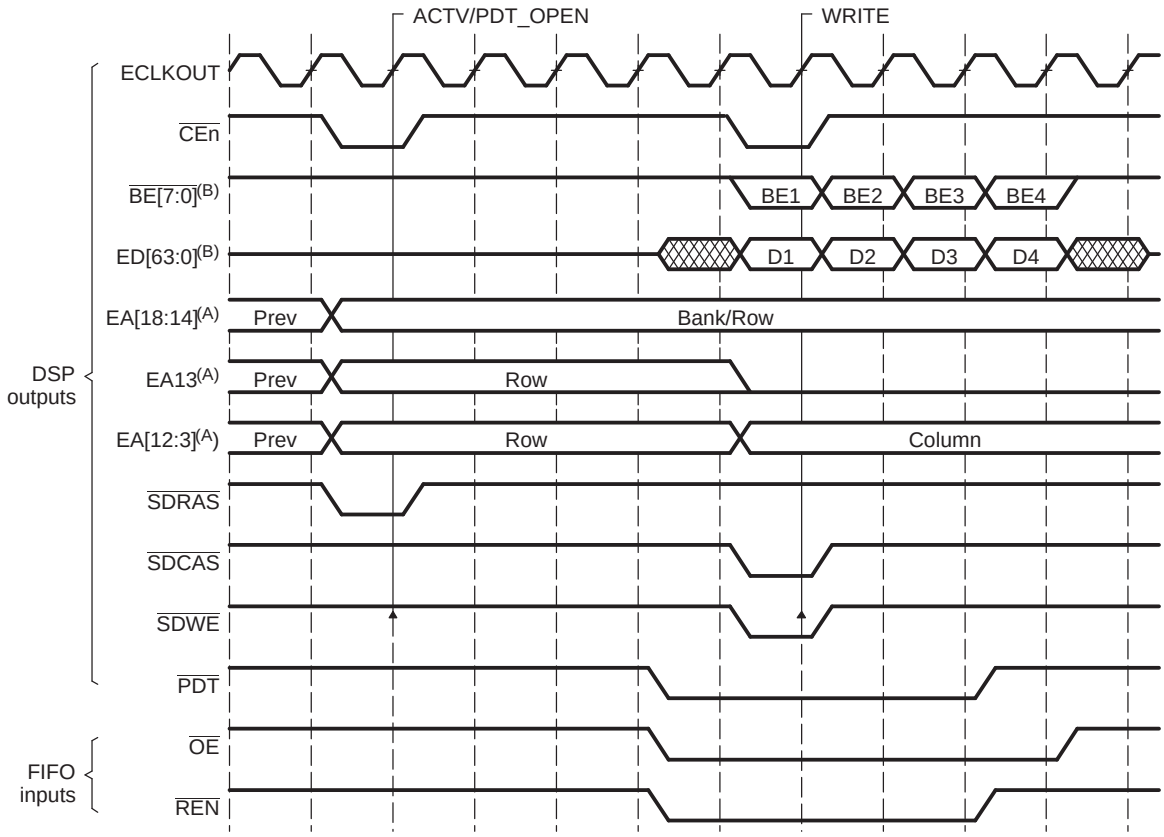


Figure 4-31. Case C: PDT Write Transfer From Standard FIFO With Glue Timing Diagram



A For EMIFB, $\overline{BE[1:0]}$, EA[16:12], EA[10:1], EA11, and ED[15:0], respectively, are used.

B For 32-bit EMIFA: $\overline{BE[3:0]}$ and ED[31:0] are used.

4.6.2 PDT Read

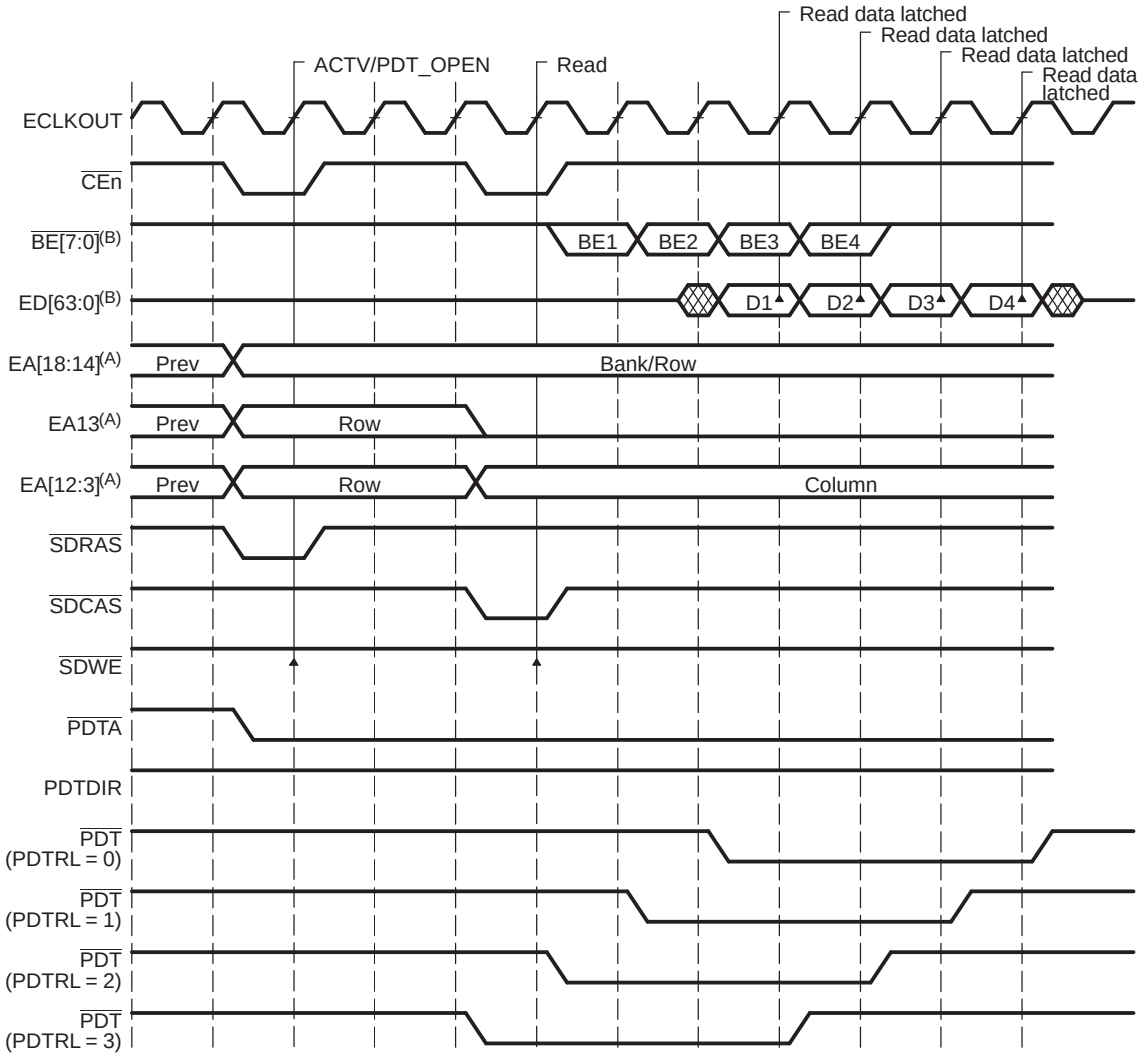
A PDT read transfer refers to a transfer from memory to a peripheral, in which the memory is physically read. To enable a PDT read transfer, set the PDTS bit in the EDMA options field to 1. The assertion/deassertion of the PDT address pins ($\overline{\text{PDTA}}$ and PDTDIR) and the PDT pin are timed according to the source memory clock. Since the source memory is SDRAM, ECLKOUT1 is used.

A PDT read transfer procedure is as follows:

1. The source address is to a CE space set as SDRAM:
   - The PDT access bit (PDTA) is used to give the system advance warning that a PDT transaction is pending. The system may then activate bus switches or other external logic that controls the actual PDT transfer.
   - If the access is to a closed page, then during the ACTV cycle, $\overline{\text{PDTA}}$ is asserted low.
   - If the access is to an open page previously accessed without a PDT operation, then the page will be closed and reopened, with $\overline{\text{PDTA}}$ asserted low during the ACTV cycle.
   - If the access is to an open page previously accessed with a PDT operation, then the access goes directly to the data phase.
   - PDTDIR remains inactive (high) throughout the course of the transaction.
2. Normal read control signals are generated to the appropriate CE space.
3. The read transaction proceeds as normal except:
   - EMIF ignores data at the ED pins.
   - $\overline{\text{PDT}}$ is asserted low PDTRL cycles before the data is to be returned by the source SDRAM.

Figure 4-32 displays the timing diagram for a PDT read transaction.

Figure 4-32. PDT Read Transaction (CAS Latency is 3) Timing Diagram



A For EMIFB, BE[1:0], EA[16:12], EA[10:1], EA11, and ED[15:0], respectively, are used.

B For 32-bit EMIFA: BE[3:0] and ED[31:0] are used.

4.6.2.1 PDT Read Examples

Both the standard synchronous FIFO interface and the first word fall through (FWFT) FIFO interface support PDT read transactions. Figure 4-33 shows an example of a PDT read transaction from SDRAM to a synchronous FIFO. The PDT signal is used to generate the write enable (WEN) input to the FIFO. PDT latency should be programmed to 0. This system is not restricted to SDRAM only, any combination of memory types is allowed. This example can extend to other external peripherals. Note in this example that no glue is required. However, if both read and write PDT transactions are required on the same bus, glue is required to properly create the OE, REN, and WEN signals for the FIFO (see Section 4.6.3.1). Figure 4-34 shows the timing diagram for a PDT read transfer to a synchronous FIFO.

Figure 4-33. Case D: Glueless PDT Read Interface to Synchronous FIFO Block Diagram

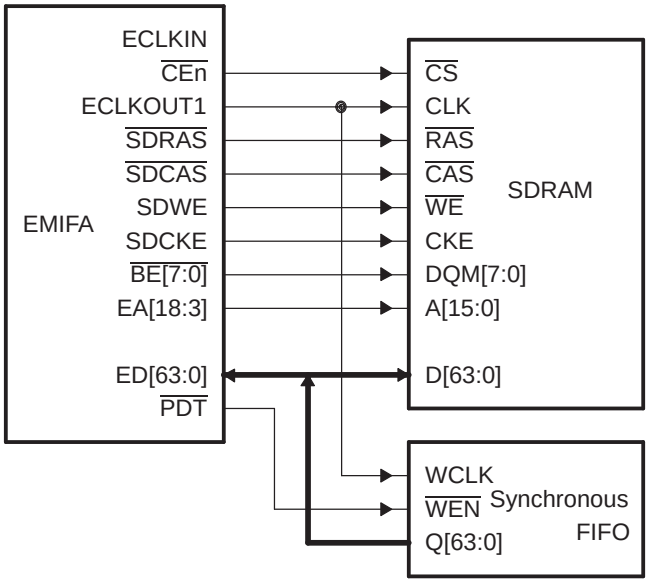
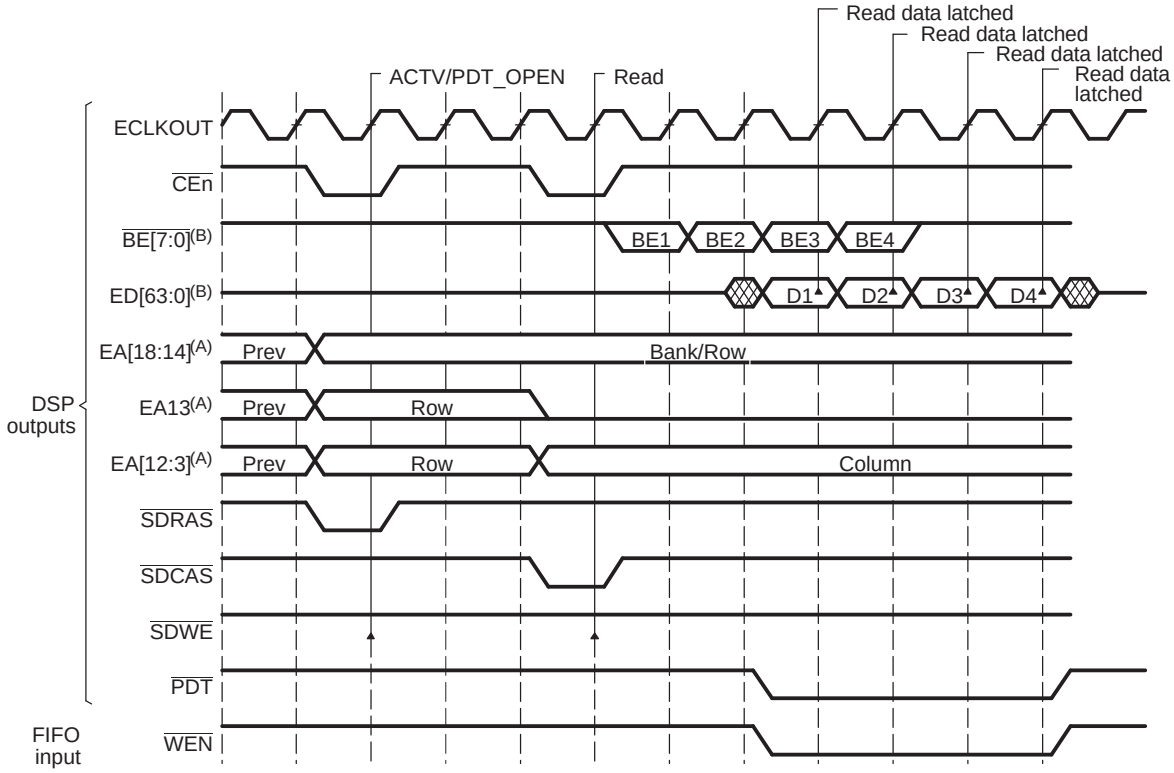


Figure 4-34. Case D: Glueless PDT Read Transfer to Synchronous FIFO Timing Diagram



A For EMIFB,$\overline{\text{BE[1:0]}}$, EA[16:12], EA[10:1], EA11, and ED[15:0], respectively, are used.

B For 32-bit EMIFA:$\overline{\text{BE[3:0]}}$ and ED[31:0] are used.

4.6.3 PDT Transfers with Multiple FIFOs on the Same Bus

The following sections describe PDT transfers with multiple FIFOs connected to a single CE space via the same data bus.

4.6.3.1 PDT Read and Write Transactions on the Same Bus

If both PDT read and write transactions are required on the same bus, glue is required to properly create the $\overline{OE}$, $\overline{REN}$, and $\overline{WEN}$ signals for the FIFO. Figure 4-35 shows a system that can perform both a PDT read and write transaction to a CE space configured as SDRAM.

The discrete logic needed to generate the appropriate input signals to the FIFOs has two main stages: Direction Detect and Demux and Signal Generation. The direction detect stage latches the state of the PDTDIR (EA20, E19, or E18, depending on the EMIF data bus interface) signal, if $\overline{CEn}$ is active and outputs the signal DIR. The demux stage receives the DIR signal and the $\overline{PDT}$ signal as inputs. Based on these inputs, the demux stage generates the appropriate input signals to drive the selected read or write FIFO. Figure 4-36 and Figure 4-37 show the timing diagrams when write and read transactions are performed in a system with FWFT FIFOs, respectively.

During a PDT write transaction, PDTDIR is active (low), denoting data is read from the synchronous FIFO and written to SDRAM. Therefore, during a PDT write transaction the appropriate $\overline{OE}$ and $\overline{REN}$ signals should be generated by the demux stage (see Figure 4-36).

During a PDT read transaction, PDTDIR is inactive (high), denoting data is read from SDRAM and written to the synchronous FIFO. Therefore, during a PDT read transaction the appropriate $\overline{WEN}$ signal should be generated by the demux stage (see Figure 4-37).

The $\overline{OE}$ and $\overline{REN}$ signals generated during the PDT write transaction, shown in Figure 4-36, are identical to those described for case B. The $\overline{WEN}$ signal generated during the PDT read transaction, shown in Figure 4-37, is identical to that described for case D. Therefore, for PDT write and PDT read timing diagrams when standard FIFOs are in the system, see Figure 4-31 and Figure 4-34, respectively.

Figure 4-35. Case E: PDT Read and Write Interface With Multiple FIFOs Block Diagram

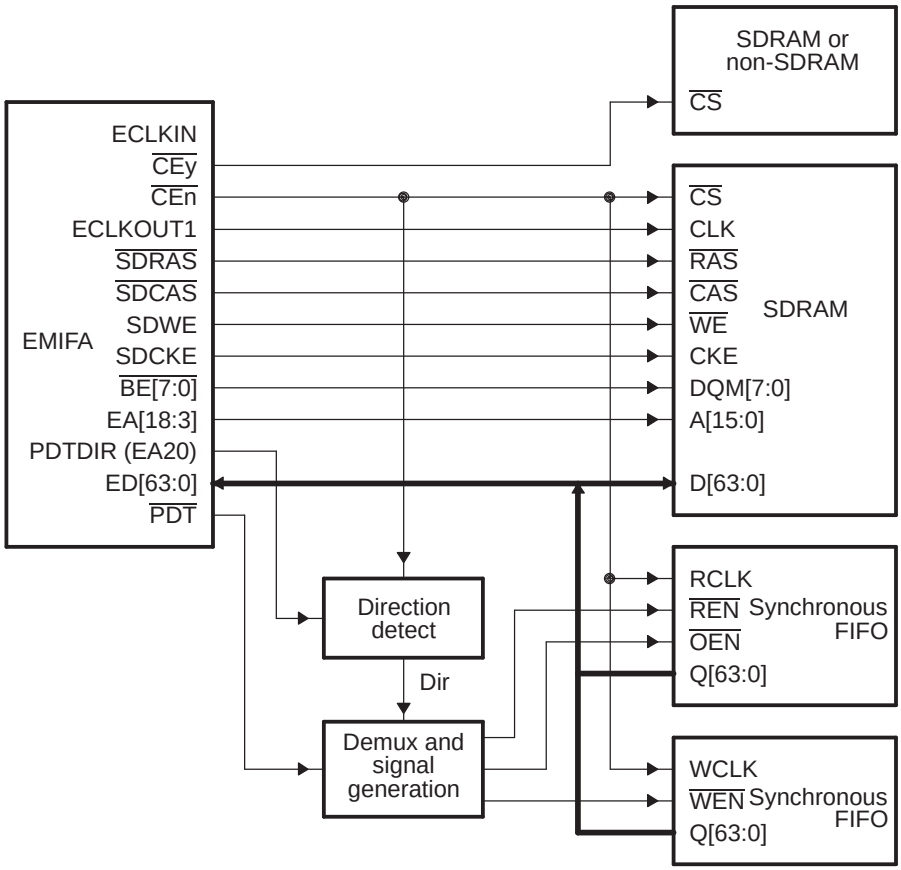
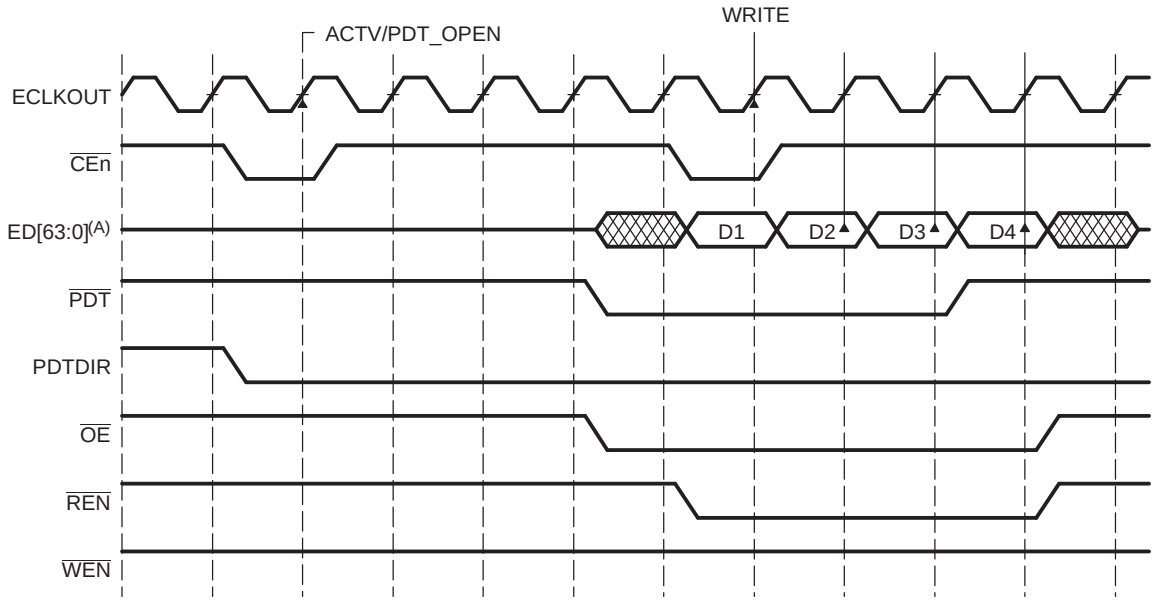
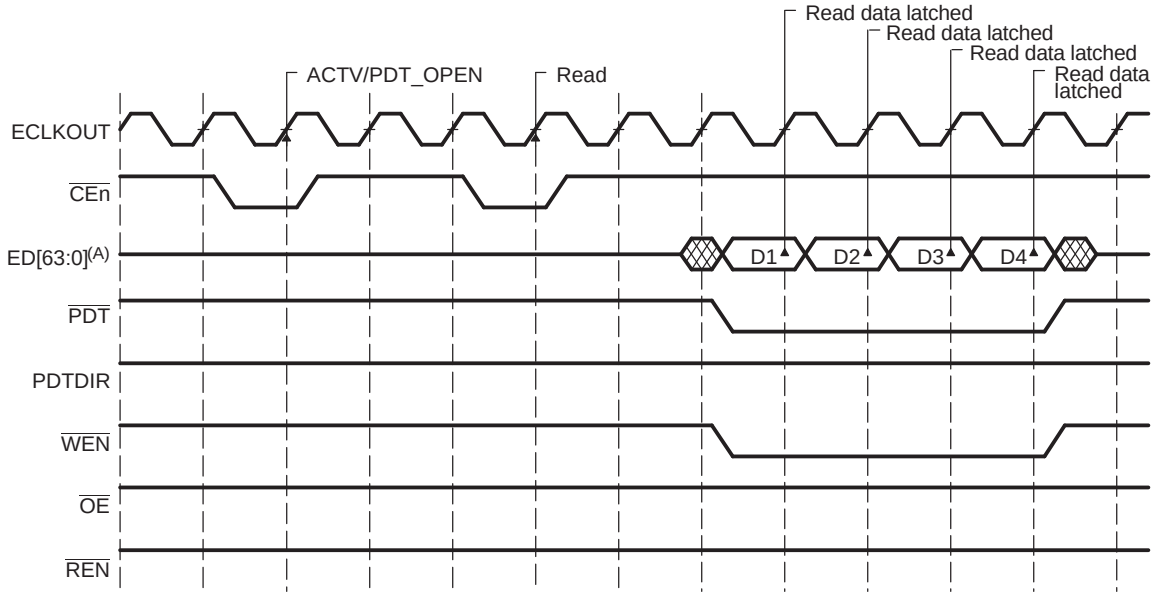


Figure 4-36. Case E: PDT Write Transfer with Read and Write FIFOs in the System (FWFT FIFO) Timing Diagram



A For EMIFB, ED[15:0] is used; for 32-bit EMIFA, ED[31:0] is used.

Figure 4-37. Case E: PDT Read Transfer with Read and Write FIFOs in the System (FWFT FIFO) Timing Diagram



A For EMIFB, ED[15:0] is used; for 32-bit EMIFA, ED[31:0] is used.

4.6.3.2 Multiple PDT Read and Write Transactions on the Same Bus

Each of the previous systems can extend to include additional read and or write FIFOs. In a system where more than two synchronous FIFOs interface to a single CE space, additional unused upper row address bits of the SDRAM can be used to select the appropriate FIFO for the current transaction. In this case, the required glue receives PDTDIR, $\overline{\text{PDT}}$, EAxx (upper address bits), and $\overline{\text{CEn}}$ as inputs. Based on the state of these inputs, the control signals are generated for the selected FIFO.

The size of the SDRAM in a given CE space limits the addition of multiple read and or write FIFOs because the size of the SDRAM dictates the number of column and row address bits required per transaction. Therefore, in some systems, it is possible to have zero unused valid address bits (see Figure 4-7 and Figure 4-8). For example, a 64-bit SDRAM that requires 11 row address bits, 8 column address bits, and 1 bank bit leaves 4 unused valid address bits for EMIFA (see the first row in Figure 4-7). This means an additional 16 FIFOs per direction can be added to the data bus. However, a 64-bit SDRAM that requires 13 row address bits, 10 column address bits, and 2 bank bits leaves zero unused valid address bits for EMIFA (see the last row in Figure 4-7). This means no additional FIFOs can be added to the data bus. Table 4-12 shows the relationship between unused valid address bits and the number of additional peripherals possible on that same data bus.

Table 4-12. Limitations on the Number of Additional Peripherals for a PDT Transfer

Number of Unused Valid Address Bits	Number of Additional Peripherals Possible
0	0
1	2
2	4
3	8
4	16

4.6.4 PDT Transfers: Bus Width and DMA Considerations

When performing a PDT transfer, the bus width and DMA configuration must be considered. The following describes the proper system configurations for a PDT transfer:

- The FIFO (or external peripheral) bus width must equal the SDRAM bus width.
- DMA must be configured such that:
  - The SRC and DST addresses are set to the same address, which matches the SDRAM address.
  - The SRC and DST addresses must be aligned to the memory (MTYPE) bus width.
  - Element size (ESIZE) is set to a 32-bit word. This is a preferred setting, see the *TMS320C6000 DSP Enhanced DMA (EDMA) Controller Reference Guide* (SPRU234).
  - Element count (ELECNT) is set to a multiple of the bus width size (in elements).

Table 4-13 summarizes the DMA configurations for supported SDRAM bus widths (MTYPE). The SUM and DUM bits are set to increment.

Table 4-13. DMA Configuration for a PDT Transfer

MTYPE (SDRAM width in bits)	Element size (ESIZE)	Element count (ELECNT)
8	32, 16, 8	No restrictions
16	32, 16	No restrictions
32	32	No restrictions
64	32	Even number

4.7 Memory Request Priority

The C64x EMIF has multiple requestors competing for the interface. Table 4-14 summarizes the priority scheme that the EMIF uses in the case of multiple pending requests. The C64x EMIF has fewer interface requestors than the C620x/C670x EMIF because the enhanced DMA (EDMA) controller processes the data memory controller (DMC), program memory controller (PMC), and EDMA transactions. Other requestors include the hold interface and internal EMIF operations, such as mode register set (MRS) and refresh (REFR).

Table 4-14. EMIF Prioritization of Memory Requests

Priority	Requestor
Highest	External hold
	Mode register set
	Refresh
Lowest	EDMA(1)

(1) Refer to *TMS320C6000 DSP Enhanced DMA (EDMA) Controller Reference Guide* (SPRU234)for details on prioritization within the EDMA.

4.8 EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through memory-mapped registers within the EMIF. Access to these registers requires the EMIF clock. Table 4-15 lists the memory-mapped registers in the C64x DSP. See the device-specific datasheet for the memory address of these registers.

Table 4-15. EMIF Registers for C64x DSP

Acronym	Register Name	Section
GBLCTL	EMIF global control register	Section 4.8.1
CECTL0-3	EMIF CE space control registers	Section 4.8.2
CESEC0-3	EMIF CE space secondary control registers	Section 4.8.3
SDCTL	EMIF SDRAM control register	Section 4.8.4
SDTIM	EMIF SDRAM refresh control register	Section 4.8.5
SDEXT	EMIF SDRAM extension register	Section 4.8.6
PDTCTL	EMIF peripheral device transfer control register	Section 4.8.7

4.8.1 EMIF Global Control Register (GBLCTL)

The EMIF global control register (GBLCTL), shown in and described in Table 4-16, configures parameters common to all the CE spaces.

Figure 4-38. EMIF Global Control Register (GBLCTL)

31						20	19	18	17	16
Reserved							EK2RATE		EK2HZ	EK2EN
R/W-0							R/W-10		R/W-0	R/W-1
15	14	13	12	11	10	9	8			
Reserved		BRMODE	Reserved	BUSREQ	ARDY	HOLD	HOLDA			
R/W-0		R/W-1	R-0	R-0	R-0	R-0	R-0			
7	6	5	4	3	2		0			
NOHOLD	EK1HZ	EK1EN	CLK4EN	CLK6EN	Reserved					
R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-16. EMIF Global Control Register (GBLCTL) Field Descriptions

Bit	*field* [1]	*symval* [1]	Value	Description
31-20	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
19-18	EK2RATE[2]		0-3h	ECLKOUT2 rate. ECLKOUT2 runs at:
		FULLCLK	0	1ıEMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate.
		HALFCLK	1h	1/2ıEMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate.
		QUARCLK	2h	1/4ıEMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate.
		-	3h	Reserved.
17	EK2HZ[3]			ECLKOUT2 high-impedance control bit.
		CLK	0	ECLKOUT2 continues clocking during Hold (if EK2EN = 1).
		HIGHZ	1	ECLKOUT2 is in high-impedance state during Hold.
16	EK2EN[3]			ECLKOUT2 enable bit.
		DISABLE	0	ECLKOUT2 is held low.
		ENABLE	1	ECLKOUT2 is enabled to clock.
15-14	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
13	BRMODE			Bus request mode (BRMODE) bit indicates if BUSREQ shows memory refresh status.
		MSTATUS	0	BUSREQ indicates memory access pending or in progress.
		MRSTATUS	1	BUSREQ indicates memory access or refresh pending or in progress.
12	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
11	BUSREQ			Bus request (BUSREQ) output bit indicates if the EMIF has an access/refresh pending or in progress.
		LOW	0	BUSREQ output is low. No access/refresh pending.
		HIGH	1	BUSREQ output is high. Access/refresh pending or in progress.
10	ARDY			ARDY input bit. Valid ARDY bit is shown only when performing asynchronous memory access (when async $\overline{CEn}$ is active).
		LOW	0	ARDY input is low. External device is not ready.
		HIGH	1	ARDY input is high. External device is ready.

(1) For CSL implementation, use the notation EMIFA_GBLCTL_*field_symval* or EMIFB_GBLCTL_*field_symval*.
(2) ECLKOUT2 rate should only be changed once during EMIF initialization from the default (1/4x) to either 1/2x or 1x.
(3) ECLKOUT*n* does not turn off/on glitch free via EK*n*EN or via EK*n*HZ. See Section 1.9.

Table 4-16. EMIF Global Control Register (GBLCTL) Field Descriptions (continued)

Bit	*field* [1]	*symval* [1]	Value	Description
9	HOLD			$\overline{\text{HOLD}}$ input bit.
		LOW	0	$\overline{\text{HOLD}}$ input is low. External device requesting EMIF.
		HIGH	1	$\overline{\text{HOLD}}$ input is high. No external request pending.
8	HOLDA			$\overline{\text{HOLDA}}$ output bit.
		LOW	0	$\overline{\text{HOLDA}}$ output is low. External device owns EMIF.
		HIGH	1	$\overline{\text{HOLDA}}$ output is high. External device does not own EMIF.
7	NOHOLD			External NOHOLD enable bit.
		DISABLE	0	No hold is disabled. Hold requests via the $\overline{\text{HOLD}}$ input are acknowledged via the HOLDA output at the earliest possible time.
		ENABLE	1	No hold is enabled. Hold requests via the $\overline{\text{HOLD}}$ input are ignored.
6	EK1HZ [3]			ECLKOUT1 high-impedance control bit.
		CLK	0	ECLKOUT1 continues clocking during Hold (if EK1EN = 1).
		HIGHZ	1	ECLKOUT1 is in high-impedance state during Hold.
5	EK1EN [3]			ECLKOUT1 enable bit.
		DISABLE	0	ECLKOUT1 is held low.
		ENABLE	1	ECLKOUT1 is enabled to clock.
4	CLK4EN [4]			CLKOUT4 enable bit. CLKOUT4 pin is muxed with GP1 pin. Upon exiting reset, CLKOUT4 is enabled and clocking. After reset, CLKOUT4 may be configured as GP1 via the GPIO enable register (GPEN).
		DISABLE	0	CLKOUT4 is held high.
		ENABLE	1	CLKOUT4 is enabled to clock.
3	CLK6EN [4]			CLKOUT 6 enable bit. CLKOUT6 pin is muxed with GP2 pin. Upon exiting reset, CLKOUT6 is enabled and clocking. After reset, CLKOUT6 may be configured as GP2 via the GPIO enable register (GPEN).
		DISABLE	0	CLKOUT6 is held high.
		ENABLE	1	CLKOUT6 is enabled to clock.
2-0	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.

(4) Applies to EMIFA only.

4.8.2 EMIF CE Space Control Registers (CECTL0-3)

The CE space control register (CECTL0-3) is shown in Figure 4-39 and described in Table 4-17. These registers correspond to the CE memory spaces supported by the EMIF. There are four CE space control registers corresponding to the four external CE signals.

The MTYPE field identifies the memory type for the corresponding CE space. If the MTYPE field selects a synchronous memory type or programmable synchronous, the remaining register fields have no effect. If the MTYPE field selects an asynchronous type, the remaining register fields specify the shaping of the address and control signals for access to that space. These features are discussed in Section 1.5.

The MTYPE field should only be set once during system initialization, except when CE1 is used for ROM boot mode. In this mode, the CE space can be configured to another asynchronous memory type.

Figure 4-39. EMIF CE Space Control Register (CECTL)

31 28	27 22	21 20	19 16
WRSETUP	WRSTRB	WRHLD	RDSETUP
R/W-1111	R/W-11 1111	R/W-11	R/W-1111

15 14	13 8	7 4	3	2 0
TA	RDSTRB	MTYPE	WRHLDMSB	RDHLD
R/W-11	R/W-11 1111	R/W-0	R/W-0	R/W-011

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-17. EMIF CE Space Control Register (CECTL) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31-28	WRSETUP	OF(*value*)	0-Fh	Write setup width. Number of clock cycles(2) of setup time for address (EA), chip enable ($\overline{CE}$), and byte enables ($\overline{BE}$) before write strobe falls. For asynchronous read accesses, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
27-22	WRSTRB	OF(*value*)	0-3Fh	Write strobe width. The width of write strobe ($\overline{AWE}$) in clock cycles.(2)
21-20	WRHLD	OF(*value*)	0-3h	Write hold width. Number of clock cycles(2) that address (EA) and byte strobes ($\overline{BE}$) are held after write strobe rises. For asynchronous read accesses, this is also the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.
19-16	RDSETUP	OF(*value*)	0-Fh	Read setup width. Number of clock cycles(2) of setup time for address (EA), chip enable ($\overline{CE}$), and byte enables ($\overline{BE}$) before read strobe falls. For asynchronous read accesses, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
15-14	TA	OF(*value*)	0-3h	Minimum Turn-Around time. Turn-around time controls the minimum number of ECLKOUT cycles(2) between a read followed by a write (same or different CE spaces), or between reads from different CE spaces. Applies only to asynchronous memory types.
13-8	RDSTRB	OF(*value*)	0-3Fh	Read strobe width. The width of read strobe ($\overline{ARE}$) in clock cycles.(2)

(1) For CSL implementation, use the notation EMIFA_CECTL_*field_symval* or EMIFB_CECTL_*field_symval.*
(2) Clock cycles are in terms of ECLKOUT1 for C64x DSP.

Table 4-17. EMIF CE Space Control Register (CECTL) Field Descriptions (continued)

Bit	*field* [1]	*symval* [1]	Value	Description
7-4	MTYPE[3]		0-Fh	Memory type of the corresponding CE spaces.
		ASYNC8	0	8-bit-wide asynchronous interface.
		ASYNC16	1h	16-bit-wide asynchronous interface.
		ASYNC32	2h	32-bit-wide asynchronous interface.
		SDRAM32	3h	32-bit-wide SDRAM.
		SYNC32	4h	32-bit-wide programmable synchronous memory.
		-	5h-7h	Reserved.
		SDRAM8	8h	8-bit-wide SDRAM.
		SDRAM16	9h	16-bit-wide SDRAM.
		SYNC8	Ah	8-bit-wide programmable synchronous memory.
		SYNC16	Bh	16-bit-wide programmable synchronous memory.
		ASYNC64	Ch	64-bit-wide asynchronous interface.
		SDRAM64	Dh	64-bit-wide SDRAM.
		SYNC64	Eh	64-bit-wide programmable synchronous memory.
		-	Fh	Reserved.
3	WRHLDMSB	OF(*value*)	0-1	Write hold width MSB is the most-significant bit of write hold.
2-0	RDHLD	OF(*value*)	0-7h	Read hold width. Number of clock cycles[2] that address (EA) and byte strobes ($\overline{BE}$) are held after read strobe rises. For asynchronous read accesses, this is also the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.

(3) 32-bit and 64-bit interfaces (MTYPE=0010b, 0011b, 0100b, 1100b, 1101b, 1110b) do not apply to C64x EMIFB.

4.8.3 EMIF CE Space Secondary Control Registers (CESEC0-3)

The CE space secondary control register (CESEC) is shown in and described in Table 4-18. These registers are added for the programmable synchronous interface, and control the cycle timing of programmable synchronous memory accesses and the clock, used for synchronization for the specific CE space. CESEC applies only to C64x programmable synchronous memory interface.

Figure 4-40. EMIF CE Space Secondary Control Register (CESEC)

31							16
Reserved							
R/W-0							
15	7	6	5	4	3	2	1 0
Reserved		SNCCLK	RENEN	CEEXT	SYNCWL		SYNCRL
R/W-0		R/W-0	R/W-0	R/W-0	R/W-0		R/W-10

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-18. EMIF CE Space Secondary Control Register (CESEC) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31-7	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
6	SNCCLK			Synchronization clock selection bit.
		ECLKOUT1	0	Control/data signals for this CE space are synchronized to ECLKOUT1.
		ECLKOUT2	1	Control/data for this CE space are synchronized to ECLKOUT2.
5	RENEN			Read Enable enable bit.
		ADS	0	ADS mode. $\overline{SADS}$/$\overline{SRE}$ signal acts as $\overline{SADS}$ signal. $\overline{SADS}$ goes active for reads, writes, and deselect. Deselect is issued after a command is completed if no new commands are pending from the EDMA. (used for SBSRAM or ZBT SRAM interface).
		READ	1	Read enable mode. $\overline{SADS}$/$\overline{SRE}$ signal acts as $\overline{SRE}$ signal. $\overline{SRE}$ goes low only for reads. No deselect cycle is issued. (used for FIFO interface).
4	CEEXT			CE extension register ENABLE BIT.
		INACTIVE	0	CE goes inactive after the final command has been issued (not necessarily when all the data has been latched).
		ACTIVE	1	On read cycles, the CE signal will go active when $\overline{SOE}$ goes active and will stay active until $\overline{SOE}$ goes inactive. The $\overline{SOE}$ timing is controlled by SYNCRL. (used for synchronous FIFO reads with glue, where $\overline{CE}$ gates $\overline{OE}$).
3-2	SYNCWL		0-3h	Synchronous interface data write latency.
		0CYCLE	0	0 cycle read latency.
		1CYCLE	1h	1 cycle read latency.
		2CYCLE	2h	2 cycle read latency.
		3CYCLE	3h	3 cycle read latency.
1-0	SYNCRL		0-3h	Synchronous interface data read latency.
		0CYCLE	0	0 cycle read latency.
		1CYCLE	1h	1 cycle read latency.
		2CYCLE	2h	2 cycle read latency.
		3CYCLE	3h	3 cycle read latency.

(1) For CSL implementation, use the notation EMIFA_CESEC_*field_symval* or EMIFB_CESEC_*field_symval.*

4.8.4 EMIF SDRAM Control Register (SDCTL)

The SDRAM control register (SDCTL) controls SDRAM parameters for all CE spaces that specify an SDRAM memory type in the MTYPE field of the associated CE space control register (CECTL). Because SDCTL controls all SDRAM spaces, each space must contain SDRAM with the same refresh, timing, and page characteristics. SDCTL should not be modified while accessing SDRAM. The SDCTL is shown in and described in Table 4-19.

The SLFRFR bit enables the self-refresh mode, in which the EMIF places the external SDRAM in a low-power mode to maintain valid data while consuming a minimal amount of power. If SDRAM is not in use by the system, then the SLFRFR bit can be used to control SDCKE as a general-purpose output. See Section 4.4.4 for details.

Figure 4-41. EMIF SDRAM Control Register (SDCTL)

31	30	29 28	27 26	25	24	23 20	19 16
Reserved	SDBSZ	SDRSZ	SDCSZ	RFEN	INIT	TRCD	TRP
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0100	R/W-1000

15 12	11 2	1	0
TRC	Reserved		SLFRFR(A)
R/W-1111	R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(A) This bit only applies to EMIFA; this bit is reserved on EMIFB.

Table 4-19. EMIF SDRAM Control Register (SDCTL) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
30	SDBSZ			SDRAM bank size bit.
		2BANKS	0	One bank-select pin (two banks).
		4BANKS	1	Two bank-select pins (four banks).
29-28	SDRSZ		0-3h	SDRAM row size bits.
		11ROW	0	11 row address pins (2048 rows per bank).
		12ROW	1h	12 row address pins (4096 rows per bank).
		13ROW	2h	13 row address pins (8192 rows per bank).
		-	3h	Reserved.
27-26	SDCSZ		0-3h	SDRAM column size bits.
		9COL	0	9 column address pins (512 elements per row).
		8COL	1h	8 column address pins (256 elements per row).
		10COL	2h	10 column address pins (1024 elements per row).
		-	3h	Reserved.
25	RFEN			Refresh enable bit. If SDRAM is not used, be sure RFEN = 0; otherwise, BUSREQ may become asserted when SDRAM timer counts down to 0.
		DISABLE	0	SDRAM refresh is disabled.
		ENABLE	1	SDRAM refresh is enabled.

(1) For CSL implementation, use the notation EMIFA_SDCTL_*field_symval* or EMIFB_SDCTL_*field_symval.*

Table 4-19. EMIF SDRAM Control Register (SDCTL) Field Descriptions (continued)

Bit	*field* [1]	*symval* [1]	Value	Description
24	INIT			Initialization bit. This bit forces initialization of all SDRAM present. Reading this bit returns an undefined value.
		NO	0	No effect.
		YES	1	Initialize SDRAM in each CE space configured for SDRAM. The CPU should initialize all of the CE space control registers and SDRAM extension register before setting INIT = 1.
23-20	TRCD[2]	OF(*value*)	0-Fh	Specifies the t_{RCD} value of the SDRAM in EMIF clock cycles.[3] TRCD = t_{RCD} / t_{cyc} - 1
19-16	TRP	OF(*value*)	0-Fh	Specifies the t_{RC} value of the SDRAM in EMIF clock cycles.[3] TRP = t_{RP} / t_{cyc} - 1
15-12	TRC	OF(*value*)	0-Fh	Specifies the t_{RC} value of the SDRAM in EMIF clock cycles.[3] TRC = t_{RC} / t_{cyc} - 1
11-1	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	SLFRFR			Self-refresh mode, if SDRAM is used in the system:
		DISABLE	0	Self-refresh mode is disabled.
		ENABLE	1	Self-refresh mode is enabled.
				If SDRAM is not used:
		DISABLE	0	General-purpose output, SDCKE = 1.
		ENABLE	1	General-purpose output, SDCKE = 0.

(2) TRCD specifies the number of ECLKOUT1 cycles between an ACTV command and a READ or WRT command (CAS). The specified separation is maintained while driving write data one cycle earlier.

(3) t_{cyc} refers to the EMIF clock period, which is equal to ECLKOUT1 period for C64x DSP.

4.8.5 EMIF SDRAM Timing Register (SDTIM)

The SDRAM timing register (SDTIM) controls the refresh period in terms of EMIF clock cycles. The SDTIM is shown in and described in Table 4-20. Optionally, the PERIOD field can send an interrupt to the CPU. Thus, this counter can be used as a general-purpose timer if SDRAM is not used by the system. The CPU can read the counter (CNTR) field. When the counter reaches 0, it is automatically reloaded with the period and SDINT (synchronization event to EDMA and interrupt source to CPU) is asserted. See Section 4.4.3 and Section 1.3.3 for more information on SDRAM refresh.

The XRFR field controls the number of refreshes performed when the refresh counter reaches 0. Up to four refreshes can be performed when the refresh counter expires. For example, since all banks must be deactivated to perform a refresh, it might be desirable to perform two refreshes half as often.

The system considers all refresh requests as high priority. When it is time to refresh, the refresh is performed immediately (though transfers in progress are allowed to complete). All banks are deactivated before a refresh command is issued. When the refresh command is complete, the banks are not restored to their state before refresh.

The initial value for the CNTR field and the PERIOD field is 5DCh (1500 clock cycles). With a 10-ns EMIF cycle time, there is a 15-s time between refresh operations. SDRAMs typically require 15.625 s per refresh.

Figure 4-42. EMIF SDRAM Timing Register (SDTIM)

31 26	25 24	23 12	11 0
Reserved	XRFR	CNTR	PERIOD
R/W-0	R/W-0	R-5DCh	R/W-5DCh

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-20. EMIF SDRAM Timing Register (SDTIM) Field Descriptions

Bit	*field* (1)	*symval* (1)	Value	Description
31-26	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
25-24	XRFR	OF(*value*)	0-3h	Extra refreshes controls the number of refreshes performed to SDRAM when the refresh counter expires.
			0	1 refresh.
			1h	2 refreshes.
			2h	3 refreshes.
			3h	4 refreshes.
23-12	CNTR	OF(*value*)	0-FFFh	Current value of the refresh counter.
11-0	PERIOD	OF(*value*)	0-FFFh	Refresh period in EMIF clock cycles. (2)

(1) For CSL implementation, use the notation EMIFA_SDTIM_*field_symval* or EMIFB_SDTIM_*field_symval.*
(2) EMIF clock cycles are in terms of ECLKOUT1 for C64x DSP.

4.8.6 EMIF SDRAM Extension Register (SDEXT)

The SDRAM extension register (SDEXT) allows programming of many parameters of SDRAM. The SDEDXT is shown in and described in Table 4-21. The programmability offers two distinct advantages:

- Allows an interface to a wide variety of SDRAMs and is not limited to a few configurations or speed characteristics.
- Allows the EMIF to maintain seamless data transfer from external SDRAM due to features like hidden precharge and multiple open banks.

It should be noted that the SDRAM control register (SDCTL) must be set after configuring SDEXT.

Figure 4-43. EMIF SDRAM Extension Register (SDEXT)

31	21	20	19	18	17	16	15	14	12
Reserved		WR2RD	WR2DEAC		WR2WR	R2WDQM		RD2WR	
R/W-0		R/W-1	R/W-01		R/W-1	R/W-10		R/W-101	

11	10	9	8	7	6	5	4	3	1	0
RD2DEAC		RD2RD	THZP		TWR		TRRD	TRAS		TCL
R/W-11		R/W-1	R/W-10		R/W-01		R/W-1	R/W-111		R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-21. EMIF SDRAM Extension Register (SDEXT) Field Descriptions

Bit	*field* [1]	*symval* [1]	Value	Description
31-21	Reserved	-	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
20	WR2RD	OF(*value*)	0-1	Specifies minimum number of cycles between WRITE to READ command of the SDRAM in ECLKOUT cycles.[2] WR2RD = (# of cycles WRITE to READ) - 1
19-18	WR2DEAC	OF(*value*)	0-3h	Specifies minimum number of cycles between WRITE to DEAC/DCAB command of the SDRAM in ECLKOUT cycles.[2] WR2DEAC = (# of cycles WRITE to DEAC/DCAB) - 1
17	WR2WR	OF(*value*)	0-1	Specifies minimum number of cycles between WRITE to WRITE command of the SDRAM in ECLKOUT cycles.[2] WR2WR = (# of cycles WRITE to WRITE) - 1
16-15	R2WDQM	OF(*value*)	0-3h	Specifies number of of cycles that BEx signals must be high preceding a WRITE interrupting a READ. R2WDQM = (# of cycles BEx high) - 1
14-12	RD2WR	OF(*value*)	0-7h	Specifies number of cycles between READ to WRITE command of the SDRAM in ECLKOUT cycles.[2] RD2WR = (# of cycles READ to WRITE) - 1
11-10	RD2DEAC	OF(*value*)	0-3h	Specifies number of cycles between READ to DEAC/DCAB of the SDRAM in ECLKOUT cycles.[2] RD2DEAC = (# of cycles READ to DEAC/DCAB) - 1
9	RD2RD	OF(*value*)		Specifies number of cycles between READ to READ command (same CE space) of the SDRAM in ECLKOUT cycles.[2]
			0	READ to READ = 1 ECLKOUT cycle.
			1	READ to READ = 2 ECLKOUT cycle.
8-7	THZP	OF(*value*)	0-3h	Specifies t_{HZP} (also known as t_{ROH}) value of the SDRAM in ECLKOUT cycles.[2] THZP = t_{HZP} / t_{cyc} - 1[3]
6-5	TWR	OF(*value*)	0-3h	Specifies t_{WR} value of the SDRAM in ECLKOUT cycles.[2] TWR = t_{WR} / t_{cyc} - 1[3]
4	TRRD	OF(*value*)		Specifies t_{RRD} value of the SDRAM in ECLKOUT cycles.[2]
			0	T_{RRD} = 2 ECLKOUT cycles.
			1	T_{RRD} = 3 ECLKOUT cycles.
3-1	TRAS	OF(*value*)	0-7h	Specifies t_{RAS} value of the SDRAM in ECLKOUT cycles.[2] TRAS = t_{RAS} / t_{cyc} - 1[3]

(1) For CSL implementation, use the notation EMIFA_SDEXT_*field_symval* or EMIFB_SDEXT_*field_symval.*
(2) EMIF clock cycles are in terms of ECLKOUT1 for C64x DSP.
(3) t_{cyc} refers to the EMIF clock period, which is equal to ECLKOUT1 period for C64x DSP.

Table 4-21. EMIF SDRAM Extension Register (SDEXT) Field Descriptions (continued)

Bit	*field* [1]	*symval* [1]	Value	Description
0	TCL	OF(*value*)		Specified CAS latency of the SDRAM in ECLKOUT cycles.[2]
			0	CAS latency = 2 ECLKOUT cycles.
			1	CAS latency = 3 ECLKOUT cycles.

4.8.7 EMIF Peripheral Device Transfer Control Register (PDTCTL)

The peripheral device transfer control register (PDTCTL) configures the latency of the $\overline{\text{PDT}}$ signal with respect to the data phase of the transaction. The PDTCTL is shown in and defined in Table 4-22.

Figure 4-44. EMIF Peripheral Device Transfer Control Register (PDTCTL)

31	4	3	2	1	0
Reserved		PDTWL		PDTRL	
R-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-22. EMIF Peripheral Device Transfer Control Register (PDTCTL) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
3-2	PDTWL	0-3h	PDT write latency bits.
		0	$\overline{\text{PDT}}$ signal is asserted 0 cycles prior to the data phase of a write transaction.
		1h	$\overline{\text{PDT}}$ signal is asserted 1 cycle prior to the data phase of a write transaction.
		2h	$\overline{\text{PDT}}$ signal is asserted 2 cycles prior to the data phase of a write transaction.
		3h	$\overline{\text{PDT}}$ signal is asserted 3 cycles prior to the data phase of a write transaction.
1-0	PDTRL	0-3h	PDT read latency bits.
		0	$\overline{\text{PDT}}$ signal is asserted 0 cycles prior to the data phase of a read transaction.
		1h	$\overline{\text{PDT}}$ signal is asserted 1 cycle prior to the data phase of a read transaction.
		2h	$\overline{\text{PDT}}$ signal is asserted 2 cycles prior to the data phase of a read transaction.
		3h	$\overline{\text{PDT}}$ signal is asserted 3 cycles prior to the data phase of a read transaction.

Revision History

Table A-1 lists the changes made since the previous version of this document.

Table A-1. Document Revision History

Reference	Additions/Modifications/Deletions
Table 4-4	Changed 16M bit, 2 × 16, 512K, EMIFA row values.
	Added 16M bit, 2 × 16, 512K, EMIFB row.
	Deleted 128M bit, 4 × 32, 1M, EMIFB row values.
	Changed 256M bit, 4 × 32, 2M, EMIFA row values.

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