TMS320TCI6616
Breakthrough performance for wireless base stations

Texas Instruments

Product bulletin

With an explosive growth in data usage, cellular networks are evolving to newer standards with greater bandwidth and speed. Mobile device users are devouring data at tremendous rates on their smartphones and superphones, which can degrade performance for all users. Mobile phone users expect that their calls will go through, regardless of network traffic. This explosion of data growth impacts the base station, forcing operators to move to heterogeneous networks combining macro cells and small cell solutions to affordably deliver the bandwidth needed. Multiple input, multiple output (MIMO) antenna arrays and advanced receivers are key elements of the new wireless standards that increase the bandwidth capabilities of the network.

The TMS320TCI6616 is the first dedicated base station system-on-chip (SoC) to combine field-proven PHY technology with high-performance packet processing. It is ideally suited for the data-centric performance wireless network operators are demanding today. Its multiple TMS320C66x DSP cores provide programmable power that allows base station manufacturers to deliver the spectral efficiency that operators crave.

TI's TCI6616 is a scalable SoC based on TI's KeyStone architecture and C66x DSP core. It features the highest fixed- and floating-point operation, allowing base station designers to deliver the capacity and performance to meet tomorrow's demands today. The TCI6616 enables manufacturers to reduce the cost per bit on the operator's expensive air interface, as well as lower power consumption for new base station designs. Multicore Navigator, a queue-based packet structure, coupled with TI's Open Navigator programming interface, gives designers the ability to easily add differentiating, value-added features.

With both floating- and fixed-point DSP cores on the same device, the TCI6616 enables base station designers to take advantage of rapid algorithm prototyping and quick software redesigns, reducing costs and development time. Because the C66x cores are so powerful, significantly fewer cores are needed to provide four times the processing power of previous generations of TI processors and more than double the processing power of any announced competitive products. Designers will enjoy simplified programming with fewer cores, along with increased performance.

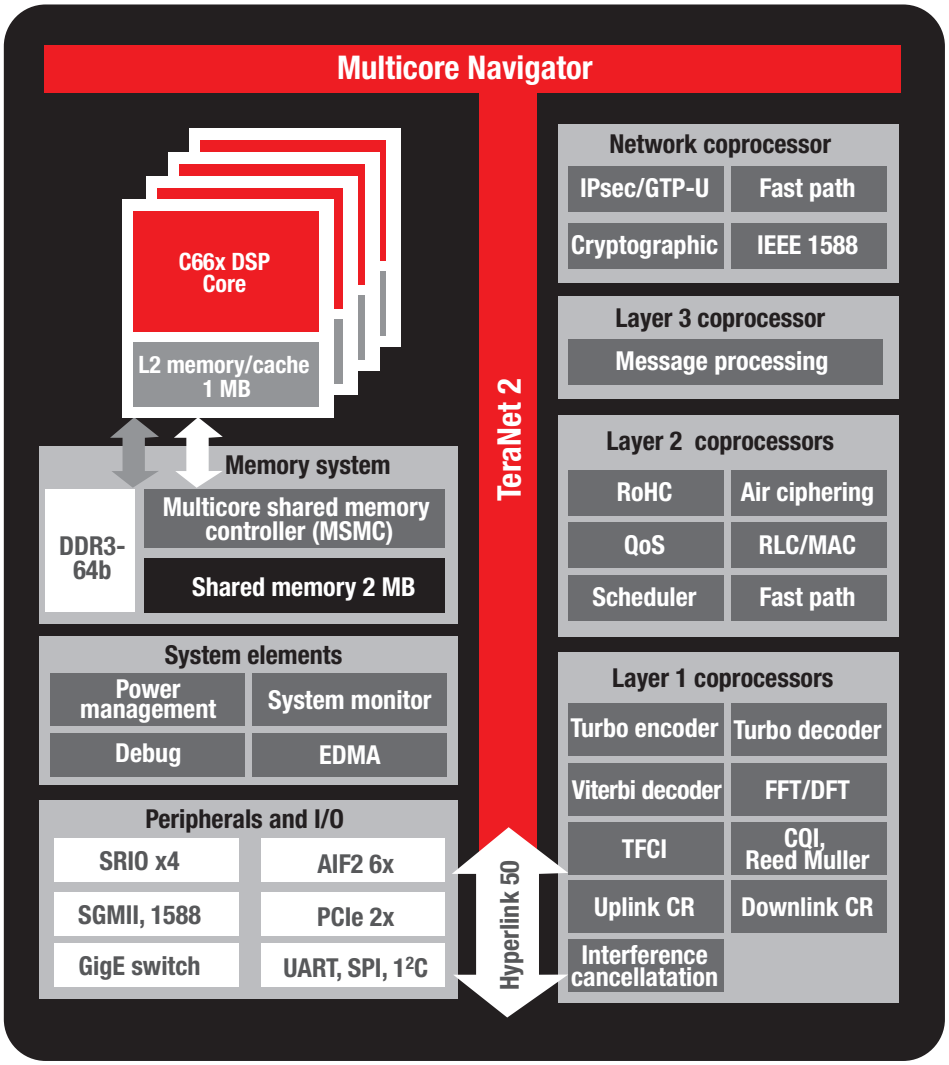
TCI6616 high-performance solution for base stations

Designed specifically for wireless infrastructure baseband applications, the TCI6616 is an ideal solution for macro base stations and enables SoC baseband solutions for GSM/EDGE, UMTS, TD-SCDMA, WiMAX and LTE applications. To make the transition from C6000™ DSPs easier, the TCI6616 is backward code-compatible, allowing software reuse and maintaining value-added designs and IP. In addition, TI's TCI6616 leverages the KeyStone architecture to enable code compatibility and scalability to meet the need of all base stations, from single sector small cells to multi-sector macro cells. With one software base driving a variety of base station products, developers will realize the highest R&D efficiency possible as well as optimized product costs.

The TMS320TCI6616 is based on 40-nm process technology and delivers 4.8 GHz of

Key features

- Highest performing multicore base station system on chip (SoC) on the market today which delivers unmatched throughput and lowest latency for multi-standard wireless base stations delivering 2X the wireless system performance of any other base station SoC
- TI's new C66x DSP combines floating and fixed point on the same core, delivering floating-point performance at fixed-point speeds for the first time.
- Only solution to feature coprocessors for every standard, including WCDMA chip rate – no FPGA/ASIC required.
- Network coprocessor and Multicore Navigator combine to provide Layer 2 and transport acceleration for all wireless base station standards.
- First product with TI's new KeyStone architecture, enabling scalability and portability from macro to small cells reducing product development expense.
- Multicore Navigator brings single-core simplicity to multicore SoCs.
- Best power/performance ratio, coupled with unique power-saving hibernation modes, delivers the lowest power for base stations.
- Leverages high-performance 40-nm process technology



▲ *TMS320CTCI6616 block diagram*

raw DSP processing power, as well as performance of up to or 153,600 16-bit GMACs per second, making it a cost-effective solution for high-performance DSP programming challenges. With the addition of the floating-point capability, the TCI6616 offers performance of up to 76 billion floating-point operations per second (GFLOPs), making it the industry's most powerful floating- and fixed-point SoC. By incorporating both fixed- and floating-point capabilities on the same core, the TCI6616 is able to perform up to five times faster than a fixed-point implementation alone. In addition, the development and debugging cycle time for complex algorithms is significantly reduced from a multiple-month cycle to just a few days.

The TCI6616 integrates large on-chip memory organized as a two-level memory system, minimizing latency and increasing system performance. The level-1 (L1) program and data memories on the TCI6616 device are 32 KB each per core. The level-2 (L2) memory is shared between program and data space and is a total of 4,096 KB (1,024 KB per core). The TCI6616 contains 2,048 KB of multicore shared memory (MSM) that is used as a shared L2 SRAM or shared L3 SRAM. A dedicated Multicore Shared Memory Controller (MSMC) prevents memory contention between the cores and arbitrates access to the shared memory between the cores and other IP blocks.

The TCI6616 has a high-performance peripheral set with everything needed to develop robust base stations of varying coverage and capacity, including:

- I^2C, SPI and UART
- PCI Express port with two lanes supporting GEN1 and GEN2
- Sixteen 64-bit general-purpose timers (also configurable as thirty-two 32-bit timers)
- 16-pin general-purpose input/output (GPIO) port with programmable interrupt/event generation mode
- Two telecom serial interface ports (TSIPs) supporting 1,024 DSOs per TSIP.
- Multicore Navigator for hardware-accelerated dispatch
- Four lanes of serial RapidIO® (SRIO), compliant with RapidIO 2.1 spec for up to 5-Gbps operation per lane
- 64-bit DDR3 SDRAM interface
- 16-bit external memory interface (EMIF) for connecting to flash memory (NAND and NOR) and asynchronous SRAM
- Second-generation SERDES-based antenna interface (AIF2) capable of up to 6.25 Gbps operation per link with six high-speed serial links, compliant to OBSAI RP3 and CPRI standards

For efficient communications between the device and the network (as well as other devices), the TCI6616 includes a network coprocessor that consists of:

- Two 10/100/1000 Ethernet media access controllers (EMACs), which provide an efficient interface between the TCI6616 DSP core processor and the core network
- Management data input/output (MDIO) module (also part of the EMAC) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system
- Packet coprocessor that provides L2 to L4 classification functionalities and the processing power of up to 1.5 Gbps
- Crypto block capable of wire-speed processing on 1-Gbps Ethernet traffic on IPSec, SRTP and 3GPP air interface security protocols
- Embedded Ethernet switch that allows multiple devices to be connected through SGMII, eliminating the need for a board-level Ethernet switch

The TCI6616 has nine high-performance embedded coprocessors to perform intensive signal processing functions common to wireless base station applications. The result is increased overall system performance. The coprocessors are four enhanced Viterbi decoder coprocessors (VCP2_A, VCP2_B, VCP2_C and VCP2_D), two third-generation

turbo decoder coprocessors (TCP3d_A and TCP3d_B), turbo encoder coprocessor (TCP3e) and two fast Fourier transform coprocessors (FFTC_A and FFTC_B). Together, they significantly accelerate channel encoding/decoding operations. Also included in the TCI6616 are four tightly coupled rake/search accelerators (RSAs) for code division multiple access (CDMA) assistance with chip-rate processing.

Faster coprocessors for optimized base station designs

Since 2001, TI has delivered radio coprocessing functions consisting of configurable IP blocks to offload processing demands as well as increase overall system performance. TI's coprocessors also reduce base station power requirements and dissipation as well as board complexity, making new products easier to design, build and debug.

As wireless radio standards evolve and related implementations become standardized, each evolution of TI's wireless SoC devices has included more and more radio acceleration/coprocessing, and as such provides a compelling roadmap to lower power and costs while delivering higher performing base station solutions for our customers. TI's SoC strategy of integrating DSP cores along with coprocessors is the simplest and most economical approach to wireless base station solutions and continues to be the market-leading solution today. TI's coprocessors eliminate external FPGAs and ASICs that were previously needed to deliver the performance needed for base stations, lowering the system cost and design complexity.

The TCI6616 has multiple dedicated high-performance embedded coprocessors to perform intensive signal processing functions common to wireless base station applications. The coprocessors are enhanced Viterbi decoder coprocessors, third-generation turbo decoder coprocessor, turbo encoder coprocessor and fast Fourier transform coprocessors. It also includes WCDMA specific spreading and despreading engines and rake search coprocessors to assist with chip-rate processing.

Delivering full multicore entitlement

TI's TCI6616 multicore SoC architecture is the first of its kind to provide full multicore entitlement, allowing for adequate system bandwidth to provide non-blocking access to all processing cores, peripherals, coprocessors and I/Os. Innovations which unleash full multicore entitlement are Multicore Navigator, TeraNet, Multicore Shared Memory Controller (MSMC) and Hyperlink.

Coprocessor	Total performance (@1.2-GHz core frequency)
FFT/DFT	1,272 MSPS @ 256-FFT 1,122 MSPS @ 192-DFT
Turbo decode	LTE – 313 Mbps @ 6144 block size WCDMA – 201 Mbps @ 5114 block size
Turbo encode	LTE – 643 Mbps @ 6144 block size WCDMA – 639 Mbps @ 5114 block size
Viterbi decoder	>38 Mbps (K = 9) Mbps
Rake Search Accelerator	32-bit multiplication per cycle
WCDMA despreading	256 AMR users supported @ eight fingers
WCDMA spreading	256 users supported with two radio links and diversity
Encryption/decryption IPSec	2.8 Gbps
Firmware-based infrastructure, multicore acceleration or Layer 2 data processing	

▲ *TI's coprocessors*

Multicore Navigator – TI's Multicore Navigator is an innovative packet-based manager that controls 8,192 queues and abstracts the connections between the various subsystems on the TCI6616. With a unified interface for communication, data transfer and job management, Multicore Navigator enables higher system performance with fewer interrupts and reduced software complexity with a "fire and forget" paradigm.

Multicore Navigator will instruct the next free DSP core to read the job and process it. Multicore Navigator is able to simplify the software architecture as well as improve performance of base stations with:

- Dynamic resource/load sharing
- Offloading of CPU overhead/delay related to inter-subsystem communications
- Hardware-based task prioritization
- Dynamic load balancing
- Common communication methodology for all IP blocks (software, I/O and accelerators)

TeraNet – TeraNet provides a hierarchal switch fabric which combines to deliver over 2 terabits of bandwidth for data transfer within the SoC. This virtually guarantees that the cores or coprocessors are never starved for data and can deliver the entitled processing horse power. As the switch fabric is architected hierarchically rather than being a flat cross bar the overall power consumption is much lower in idle states and also delivers systems with minimal latency which is a key requirement in next-generation base stations.

Multicore Shared Memory Controller (MSMC) – TI's TCI6616 includes a unique memory architecture for enhanced performance. TI's Multicore Shared Memory Controller (MSMC) allows the cores to directly access shared memory without having to use any of TeraNet 2's bandwidth. The MSMC arbitrates access to shared memory between the cores and other IP blocks, eliminating memory contention. Shared memory access for code is nearly identical in latency to local L2 access, with highly effective prefetch mechanisms for code and data.

TI's TCI6616's DDR3 is a 1,600 MHz, 64-bit bus with 8 GB of addressable memory space. Tied directly to the MSMC, the DDR3 reduces latency associated with external memory fetches and provides the speed increase and support needed for larger applications that operate on large amounts of data, which is essential for advanced 3G and 4G base stations.

Hyperlink – Hyperlink, with 4 lanes at up to 12.5 Gbps/lane, is a proprietary high-speed interconnect allowing low protocol and high-speed communication and connectivity to other KeyStone devices providing OEMs

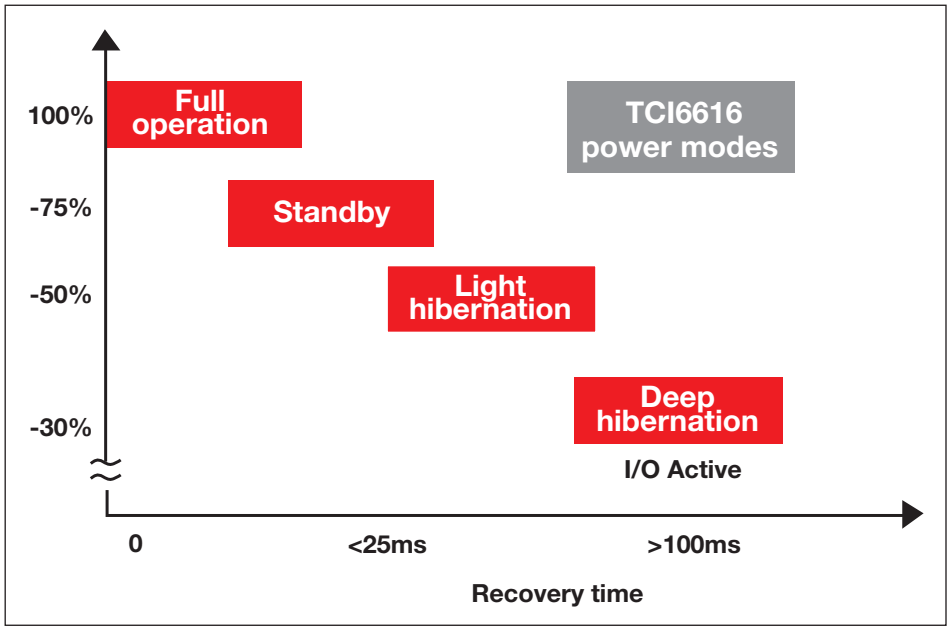
a seamless path to scalable solutions. The Hyperlink on the TCI6616 works in conjunction with the Multicore Navigator to transparently dispatch tasks to tandem devices so they execute as if they are running on local resources.

TCI6616 as Layer 2 and transport processing engine

TCI6616 combines the unmatched PHY processing capabilities with dedicated coprocessors for the Layer 2 and transport layer processing. This enables designers to create base stations without a separate network processor thereby reducing board complexity and cost without compromising performance. The network coprocessor enables fast-path processing in the transport network layer and deep into the Layer 2 of the radio network. Within the network coprocessor inside the TCI6616, the Packet Accelerator and the Security Accelerator perform fully accelerated autonomous packet-to-packet processing. They leverage the Multicore Navigator which utilizes a zero-copy approach to optimize data processing at all layers. Classsification and ordering, multicore-accessible storage, memory management, segmentations and reassembly, and delivery across multiple cores and devices are all supported by Multicore Navigator. Layer 2 data-plane and transport plane overhead can be reduced by 10-15x due to the fast-path and zero-copy processing enabled by the Multicore Navigator.

Lowest power consumption for performance

TI has a history of providing the lowest power wireless base station SoCs on the market. TI is able to achieve its ultimate low power through the combination of its process technology including, SmartReflex™ technology and the proactive use of power management techniques, (such as adaptive voltage scaling) in every wireless base station semiconductor device to keep active power at a minimum. In addition, TI has leveraged its extensive knowledge in the wireless base station market to establish multiple, dynamic power modes for the TCI6616 device (shown in the above diagram), allowing customers to work with network operators to customize a programmable strategy for optimizing power usage based on operation and regional use modes. Utilizing TI's power management techniques on the TCI6616 enables designers to develop compelling base station solutions capable of operating at less than 30 W for full Layer 1 and 2 operations. A typical Layer 1 and 2 full operation solution today uses more than 150 W and requires many additional semiconductor devices, driving up power requirements. TI's solution is five times lower than the typical full operation solution, resulting in significant power savings and reduced design costs.



▲ *Dynamic power modes*

Complete tools and support

TI provides a full suite of best-in-class Eclipse-based development and debugging tools with the TCI6616, which includes a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source-code execution. TI's compiler generates highly efficient code that is "first-pass efficient" so there is less need to optimize it. TI's debugging tools help developers visualize problems and resolve them quickly, helping designers get products to the field faster while saving development resources. In addition, TI will offer a TCI6616 evaluation module (EVM) that will help customers to quickly prototype using the TCI6616.

For more information

To learn more about the TCI6616 SoC visit **www.ti.com/tci6616**. Discover how the TCI6616 can add performance to your next wireless base station design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265