TMS320C6472 Fixed-Point Digital Signal Processor Technical Brief

Check for Samples: TMS320C6472

1 Features

- Six On-Chip TMS320C64x+ Megamodules
- Endianess: Little Endian, Big Endian
- C64x+ Megamodule Main Features:
  - High-Performance, Fixed-Point TMS320C64x+ DSP
  - 500/625/700 MHz
  - Eight 32-Bit Instructions/Cycle
  - 4000 MIPS/MMACS (16-Bits) at 500 MHz
  - Dedicated SPLOOP Instruction
  - Compact Instructions (16-Bit)
  - Instruction Set Enhancements
  - Exception Handling
  - L1/L2 Memory Architecture:
    - 256K-Bit (32K-Byte) L1P Program RAM/Cache [Direct Mapped, Flexible Allocation]
    - 256K-Bit (32K-Byte) L1D RAM/Cache [2-Way Set-Associative, Flexible Allocation]
    - 4.75M-Bit (608K-Byte) L2 Unified Mapped RAM/Cache [4-Way Set-Associative, Flexible Allocation]
    - L1P Memory Controller
    - L1D Memory Controller
    - L2 Memory Controller
  - Time Stamp Counter
  - One 64-Bit General-Purpose/Watchdog Timer
- Shared Peripherals and Interfaces
  - EDMA Controller (64 Independent Channels)
  - Shared Memory Architecture
    - Shared L2 Memory Controller
    - 768K-Byte of RAM
    - Boot ROM
  - Three Telecom Serial Interface Ports (TSIPs)
    - Each TSIP is 8 Links of 8 Mbps per Direction
  - 32-Bit DDR2 Memory Controller (DDR2-533 SDRAM)
    - 256 M-Byte x 2 Addressable Memory Space
  - Two 1x Serial RapidIO® Links, v1.2 Compliant
    - 1.25-, 2.5-, 3.125-Gbps Link Rates
    - Message Passing, DirectIO Support, Error Management Extensions, and Congestion Control
    - IEEE 1149.6 Compliant I/Os
  - UTOPIA
    - UTOPIA Level 2 Slave ATM Controller
    - 8/16-Bit Transmit and Receive Operations up to 50 MHz per Direction
    - User-Defined Cell Format up to 64 Bytes
  - Two 10/100/1000 Mb/s Ethernet MACs (EMACs)
    - Both EMACs are IEEE 802.3 Compliant
    - EMAC0 Supports:
      - MII, RMII, SS-SMII, GMII, and RGMII
      - 8 Independent Transmit (TX) Channels
      - 8 Independent Receive (RX) Channels
    - EMAC1 Supports:
      - RMII, SS-SMII and RGMII
      - 8 Independent Transmit (TX) Channels
      - 8 Independent Receive (RX) Channels
    - Both EMACs (EMAC0 and EMAC1) Share MDIO Interface
  - 16-Bit Host-Port Interface (HPI)
  - One Inter-Integrated Circuit (I^2C) Bus
  - Six Shared 64-Bit General-Purpose Timers
- System PLL and PLL Controller
- Secondary PLL and PLL Controller, Dedicated to EMAC
- Third PLL and PLL Controller Dedicated to DDR2 Memory Controller
- 16 General-Purpose I/O (GPIO) Pins
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- 737-Pin Ball Grid Array (BGA) Package (CTZ or ZTZ Suffix), 0.8-mm Ball Pitch
- 0.09-µm/7-Level Cu Metal Process (CMOS)
- 3.3-, 1.8-, 1.5-, 1.2-V I/O Supplies
- 1.0-/1.1-, 1.2-V Core Supplies
- Commercial Temperature [0°C to 85°C]
- Extended Temperature [-40°C to 100°C]

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1.1 CTZ/ZTZ BGA Package (Bottom View)

The TMS320C6472 devices are designed for a package temperature range of 0°C to 85°C (commercial temperature range) or -40°C to 100°C (extended temperature range).

NOTE

Extended temperature (A) range is available only on 500-MHz and 625-MHz devices.

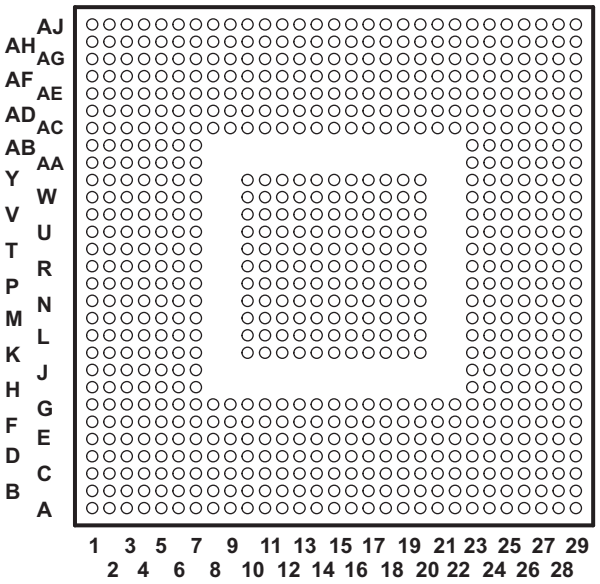

Figure 1-1. CTZ/ZTZ 737-Pin Ball Grid Array (BGA) Package (Bottom View)

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1.2 Description

The TMS320C6472 device is a Texas Instruments next-generation fixed-point digital signal processor (DSP) targeting high-performance computing applications, including high-end industrial, mission-critical, high-end image and video, communication, media gateways, and remote access servers. This device was designed with these applications in mind. A common key requirement of these applications is the availability of large on-chip memories to handle vast amounts of data during processing. With 768K-Byte of shared RAM and 608K-Byte local L2 RAM per C64x+ Megamodule, the TMS320C6472 device can eliminate the need for external memory, thereby reducing system power dissipation and system cost and optimizing board density.

The TMS320C6472 device has six optimized TMS320C64x+™ megamodules, which combine high performance with the lowest power dissipation per port. The TMS320C6472 device includes three different speeds: 500 MHz, 625 MHz, and 700 MHz. The C64x+ megamodules are the highest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. The C64x+ megamodule is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making devices like TMS320C6472 an excellent choice for applications including video and telecom infrastructure, imaging/medical, and wireless infrastructure (WI). The C64x+™ devices are upward code-compatible from previous devices that are part of the C6000™ DSP platform.

The C64x+ megamodule core employs eight functional units, two register files, and two data paths. Like the earlier C6000 devices, two of these eight functional units are multipliers or .M units. Each C64x+ megamodule core .M unit doubles the multiply throughput versus the C64x core by performing four 16-bit x 16-bit multiply-accumulates (MACs) every clock cycle. Thus, eight 16-bit x 16-bit MACs can be executed every cycle on the C64x+ core. At a 500-MHz clock rate, this means 4000 16-bit MMACs can occur every second. Moreover, each multiplier on the C64x+ megamodule core can compute one 32-bit x 32-bit MAC or four 8-bit x 8-bit MACs every clock cycle.

The C64x+ megamodule integrates a large amount of on-chip memory organized as a two-level memory system. The level-1 (L1) program and data memories on this C64x+ megamodule are 32KB each. This memory can be configured as mapped RAM, cache, or some combination of the two. When configured as cache, L1 program (L1P) is a direct mapped cache where as L1 data (L1D) is a two-way set associative cache. The level 2 (L2) memory is shared between program and data space and is 608K-Byte in size. L2 memory can also be configured as mapped RAM, cache, or some combination of the two. The C64x+ megamodule also has a 32-bit peripheral configuration (CFG) port, an internal DMA (IDMA) controller, a system component with reset/boot control, interrupt/exception control, a power-down control, and a free-running 32-bit timer for time stamp.

The peripheral set includes: three Telecom Serial Interface Port (TSIPs); an 16/8 bit Universal Test and Operations PHY Interface for Asynchronous Transfer Mode (ATM) Slave [UTOPIA Slave] port; two 10/100/1000 Ethernet media access controllers (EMACs), which provide an efficient interface between the C6472 DSP core processor and the network; a management data input/output (MDIO) module (shared by both EMACs) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system; a Serial RapidIO® with two 1x lanes and support for packet forwarding; a 32-bit DDR2 SDRAM interface; 12 64-bit general-purpose timers; an inter-integrated circuit bus module (I2C); 16 general-purpose input/output ports (GPIO) with programmable interrupt/event generation modes; and a 16-bit multiplexed host-port interface (HPI16).

The C6472 device has a complete set of development tools which includes: a C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows® debugger interface for visibility into source code execution.

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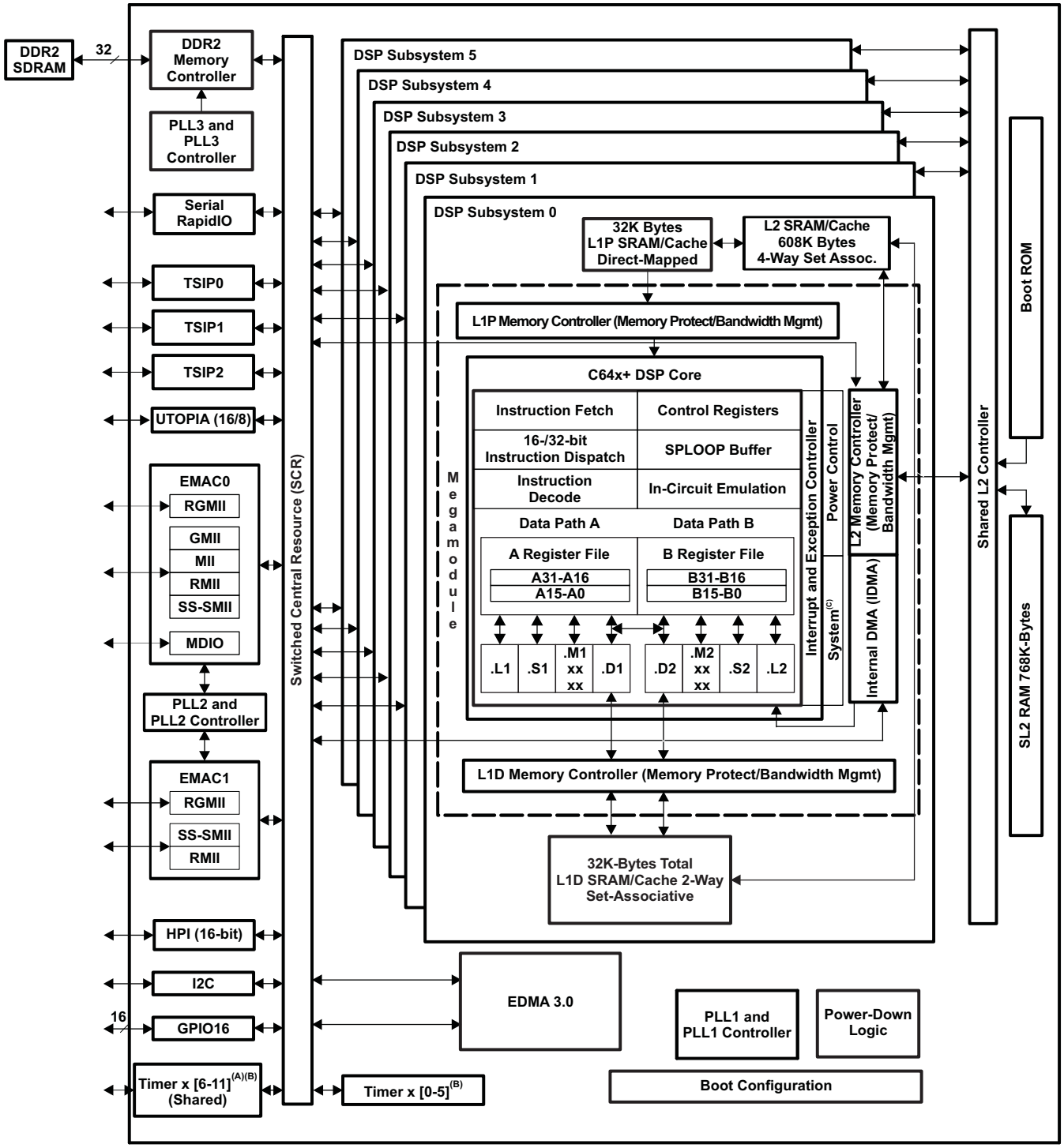
1.3 Functional Block Diagram

Figure 1-2 shows the functional block diagram of the C6472 device.



A. Timers 6-11 are shared.
B. Each of the Timer peripherals are configurable as either one 64-bit general-purpose timer *or* two 32-bit general-purpose timers *or* a watchdog timer.
C. System consists of Test, Emulation, Power Down, and Interrupt Controller.

Figure 1-2. C6472 Functional Block Diagram

2 Device Operating Conditions

2.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted)(1)(2)(3)

Supply voltage range:	CV_{DD}	-0.5 V to 1.5 V
	CV_{DD2}	-0.5 V to 1.5 V
	DV_{DD33}	-0.5 V to 4.2 V
	DV_{DD18}, AV_{DDA3}, AV_{DDA4}	-0.5 V to 2.5 V
	AV_{DDA1}, AV_{DDA2}	-0.5 V to 2.5 V
	DV_{DD15}	-0.5 V to 2.5 V
	DV_{DDR}	-0.5 V to 2.5 V
	CV_{DD1}	-0.5 V to 1.5 V
	AV_{DDA}, DV_{DDD}, AV_{DDT}	-0.5 V to 1.5 V
Input voltage (V_I) range:	3.3-V pins	-0.5 V to DV_{DD33} + 0.5 V
	RGMII pins	-0.3 V to DV_{DD15} + 0.3 V
	DDR2 memory controller pins	-0.3 V to DV_{DD18} + 0.3 V
	RIO pins	0 V to 1.32 V
Output voltage (V_O) range:	3.3-V pins	-0.5 V to DV_{DD33} + 0.5 V
	RGMII pins	-0.3 V to DV_{DD15} + 0.3 V
	DDR2 memory controller pins	-0.3 V to DV_{DD18} + 0.3 V
	RIO pins	0 V to 1.32 V
Operating case temperature range, T_C:	Standard	0°C to 85°C
	A version(4)	-40°C to 100°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.
(3) Overshoot and undershoot transients due to impedance mismatch on 3.3-V pins can be up to 30% of the supply voltage for up to 30% of the signal period without significantly impacting reliability. For RGMII and DDR2 pins, limit overshoot/undershoot to 20% of supply voltage for up to 20% of the duty cycle. These period limits assume continuous operation.
(4) Extended temperature (A version) range is available only on 500-MHz and 625-MHz devices.

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2.2 Recommended Operating Conditions[1]

PARAMETER			MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core	500 MHz	0.95	1.0	1.05	V
		625 MHz	1.05	1.1	1.16	
		700 MHz	1.14	1.2	1.26	
CV_{DD2}	Supply voltage, SRIO Core	500 MHz	0.95	1.0	1.05	V
		625 MHz	1.05	1.1	1.16	
		700 MHz	1.14	1.2	1.26	
CV_{DD1}	Supply volttage, 1.2-V DDR Core		1.14	1.2	1.26	V
DV_{DD33}	Supply voltage, 3.3-V I/O		3.135	3.3	3.465	V
DV_{DD18}	Supply voltage, 1.8-V I/O (DDR)		1.71	1.8	1.89	V
DV_{DD15}	Supply voltage, 1.8-V/1.5-V I/O (RGMII)		1.4		1.9	V
$V_{REFHSTL}$ ($0.5 * DV_{DD15}$)	Reference voltage, RGMII I/O		0.7		0.95	V
$V_{REFSSTL}$ ($0.5 * DV_{DD18}$)	Reference voltage, DDR2 I/O		0.855	0.9	0.945	V
AV_{DDA1}	Analog supply voltage, PLL1 (System PLL)		1.71	1.8	1.89	V
AV_{DDA2}	Analog supply voltage, PLL2 (EMAC PLL)		1.71	1.8	1.89	V
AV_{DDA3}	Analog supply voltage, PLL3 (DDR PLL)		1.71	1.8	1.89	V
AV_{DDA4}	Analog supply voltage, DDR		1.71	1.8	1.89	V
DV_{DDD}	SRIO Digital supply voltage		1.14	1.2	1.26	V
AV_{DDA}	SRIO Analog supply voltage		1.14	1.2	1.26	V
AV_{DDT}	SRIO Termination voltage		1.14	1.2	1.26	V
DV_{DDR}	SRIO Regulator supply voltage		1.35	1.5/1.8	1.98	V
V_{IH}	High-level input voltage	3.3-V pins (except I2C pins)	2.0		DV_{DD33} + 0.5	V
		I2C pins	0.7 * DV_{DD33}		DV_{DD33} + 0.5	
		RGMII pins	$V_{REFHSTL}$ + 0.10		DV_{DD15} + 0.3	
		DDR2 memory controller pins	$V_{REFSSTL}$ + 0.125		DV_{DD18} + 0.3	
V_{IL}	Low-level input voltage	3.3-V pins (except I2C pins)	-0.5		0.8	V
		I2C pins	-0.5		0.3 * DV_{DD33}	
		RGMII pins	-0.3		$V_{REFHSTL}$ - 0.1	
		DDR2 memory controller pins	-0.3		$V_{REFSSTL}$ - 0.125	
P_{CDD}	Core supply power[2]	CV_{DD} = CV_{DD2} = 1.0 V, CPU frequency = 500 MHz		2.38		W
		CV_{DD} = CV_{DD2} = 1.1 V, CPU frequency = 625 MHz		3.76		
		CV_{DD} = CV_{DD2} = 1.2 V, CPU frequency = 700 MHz		5.42		

(1) Operating conditions are at 500 MHz, 625 MHz, or 700 MHz.
(2) Assumes the following conditions: CPU utilization 30% DSP/60% control; DDR2 at 30% utilization (266 MHz), 35% writes, 32 bits, 15% bit switching; TSIP0, TSIP1, and TSIP2 at 20% utilization, 15% switching; UTOPIA 50 MHz, 16-bit at 50% utilization, 15% switching EMAC0, 1000 Mbps, RGMII, 50% utilization, 50% switching; EMAC1 disabled; SRIO both lanes disabled; all timers active; HPI disabled; I2C enabled at 10% utilization; room temperature (25°C). The actual power consumption is application-dependent. For more details on core and I/O activity, see the *TMS320C6472/TMS320TCI6486 Power Consumption Summary* (literature number SPRAAS4).

Recommended Operating Conditions[1] *(continued)*

PARAMETER			MIN	NOM	MAX	UNIT
P_{DDD}	I/O supply power[2]	3.3-V Supply (DV_{DD33})		0.2		W
		1.8-V Supplies, including PLLs (DV_{DD18}, AV_{DDA1}, AV_{DDA2}, AV_{DDA3}, AV_{DDA4}		0.26		
		1.5-V Supplies (DV_{DD15}, DV_{DDR})		0.05		
		1.2-V Supplies (CV_{DD1}, AV_{DDA}, DV_{DDD}, AV_{DDT})		0.28		

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2.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
V_{OH}	High-level ouput voltage	3.3 V pins (except I2C pins)	DV_{DD33} = MIN, I_{OH} = MAX	0.8 * DV_{DD33}			V
		I2C pins	DV_{DD33} = MIN, I_{OH} = MAX	0.8 * DV_{DD33}			V
		RGMII pins		DV_{DD15} - 0.4			V
		DDR2 memory controller pins		DV_{DD18} - 0.4			V
V_{OL}	Low-level ouput voltage	3.3-V pins (except I2C pins)	DV_{DD33} = MIN, I_{OL} = MAX			0.4	V
		I2C pins	Pulled up to 3.3 V, 3 mA sink current			0.4	V
		RGMII pins				0.4	V
		DDR2 memory controller pins				0.4	V
I_I	Input current (DC)	3.3-V pins (except I2C pins)	V_I = V_{SS} to DV_{DD33}, pins without internal pull-up or pull-down resistor	-1		1	uA
			V_I = V_{SS} to DV_{DD33}, pins with internal pull-up resistor	50	100	400	uA
			V_I = V_{SS} to DV_{DD33}, pins with internal pull-down resistor	-400	-100	-50	uA
		I2C pins	0.1 * DV_{DD33} ≤ V_I ≤ 0.9 * DV_{DD33}	-10		10	uA
		RGMII pins		-1		1	uA
		DDR2 memory controller pins		-1		1	uA
I_{OH}	High-level output current	E Class Buffers - EMU[18:0] and all 3.3-V Ethernet, except MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				-7	mA
		D Class Buffers - GPIO[15:0], TDO, HOUT, and SYSCLKOUT				-3	mA
		C Class Buffers - HPI, TSIP, UTOPIA, BOOTACTIVE, WDOUT, RESETSTAT, TIMO2, MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				-3	mA
		RGMII pins				-8	mA
		DDR pins				-13.4	mA

(1) For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted) *(continued)*

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current	E Class Buffers - EMU[18:0] and all 3.3-V Ethernet, except MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				7	mA
		D Class Buffers - GPIO[15:0], TDO, HOUT, and SYSCLKOUT				3	mA
		C Class Buffers - HPI, TSIP, UTOPIA, BOOTACTIVE, WDOUT, RESETSTAT, TIMO2, MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				3	mA
		RGMII pins				8	mA
		DDR pins				13.4	mA
I_{OZ}	Off-state output current	3.3-V pins		-10		20	uA
		RGMII pins		-10		10	uA
		DDR pins		-10		10	uA
T_C	Operating case temperature	commercial temperature		0		85	°C
		extended temperature(2)		-40		100	

(2) Extended temperature (A) range is available only on 500-MHz and 625-MHz devices.

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