1 C9230C100 TMS320C672x DSP ROM

1.1 Features

- **Contains the Following to Assist in Rapid Software Development and Faster Time-to-Market:**
  - **On-Chip Bootloader**
  - **Full-Feature Version of DSP/BIOS™ Operating System**
  - **Optimized Math Library (FastRTS)**
  - **Library of Commonly Used DSP Functions (DSPLIB)**
- **Applications:**
  - **Professional Audio**
    - **Mixers**
    - **Effects Boxes**
    - **Audio Synthesis**
    - **Instrument/Amp Modeling**
    - **Audio Conferencing**
    - **Audio Broadcast**
    - **Audio Encoder**
  - **Emerging Audio Applications**
  - **Biometrics**
  - **Medical**
  - **Industrial**

1.1.1 Description

The TMS320C672x is the next generation of Texas Instruments' TMS320C67x™ DSP generation of high-performance 32-/64-bit floating-point digital signal processors. The TMS320C672x includes the TMS320C6727, TMS320C6727B, TMS320C6726, TMS320C6726B, TMS320C6722, TMS320C6722B, and TMS320C6720 devices. The TMS320C672x ROM (named "C9230C100") contains a core set of TI's software collateral for assisting in rapid software development and faster time-to-market. The ROM contains an on-chip bootloader, a full-feature version of the DSP/BIOS™ operating system, an optimized math library (FastRTS), and a library of commonly used DSP functions (DSPLIB). Having features of a robust real-time operating system and common math and DSP functions present in the ROM gives the user application access to this functionality without absorbing the code size overhead within the application code. This leaves more code that can be utilized for enhanced application features.

Table 1-1 lists and describes the components that comprise the C9230C100 ROM.

Table 1-1. Components of the C9230C100 ROM

COMPONENT	DESCRIPTION
Bootloader (BOOT ROM)	On-chip bootloader
DSP/BIOS (V5.20)	DSP/BIOS real-time operating system
FastRTS (V1.20)	Optimized math library containing common math functions such as tangent/arctangent, cosine, sine, etc.
DSPLIB (V2.00)	Optimized set of commonly used DSP functions such as FIRs, FFTs, vector MAX, vector MIN, etc.

1.1.2 Determining ROM Revision

The ROM version can be found at ROM memory location 0x0000 000C. The current revision is 0xC923 0C10.

Contents

2 Overview

2.1 Components of the C9230C100 ROM

2.1.1 Bootloader (BOOT ROM)

The boot options listed in Table 2-1 are supported by the on-chip bootloader.

Table 2-1. Boot Options Supported by the On-Chip Bootloader

BOOT MODE	REMARKS
HPI	Parallel boot option. Supports mux/non-mux, byte/word address, half/full word accesses
Parallel Flash	Supports 8-/16-bit parallel flash
SPI0 Master	4-wire SPI, standard protocol. 16 bits of address/8 bits of data.
SPI0 Slave	DSP sends/receives 16-bit data.
I2C1 Master	Standard I2C bus protocol. 16 bits of address/8 bits of data.
I2C1 Slave	Addressing done through the I2C protocol. The DSP sends/receives 8-bit data.

The selection of the boot mode is based on the status of the TMS320C672x device boot pins. Pin configuration for each supported boot mode is given in Table 2-2. The status of these pins is captured on the rising edge of device reset into internal registers, which will be read later by the bootloader. The “X” entries in Table 2-2 are further used to configure the HPI operational modes.

Table 2-2. Boot Mode Selection

BOOT MODE	$\overline{\text{HCS}}$	SPI0SOMI	SPI0SIMO	SPI0CLK
HPI	0	X	X	X
Parallel Flash	1	0	1	0
SPI0 Master	1	0	0	1
SPI0 Slave	1	0	1	1
I2C1 Master	1	1	0	1
I2C1 Slave	1	1	1	1

The functionality of the bootloader can be extended by using a secondary bootloader, which is loaded into the device from external memory and executed during the boot-up process. Various boot procedures, capabilities, functional descriptions, error detection, and tools provided are explained in the Using the TMS320C672x Bootloader Application Report (literature number SPRAA69).

2.1.1.1 Cache Considerations

The ROM bootloader software disables the cache at the start of boot and does not invalidate or enable cache prior to branching to the start of application code. Therefore, the application must take the responsibility to invalidate and enable cache, if cache is used. For more details, see Using the TMS320C672x Bootloader Application Report (literature number SPRAA69).

2.1.2 Operating System (DSP/BIOS)

DSP/BIOS version 5.20 is a full-feature version of the scalable DSP/BIOS kernel providing real-time scheduling, synchronization, and real-time instrumentation. This ROMed version of DSP/BIOS provides a multitasking manager, trace manager, system services manager, stream I/O manager, semaphore manager, real-time data exchanger, memory segment manager, event log manager and other components of the DSP/BIOS OS. These features in the TMS320C672x ROM can be utilized during both software development and system usage. Users can seamlessly migrate from initial software development using DSP/BIOS configuration tools for rapid software development and debug, to fine-tuning application code for size and speed using ROMed DSP/BIOS components by linking the appropriate ROM image with their code. No explicit changes to the application code or previously defined DSP/BIOS configuration files is required.

For documentation or download of DSP/BIOS 5.20.02, 5.20.03, or 5.20.04, see the DSP/BIOS Product Release web site (link to https://www-a.ti.com/downloads/sds_support/targetcontent/bios/index.html).

2.1.3 Optimized Math Library (FastRTS)

The Optimized DSP Math Library (a subset of rts6700.lib) for trigonometric and algebraic functions is provided in the TMS320C672x ROM. These functions are extensively used by general-purpose DSP algorithms. For further information, refer to the TMS320C67x FastRTS Library Programmer's Reference (literature number SPRU100).

2.1.4 Digital Signal Processing Library (DSPLIB)

DSPLIB is an optimized floating-point DSP Function Library for C programmers using TMS320C672x devices. It includes C-callable, assembly-optimized general-purpose signal-processing routines. These routines are typically used in computationally intensive real-time applications where optimal execution speed is critical. By using these routines, you can achieve execution speeds considerably faster than equivalent code written in standard ANSI C language. An application can further decrease execution time by taking advantage of decreased access time to DSPLIB routines in ROM.

For all ROM components DSP/BIOS, FastRTS, DSPLIB, no explicit changes to user application code is required to migrate from using non-ROM based versions of these software components to making full use of the ROM contents. All references are resolved at link stage of software build.

For more information about DSPLIB, see the TMS320C67x DSP Library Programmer's Reference Guide (literature number SPRU657).

2.2 Accessing ROM Content

Accessing the contents of the TMS320C672x ROM is accomplished by linking a set of predefined libraries and objects with user application code. The components are independent; for example, an application could use DSP/BIOS from ROM, but use FastRTS linked directly with the application code in RAM.

The memory map of the ROM contents is shown in Table 2-3.

Table 2-3. TMS320C672x ROM (C9230C100) Memory Map

ADDRESS	CONTENT
0x0000 0000 – 0x0001 FFFF	On-Chip Bootloader
0x0002 0000 – 0x0002 BFFF	DSPLIB
0x0002 C000 – 0x0002 FFFF	FastRTS
0x0003 0000 – 0x0005 FFFF	DSP/BIOS
0x1000 0000 – 0x1000 0FFF	Reserved at Boot for Bootloader
0x1000 1000 – 0x1000 1AFF	DSP/BIOS RAM
0x1000 1B00 – 0x1000 1C00	FastRTS RAM

2.2.1 Accessing DSPLIB and FastRTS

An application can incorporate calls to the ROMed version of DSPLIB and FastRTS functions by including predefined libraries (c67xdsplibr.lib and fastrts67xr.lib) in the build options to the linker and defining the address ranges listed in the ROM Memory Map in the linker command file.

A sample linker command file to access the code for DSPLIB and FastRTS might read as follows:

```
-c
-heap  0x2000
-stack 0x4000
-l fastrts67xr.lib          /* Include references to ROMed library content */
-l c67xdsplibr.lib

/* SPECIFY THE SYSTEM MEMORY MAP */

MEMORY
{
    IROM_BOOT:       o = 00000000h   l = 00020000h
    IROM_DSPLIB:     o = 00020000h   l = 0000C000h
    IROM_FASTRTS:    o = 0002C000h   l = 00004000h
    IROM_BIOS:       o = 00030000h   l = 00030000h
    IRAM_BOOT:       o = 10000000h   l = 00001000h
    IRAM_BIOS:       o = 10001000h   l = 00000B00h
    IRAM_RESERVED:   o = 10001B00h   l = 00000100h
    IRAM_STACK:      o = 10001C00h   l = 00000800h
    IRAM:            o = 10002400h   l = 0003DC00h
    BOOTSRAM:        o = 90000000h   l = 10000000h
    SDRAM:           o = 80000000h   l = 10000000h
}


SECTIONS
{
  /*-----------------------------------------------------------*/
  /* Sample allocation for Compiler generated sections that may  */
  /* be defined in application code.                           */
  /*-----------------------------------------------------------*/
    .text        >       SDRAM
    .stack       >       IRAM
    .bss         >       IRAM
    .cinit       >       SDRAM
    .pinit       >       SDRAM
    .cio         >       IRAM
    .const       >       IRAM
    .data        >       IRAM
    .switch      >       SDRAM
    .sysmem      >       IRAM
    .far         >       SDRAM

}
```

No other requirements are needed to access content for DSPLIB and FastRTS. A brief example has been included in the file attached to this document. The examples are located in the folder, “UsingROMApplications”, which will be created when the accompanying .zip file, http://www-s.ti.com/sc/psheets/sprc203/sprc203.zip, is expanded. The library files, c67xdsplibR.lib and fastrts67xR.lib, are also included with this attachment.

2.2.2 Accessing DSP/BIOS

Accessing the DSP/BIOS content requires no change to the application code. Use the graphical configuration tool (or text editor) to set 'bios.GBL.LINKWITHROM = 1' in the configuration file (prog.tcf). The generated linker command file (progcfg.cmd) will reference the DSP/BIOS code in ROM and reserve the associated RAM.

This version of ROM is only compatible with DSP/BIOS 5.20.xx.

2.3 ROM Patches

Due to bug fixes and upgrades, it may be necessary to patch the software functionality found in the ROM. All patches to the ROM will be implemented by linking the software patch in the final application code. The system designer should be careful to consider reserving a portion of system memory in the linker command file to allow for ROM patches.

2.3.1 Patches to Bootloader/System Initialization

Patches to the ROM content for the bootloader section of the code will be delivered as libraries. The libraries will contain functionality to replace defective ROM code.

2.3.1.1 Patch Required

The current ROM version, C9230C100, contains a system initialization error. A patch is currently available which should be applied for all applications developed on devices with this ROM version. The patch MUST be applied regardless of whether or not the user application code explicitly references any of the applications present in the internal ROM of the device.

Please note that this patch requires a minimum of 0x2048 32-bit words in application code/data space. Applications written all or partially in C/C++ require no code changes to apply this system patch. Including the object applySystemPatch.obj and the library c672xSystemPatchV2_00_00.lib when the application is linked is sufficient. These files can be included by a linker command file or by using the project management features of Code Composer Studio™ (CCS). No patch is currently available for assembly-only applications.

To download this software patch and an example linker command file, go to:

http://www-s.ti.com/sc/psheets/sprc203/sprc203.zip

When the zip file is expanded , the system patch will be found in a sub-directory labeled “SystemPatch”.

2.3.2 DSPLIB and FastRTS

Patches to the ROM content for DSPLIB and FastRTS will be provided as new versions of the libraries c67xdsplibr.lib and fastrts67xr.lib, respectively. The libraries provided will contain new content to only replace the functions in ROM for which a software update is needed. All other content will be accessed from the ROM as previously defined. DSPLIB and FastRTS patches will be provided as downloaded content from the web.

No patch is required at this time.

2.3.3 DSP/BIOS

Patches to DSP/BIOS will be provided as downloadable software updates via the web. As with all patches for ROM content, applying these patches will result in added content to the code/data space for the application.

No patch is required at this time.

3 Revision History

This data sheet revision history highlights the technical changes made to the SPRS277B device-specific data sheet to make it an SPRS277C revision.

Scope: Added silicon revision 1.2 devices: TMS320C6727B, TMS320C6726B, TMS320C6722B, and TMS320C6720.

ADDS/CHANGES/DELETES
Section 1.1.1, Description: • added silicon revision 1.2 devices (TMS320C6727B, TMS320C6726B, TMS320C6722B, and TMS320C6720) to the list of TMS320C672x devices

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