REVISION STATUS OF SHEETS

REV										
SH										
REV	C	C	A	A1	A	C	C	C2	C	C2
SH	21	22	23	24	25	26	27	28	29	30
REV	A	A	A	D	A	A	A	A	A	A
SH	11	12	13	14	15	16	17	18	19	20
REV	D	D	D	D	D	D	D	B	A	A
SH	1	2	3	4	5	6	7	8	9	10

NEXT ASSY	USED ON			
APPLICATION				
		DWN	J.A.C.	DATE 02/05/2016
		CHK	T.W.K.	DATE 02/05/2016
		ENGR	J.A.C.	DATE 02/05/2016
		ENGR-MGR	J.A.C.	DATE 02/05/2016
		QA	C.M.D.	DATE 02/05/2016
		MFG	J.A.C.	DATE 02/05/2016
		RLSE	J.A.C.	DATE 02/05/2016

TEXAS INSTRUMENTS INCORPORATED

Title: “DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board”

Page Contents: TITLE PAGE

Size: B DOC NO: 518202 REV: D

Date: Friday, September 08, 2017 Sheet 1 of 30

ECN Number	518200-E002			
Date Requested	10/20/2016			
Requester	Robert E.			
Approvals	Tony C.			
Assembly Number	518200-0001			
Current Assembly Rev	B			
New Assembly Rev	C			
Date Implemented	10/24/2016			
Implentation notes				
				EEPROM will bump to Rev A.2

Item#	**Init Date**	**Priority**	**Status**	**Description**
				ASSY, PWB, LOGIC Rev B TO C
DR13				Add silkscreen for JP1
				Pin 1 - CANH
				Pin 2 - CANL
DR14				NA
DR15				SHEET 2:
				Change CDCEL925, U114 power raile to VPO_L3_1V8
				SHEET 28:
				U43 From 104715-0001R-TI to 104715-0002R-TI
				Create new part # 104715-0002R-TI for updated OTP
				U42 From 104714-0135R-TI to 104714-0136R-TI
				Create new part # 104714-0136R-TI for updated OTP
				Sheet 29
				Change C528 From 102963-0101R 10uF To 104448-0220R 2.2uF
DR16				Update J6 Entry symobl to v.44
DR17				Remove the Lead Free and replace with RoHS Exempt
DR18				SHEET 21
				Add EVM_12V to P10 pins 1,3
				Add CSI2_GPIO_PWMA to pin 6
				Add CSI2_GPIO_PWMB to pin 8
				SHEET 26
				Add R564, R565 R0201-NOPOP
				Map H_MMC3_D4 to EHRPWM3A
				Map H_MMC3_D5 to EHRPWM3B
DR19				SHEET 3: Change VPP to LDO at 2V vs FET
				Delete Q6
				Add U133 - 104954-0001R
				Add R562 - 102145-3163R, 31.6k 1%
				Add R563 - 102145-4703R, 47K 1%
DR20				EEPROM will bump to Rev A.2
DR21				SHEET 27: Add bleed circuit for 3v3 rail
				Add Q6 - 102437-0001R
				Add Q6 - 102159-0001R
				Add R826 - 100688-3650R
				Add R827 - 101370-1003R

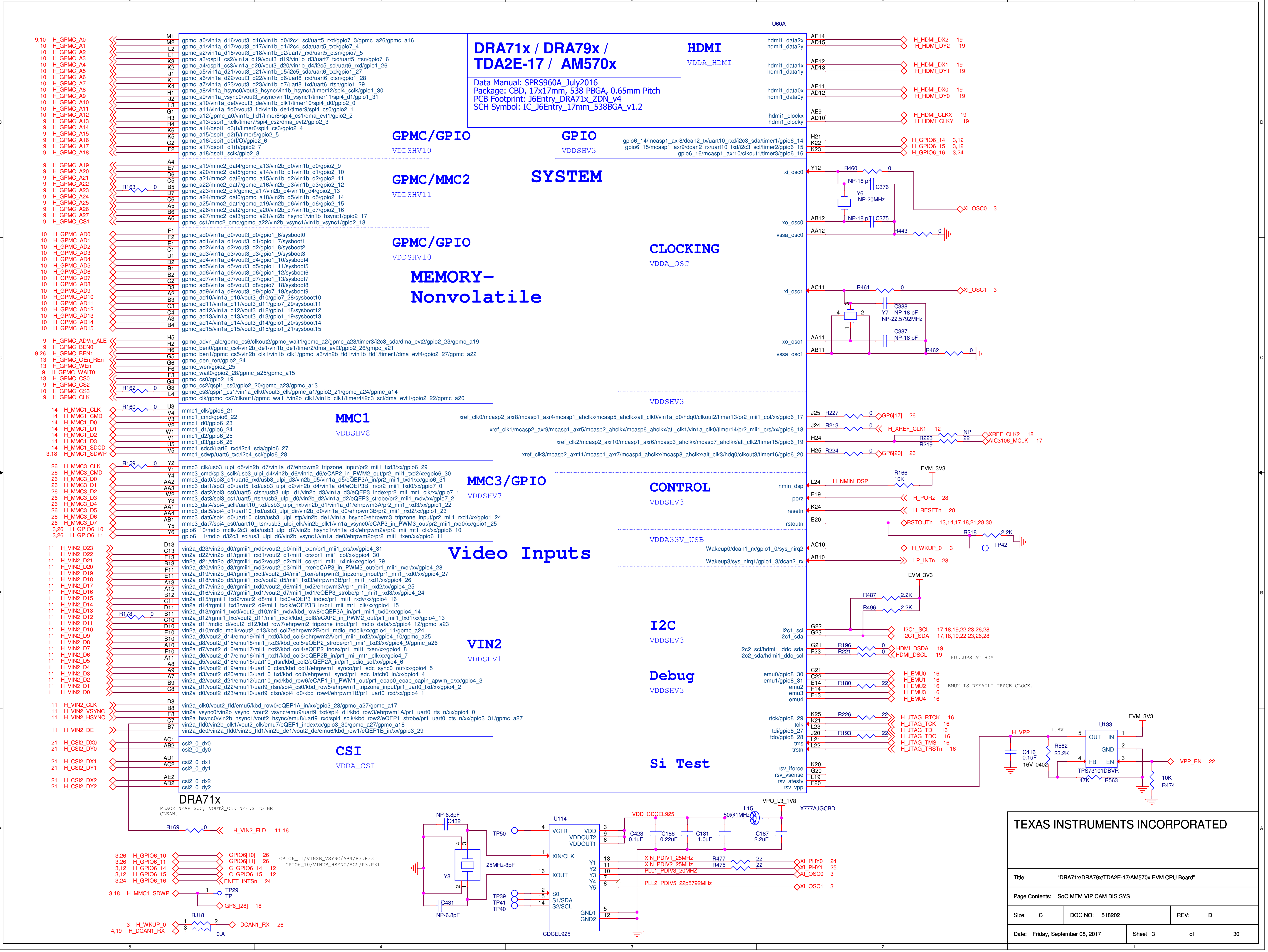
REV C1: ADD ERRATA SHEET 31

REV C2:
UPDATE LP87xx PART NUMBERS FOR CORRECT OTP.
UPDATE AUTOMATION POWER CONTROL NOTE

REV D:
UPDATE SOC SYMBOL TO v1.2
R562 From 102145-3163R to 102145-2323R (31.6K to 23.2K for 1.8V instead of 2.0V on VPP)
ENCORPORATE ERRATA FOR GPIO6_16/GPIO6_14 SIGNAL SWAP
UPDATE SD CARD FOOTPRINT FOR NON-EOL PART

TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"
Page Contents: NOTES
Size: C DOC NO: 518202 REV: D
Date: Friday, September 08, 2017 Sheet 2 of 30

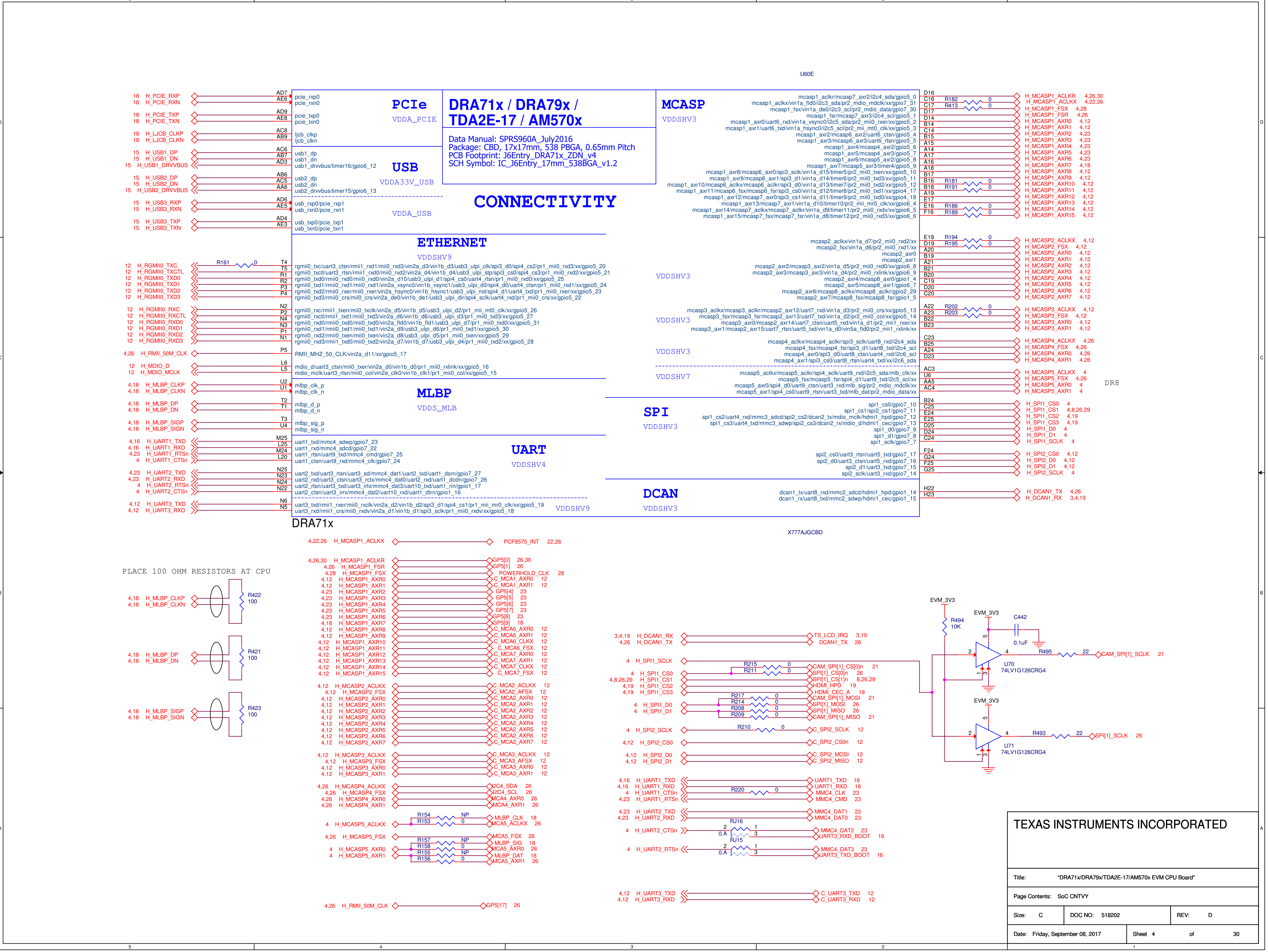


TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

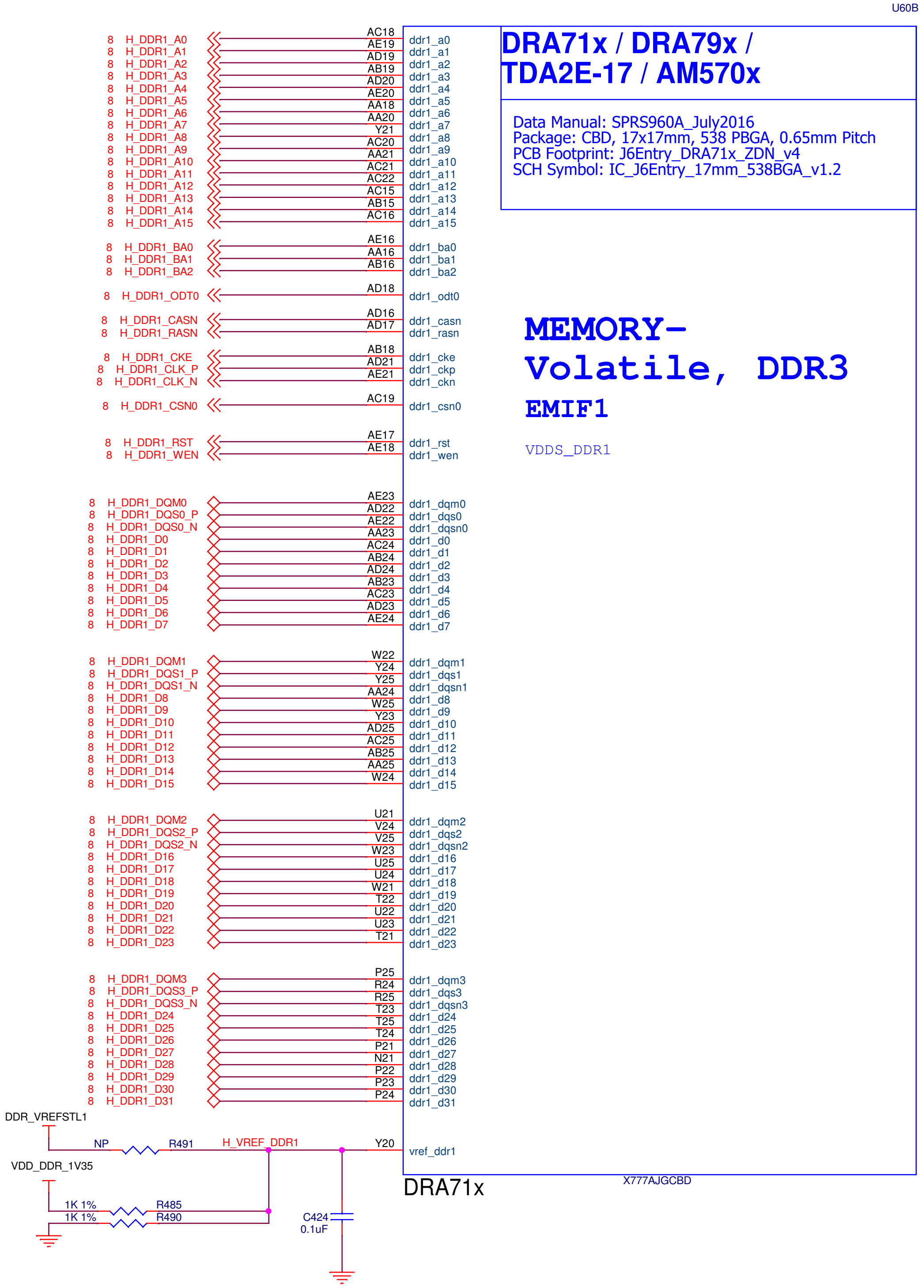
Page Contents: SoC MEM VIP CAM DIS SYS

Size: C	DOC NO: 518202	REV: D
Date: Friday, September 08, 2017	Sheet 3 of 30	

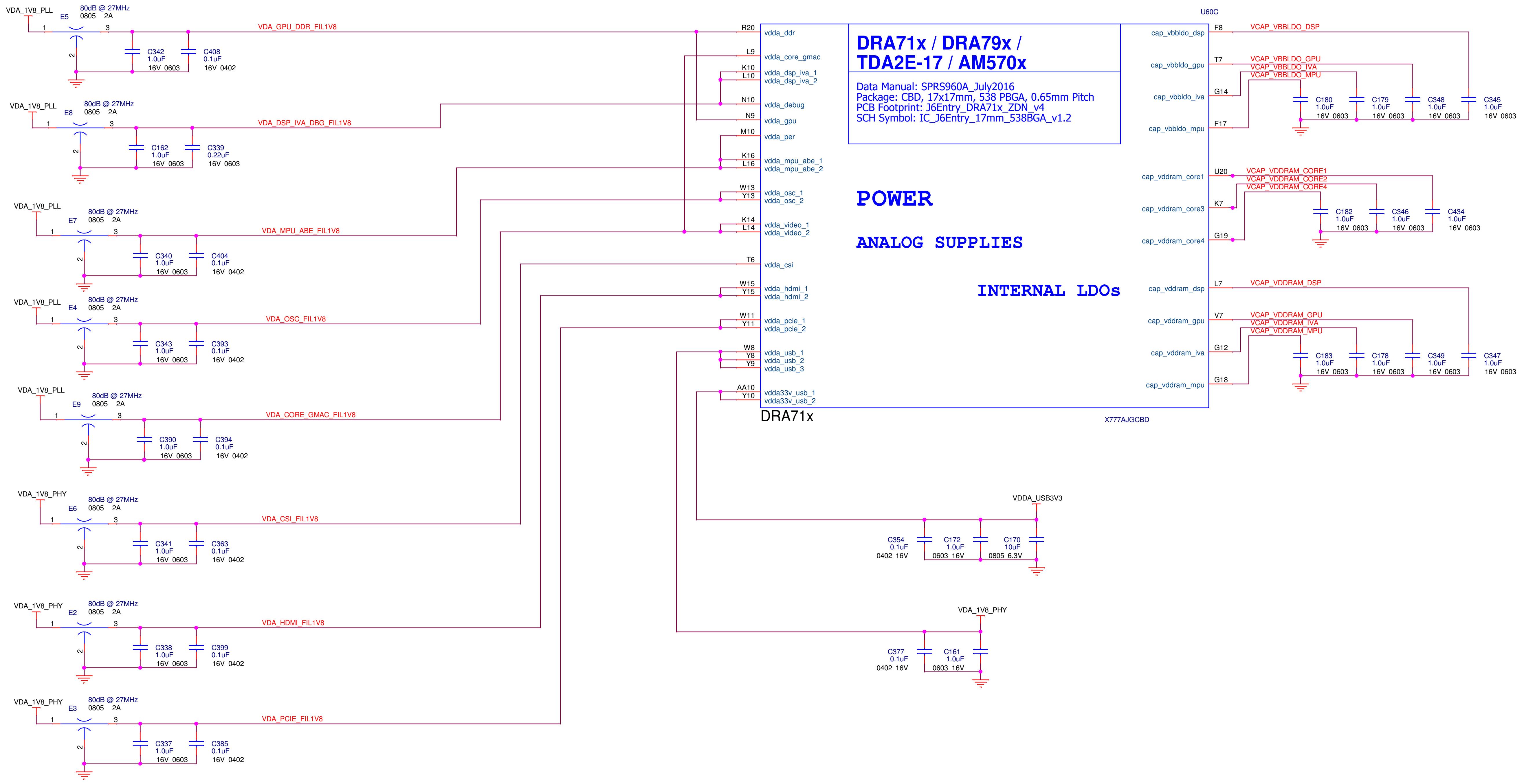


TEXAS INSTRUMENTS INCORPORATED

Title:	"DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents:	SoC CNTVY		
Size: C	DOC NO: 518202	REV: D	
Date: Friday, September 08, 2017	Sheet 4	of	30



TEXAS INSTRUMENTS INCORPORATED			
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"			
Page Contents: SoC DDR			
Size: C	DOC NO: 518202	REV: D	
Date: Friday, September 08, 2017	Sheet 5	of	30



TEXAS INSTRUMENTS INCORPORATED

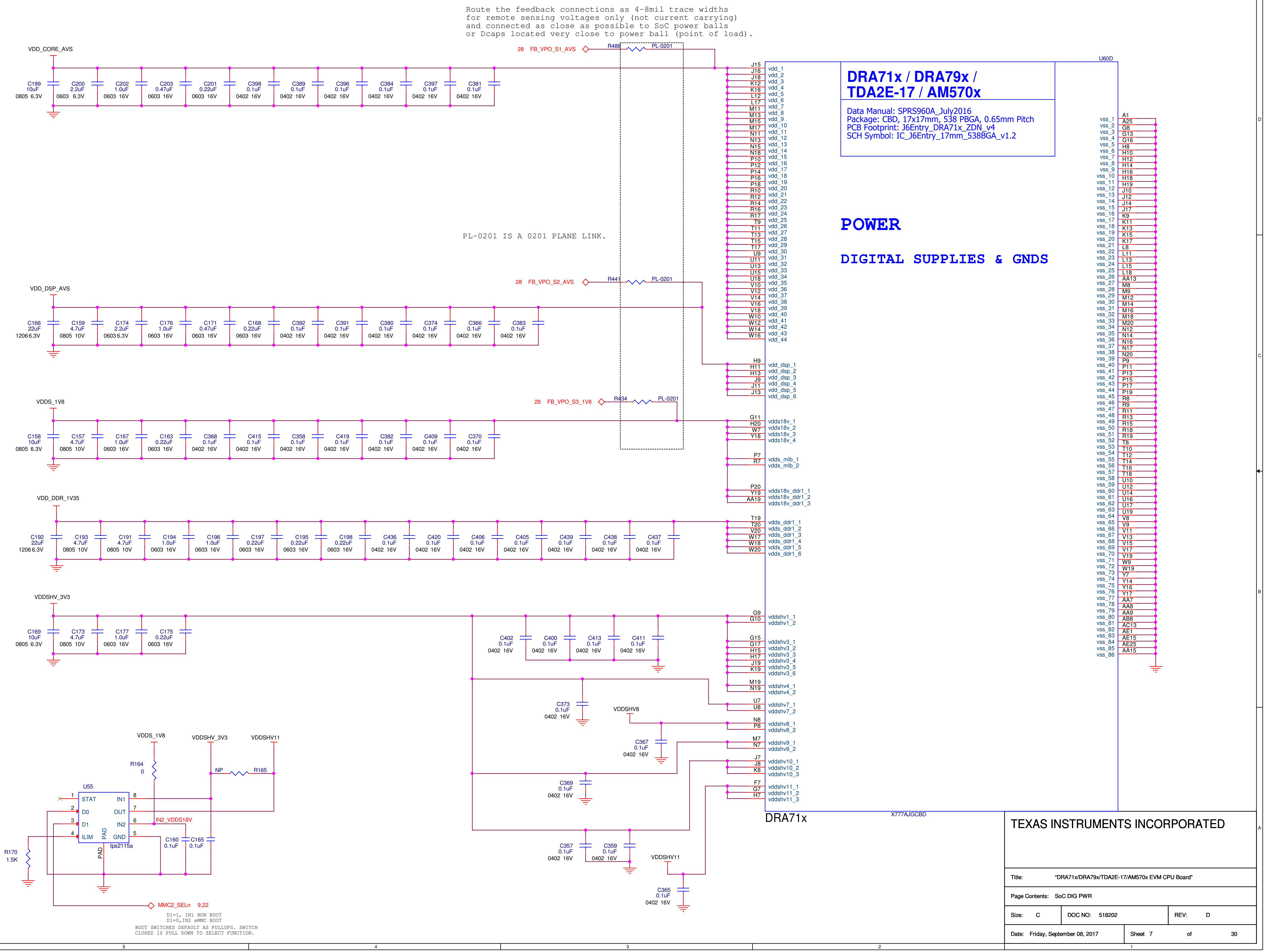
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: SoC ANA PWR

Size: C | DOC NO: 518202 | REV: D

Date: Friday, September 08, 2017 | Sheet 6 of 30

Route the feedback connections as 4-8mil trace widths
for remote sensing voltages only (not current carrying)
and connected as close as possible to SoC power balls
or Dcaps located very close to power ball (point of load).

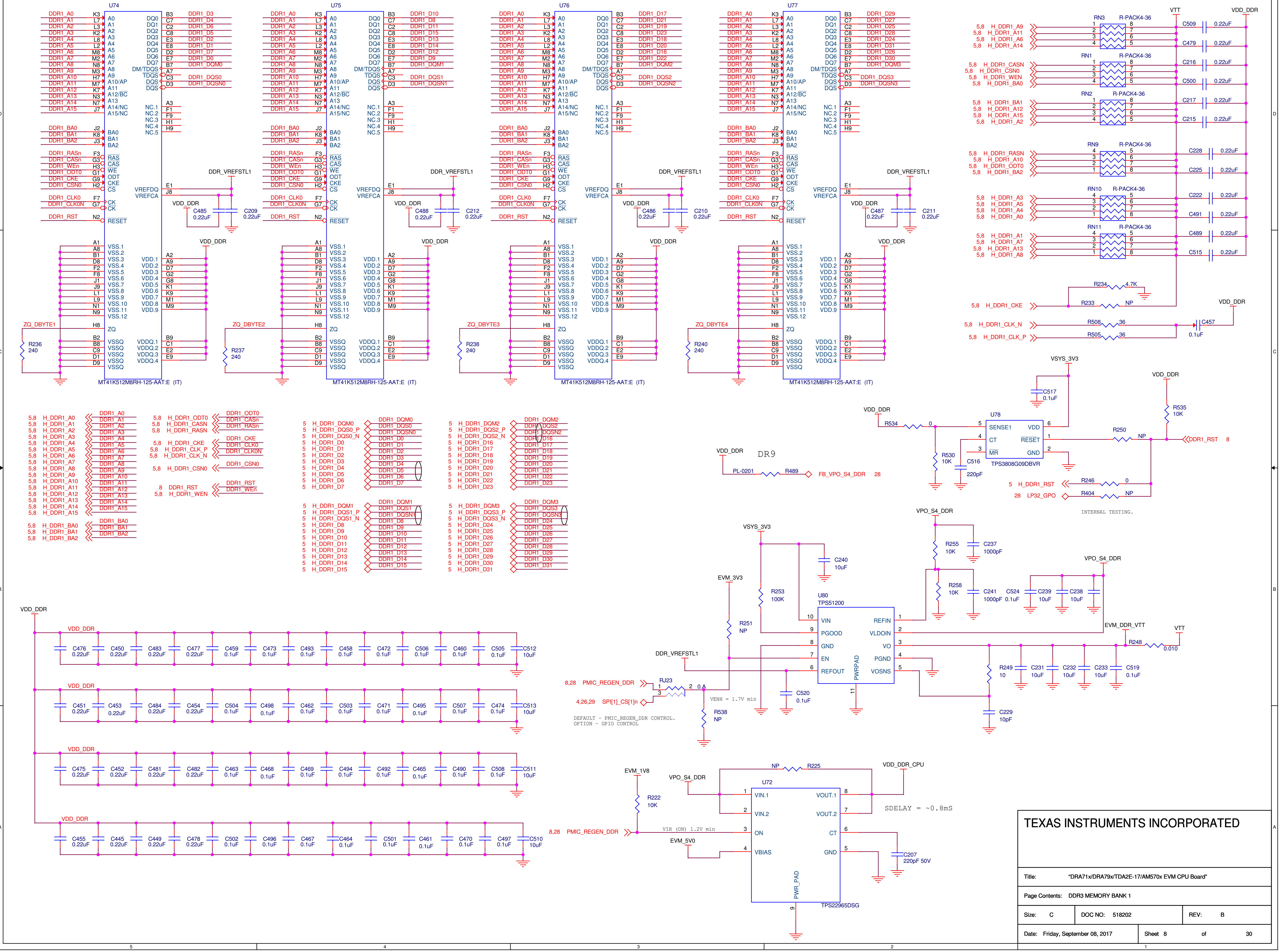


PL-0201 IS A 0201 PLANE LINK.

D1=1, IN1 NOR BOOT
D1=0,IN2 eMMC BOOT
BOOT SWITCHES DEFAULT AS PULLUPS. SWITCH
CLOSED IS PULL DOWN TO SELECT FUNCTION.

TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents: SoC DIG PWR		
Size: C	DOC NO: 518202	REV: D
Date: Friday, September 08, 2017	Sheet 7	of 30



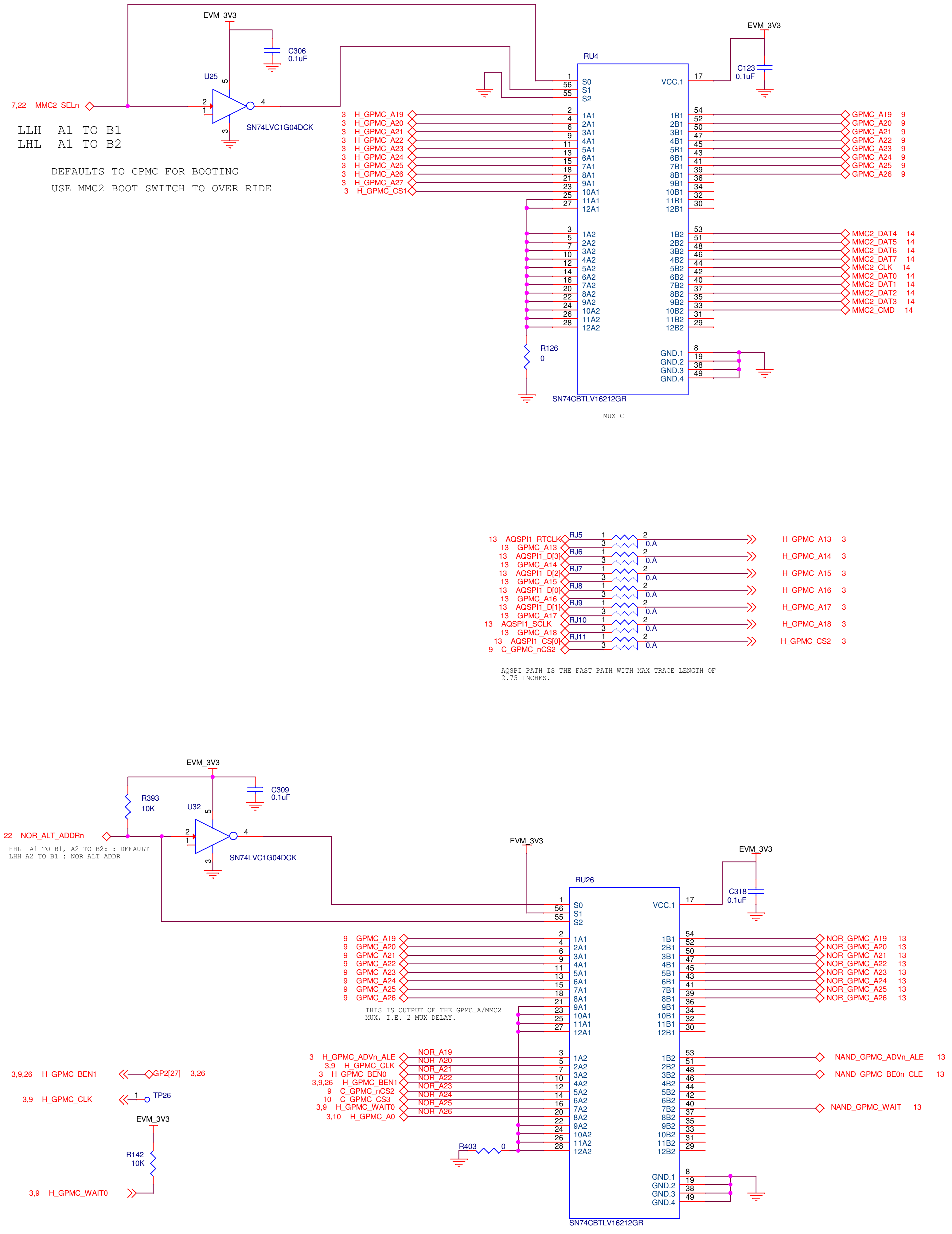
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: DDR3 MEMORY BANK 1

Size: C DOC NO: 518202 REV: B

Date: Friday, September 08, 2017 Sheet 8 of 30



gpmc_a[19]	mmc2_dat[4]
gpmc_a[20]	mmc2_dat[5]
gpmc_a[21]	mmc2_dat[6]
gpmc_a[22]	mmc2_dat[7]
gpmc_a[23]	mmc2_clk
gpmc_a[24]	mmc2_dat[0]
gpmc_a[25]	mmc2_dat[1]
gpmc_a[26]	mmc2_dat[2]
gpmc_a[27]	mmc2_dat[3]
gpmc_cs[1]	mmc2_cmd

TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

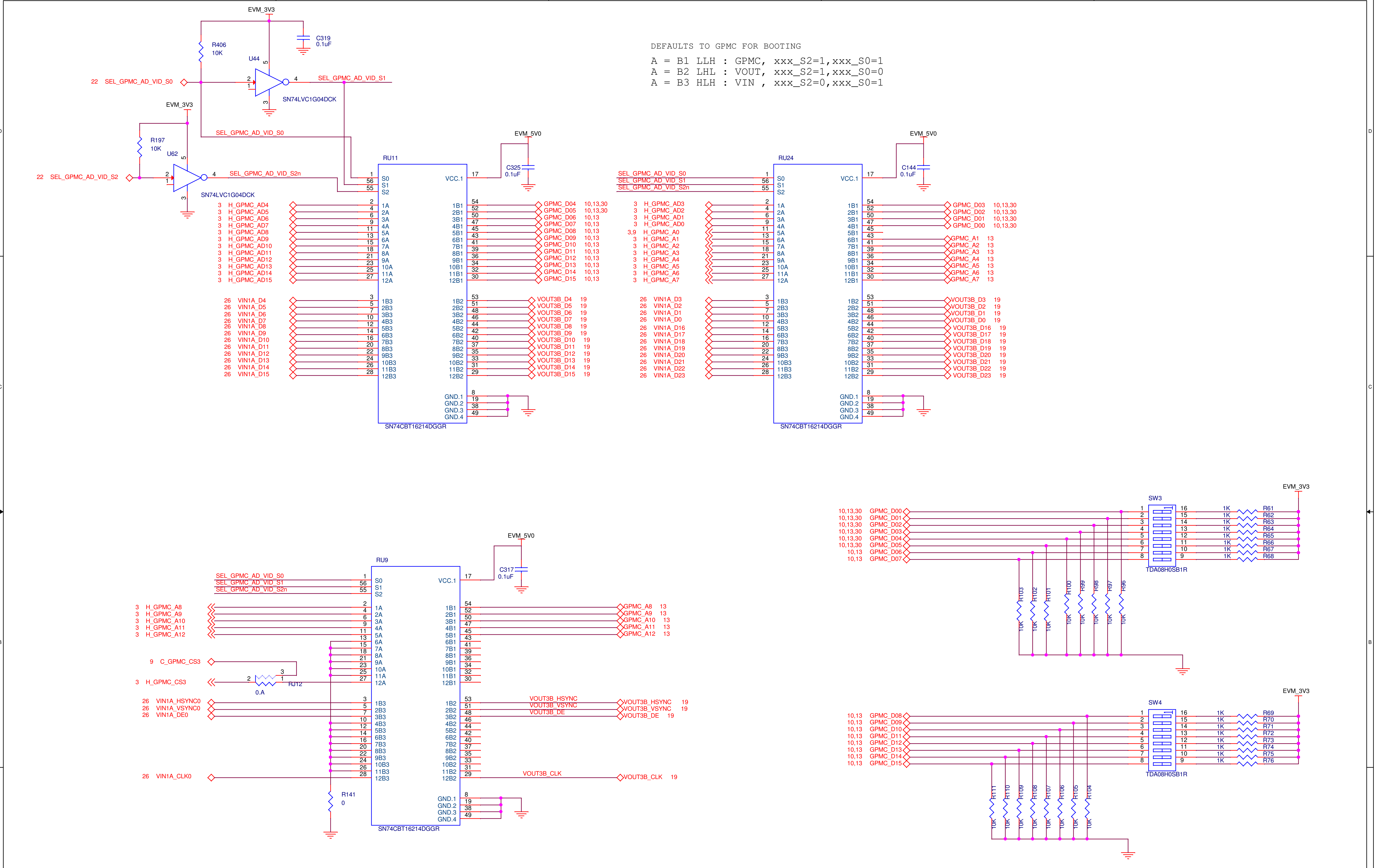
Page Contents: MUX A/C QSPI/EMMC/GPMX

Size: C DOC NO: 518202 REV: A

Date: Friday, September 08, 2017 Sheet 9 of 30

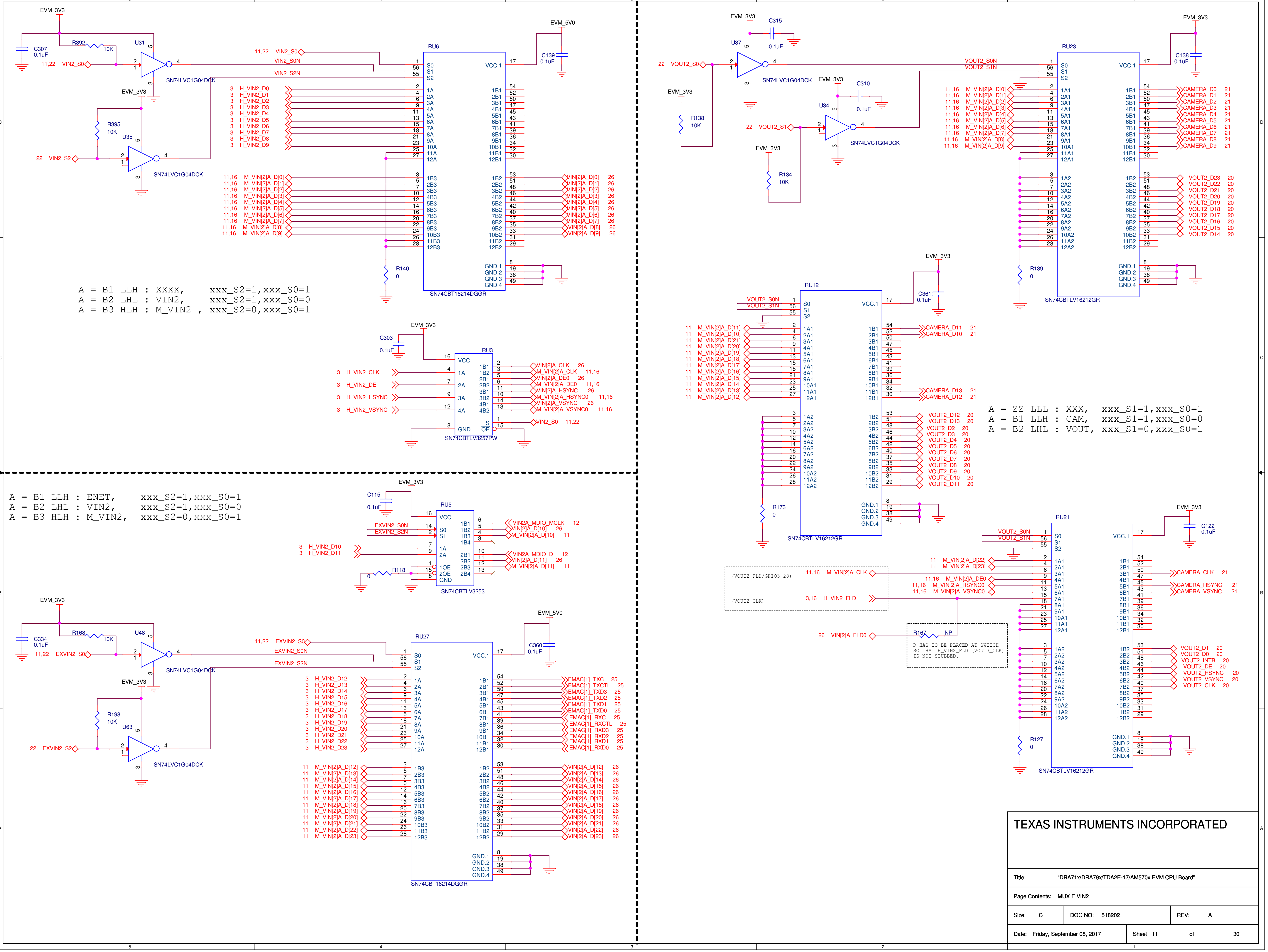
DEFAULTS TO GPMC FOR BOOTING

A = B1 LLH : GPMC, xxx_S2=1,xxx_S0=1
A = B2 LHL : VOUT, xxx_S2=1,xxx_S0=0
A = B3 HLH : VIN , xxx_S2=0,xxx_S0=1



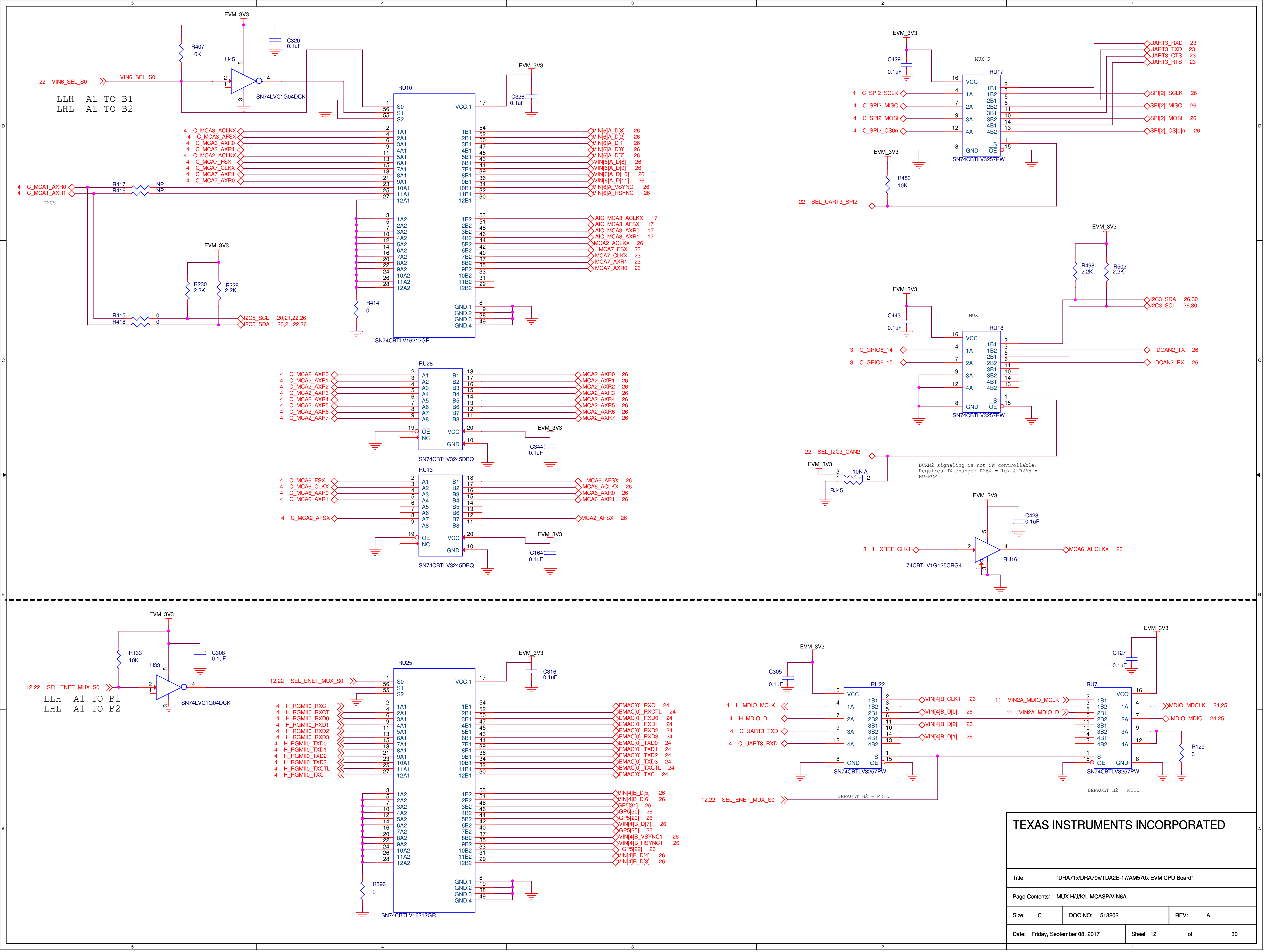
TEXAS INSTRUMENTS INCORPORATED

Title:	"DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"
Page Contents:	MUX B VOUT3/GPMC
Size: C	DOC NO: 518202	REV: A
Date: Friday, September 08, 2017	Sheet 10 of 30



TEXAS INSTRUMENTS INCORPORATED

Title:	"DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents:	MUX E VIN2		
Size: C	DOC NO: 518202		REV: A
Date: Friday, September 08, 2017	Sheet 11	of	30



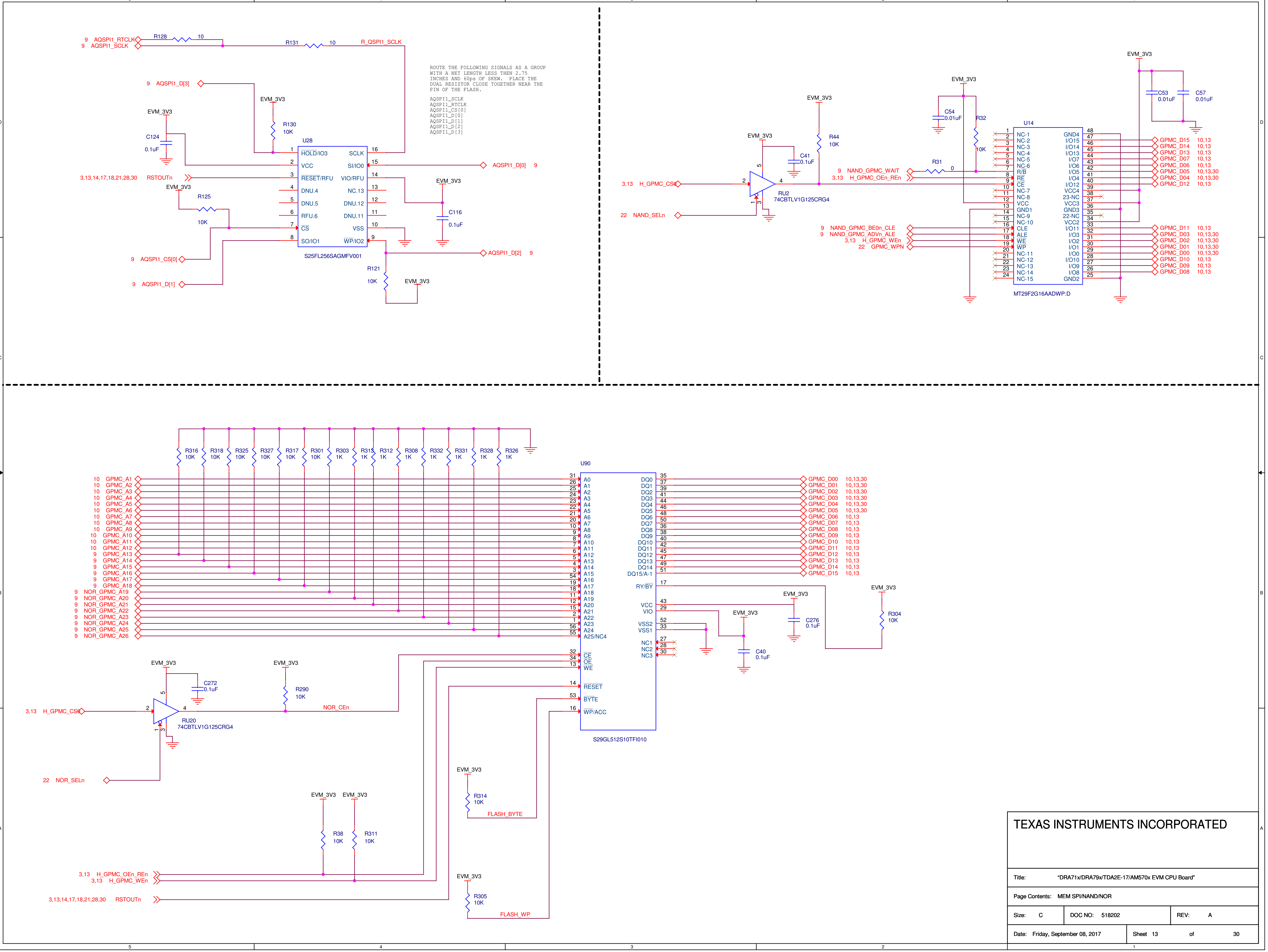
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: MUX H/J/K/L MCASP/VIN6A

Size: C DOC NO: 518202 REV: A

Date: Friday, September 08, 2017 Sheet 12 of 30



ROUTE THE FOLLOWING SIGNALS AS A GROUP WITH A NET LENGTH LESS THEN 2.75 INCHES AND 60ps OF SKEW. PLACE THE DUAL RESISTOR CLOSE TOGETHER NEAR THE PIN OF THE FLASH.

AQSPI1_SCLK
AQSPI1_RTCLK
AQSPI1_CS[0]
AQSPI1_D[0]
AQSPI1_D[1]
AQSPI1_D[2]
AQSPI1_D[3]

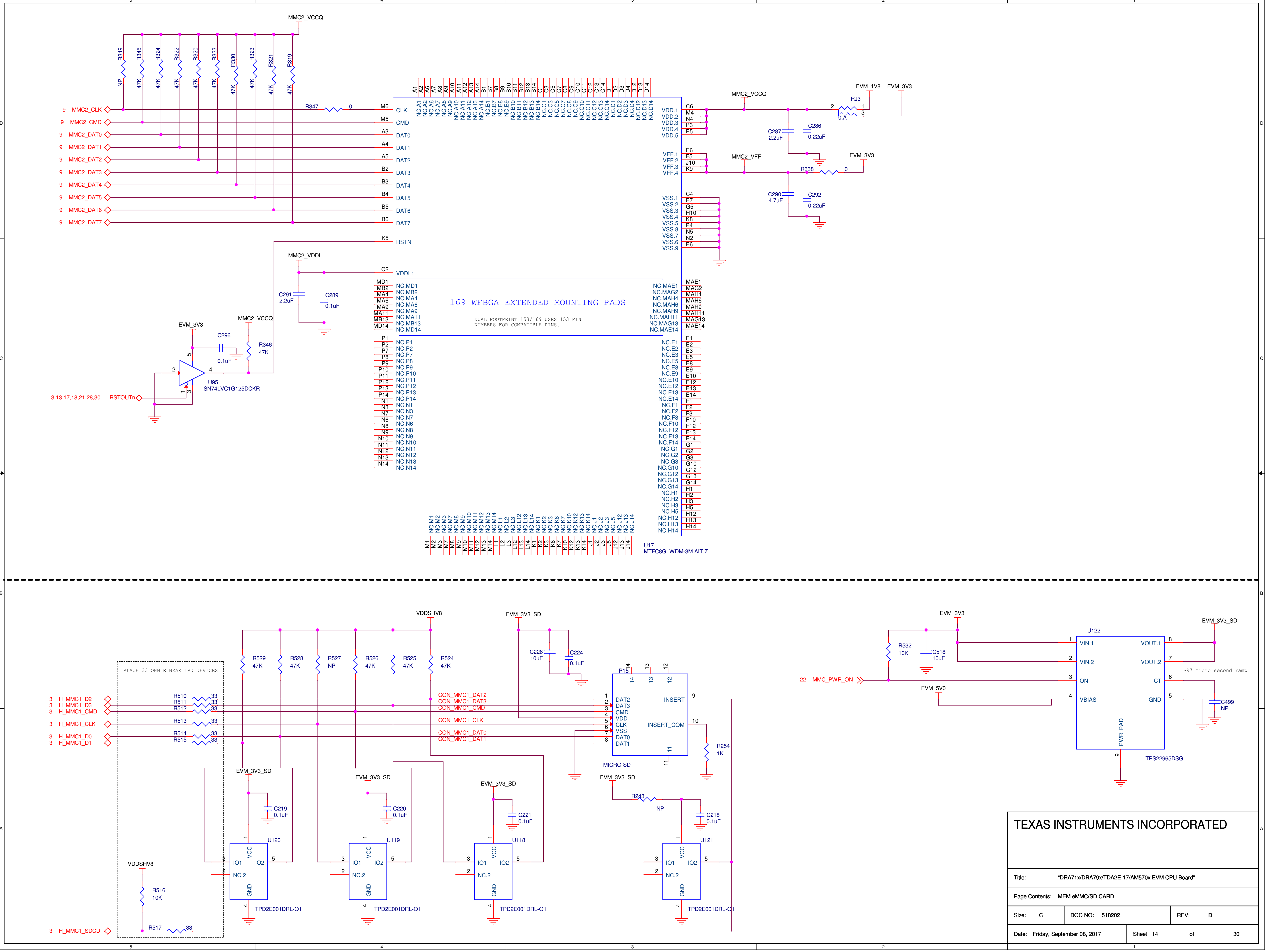
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: MEM SPI/NAND/NOR

Size: C DOC NO: 518202 REV: A

Date: Friday, September 08, 2017 Sheet 13 of 30

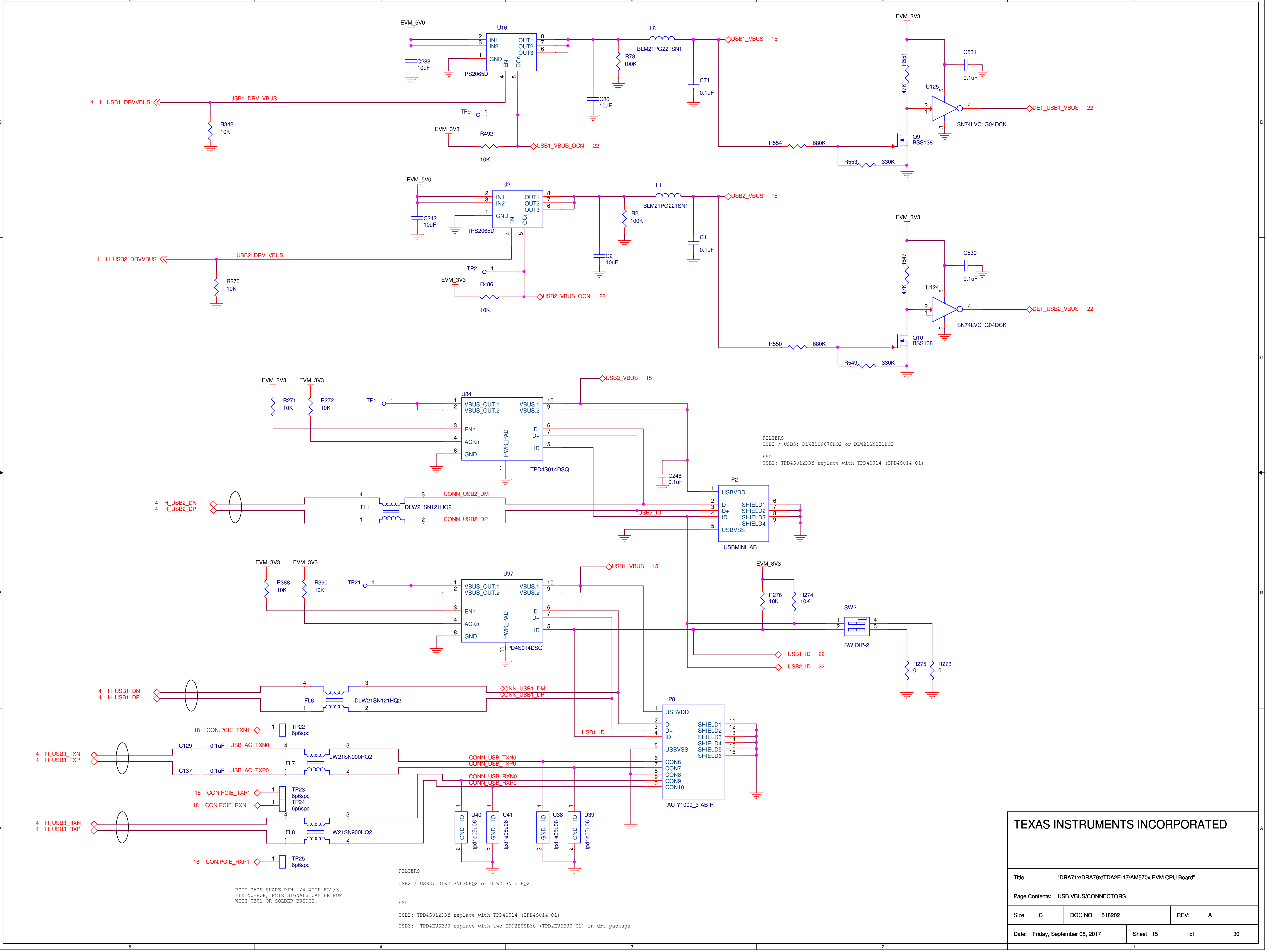


TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: MEM eMMC/SD CARD

Size: C	DOC NO: 518202	REV: D
Date: Friday, September 08, 2017	Sheet 14 of 30	



FILTERS
USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2

ESD
USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)

PCIE PADS SHARE PIN 1/4 WITH FL2/3.
FLx NO-POP, PCIE SIGNALS CAN BE POP
WITH 0201 OR SOLDER BRIDGE.

FILTERS

USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2

ESD

USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)

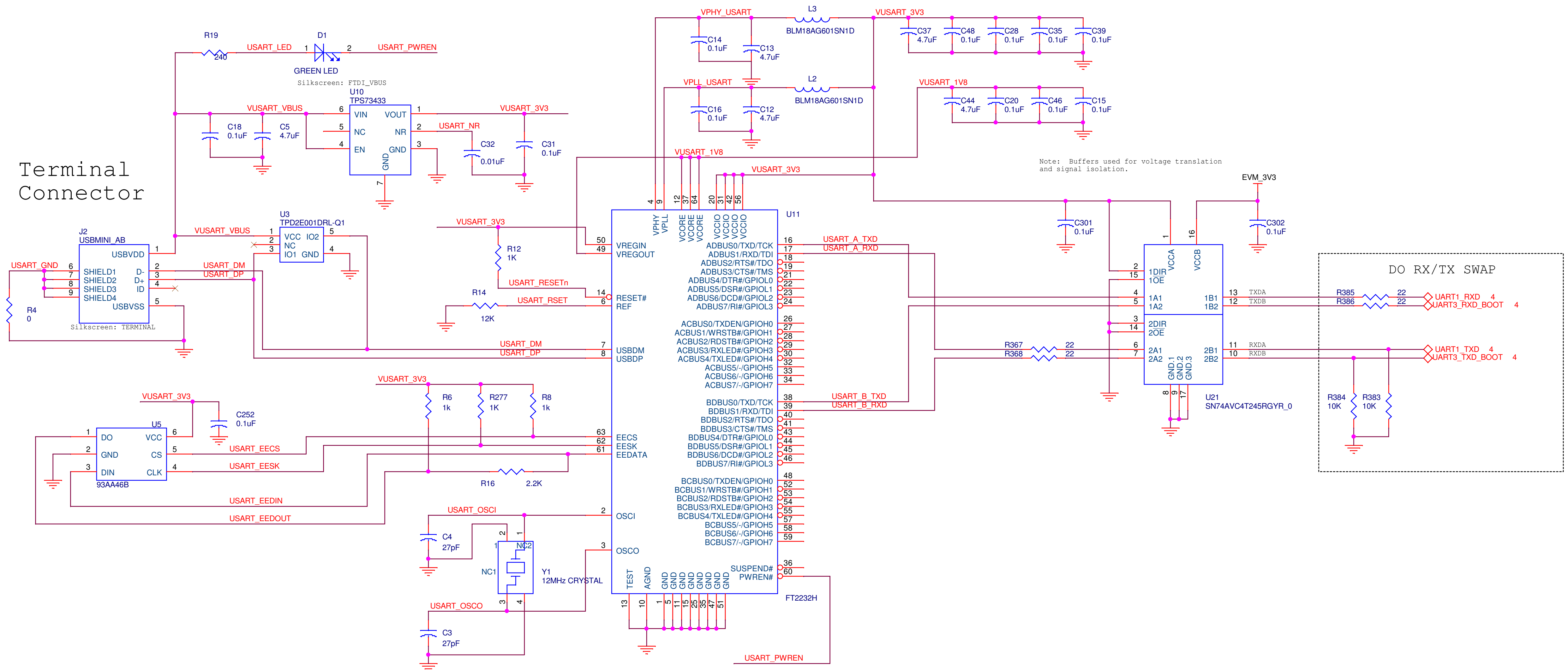
USB3: TPD4EUSB30 replace with two TPD2EUSB30 (TPD2EUSB30-Q1) in drt package

TEXAS INSTRUMENTS INCORPORATED

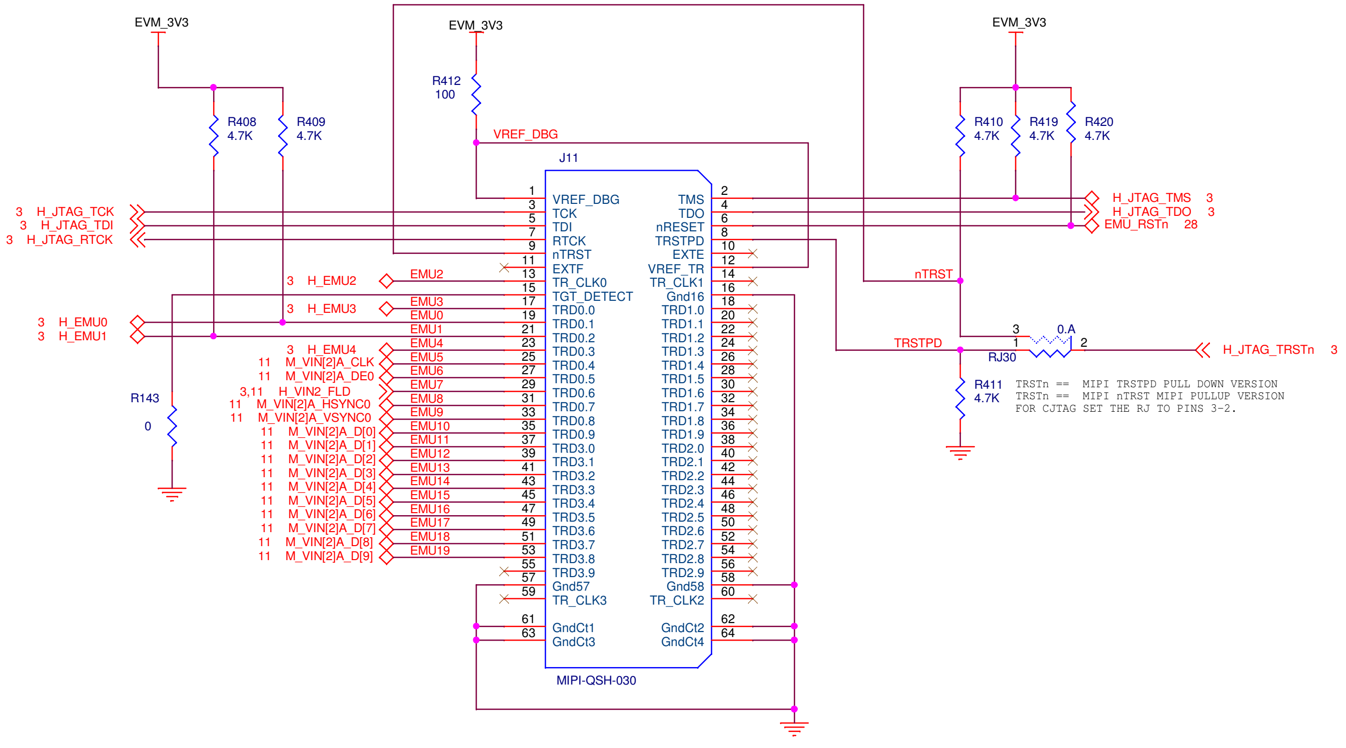
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: USB VBUS/CONNECTORS

Size: C	DOC NO: 518202	REV: A
Date: Friday, September 08, 2017	Sheet 15 of 30	



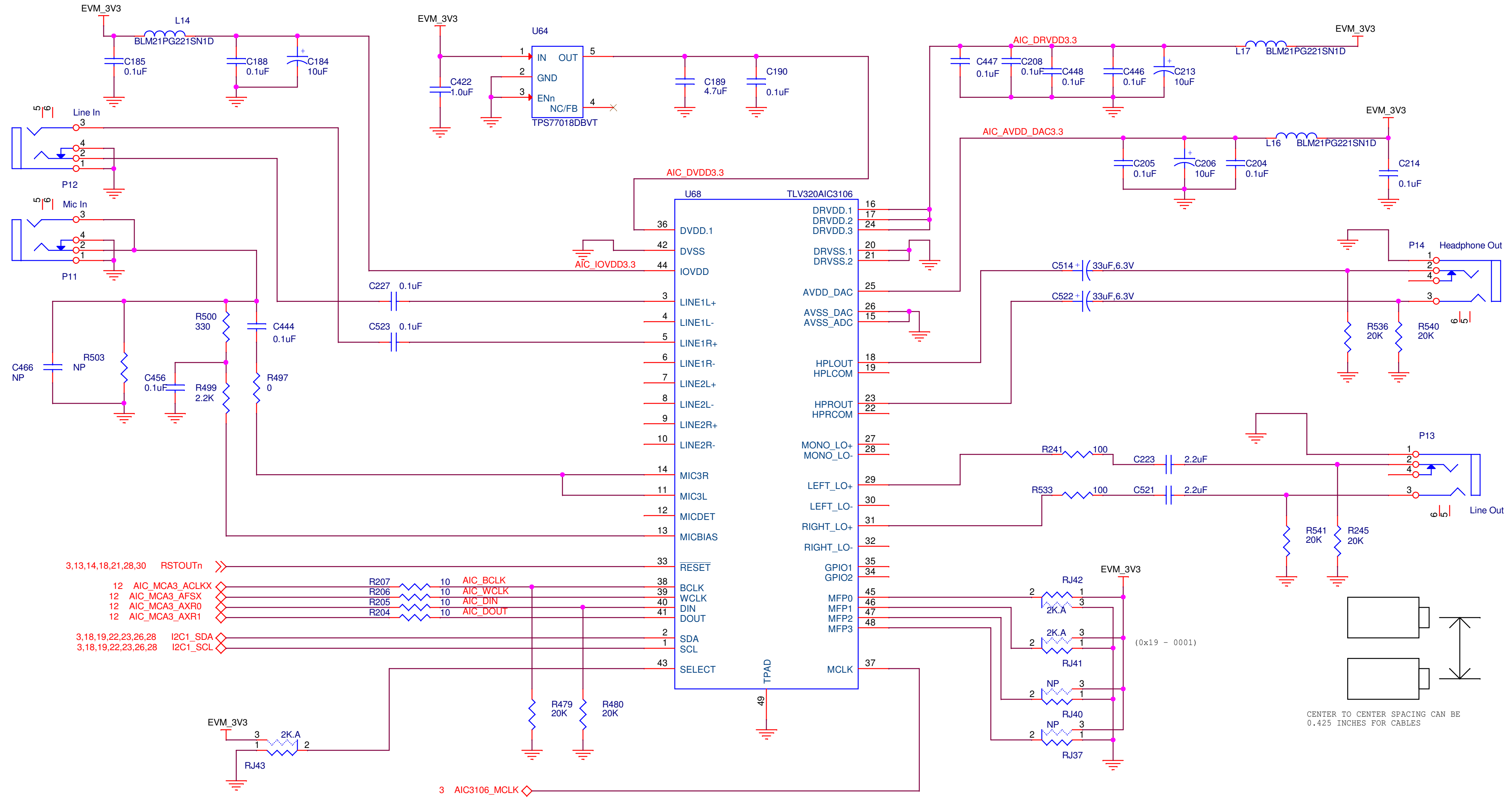
Note: Buffers used for voltage translation and signal isolation.



TRSTn == MIPI TRSTPD PULL DOWN VERSION
TRSTn == MIPI nTRST MIPI PULLUP VERSION
FOR CJTAG SET THE RJ TO PINS 3-2.

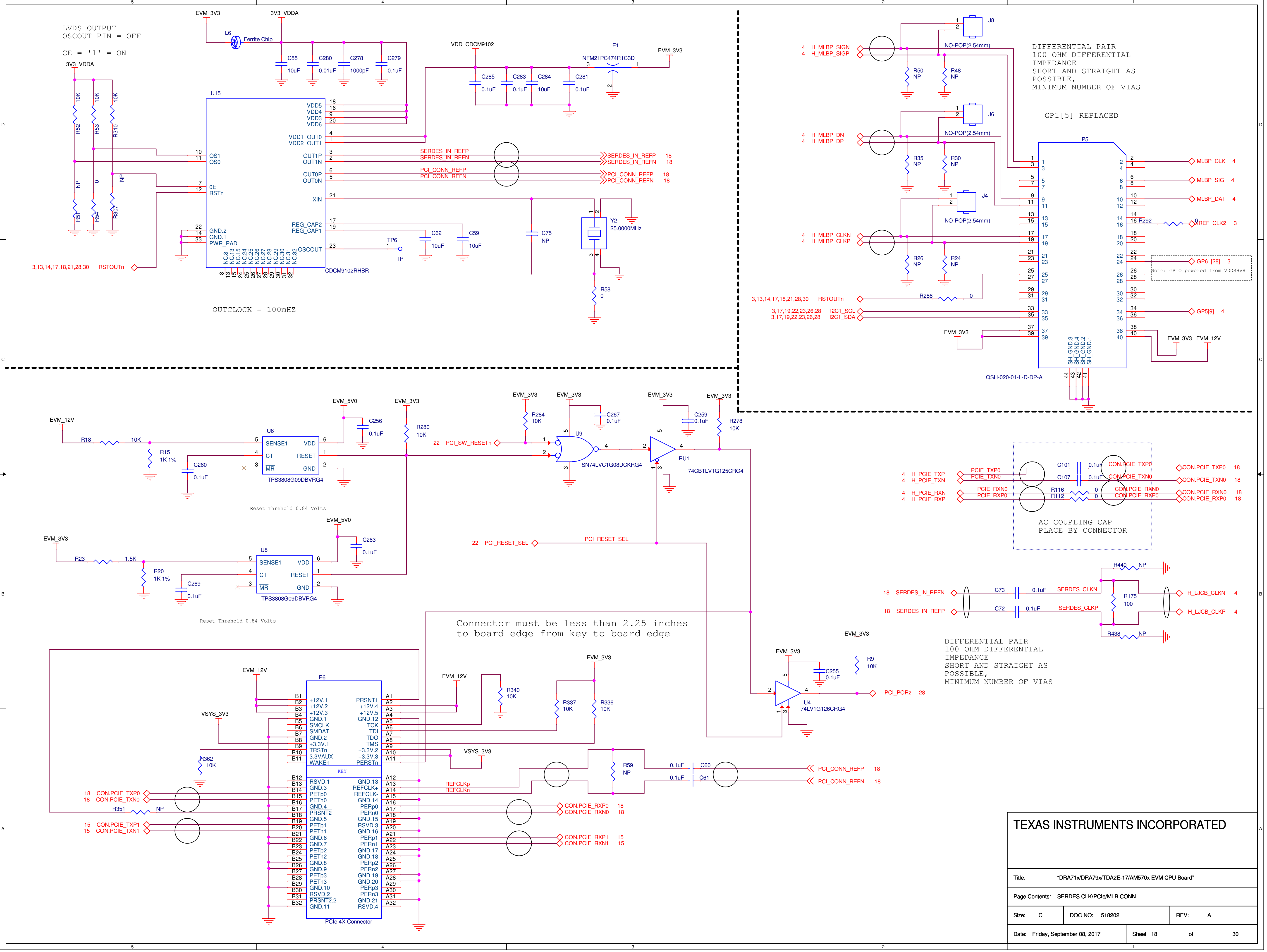
TEXAS INSTRUMENTS INCORPORATED

Title:	"DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents:	USB-UART/JTAG		
Size: C	DOC NO: 518202	REV: A	
Date: Friday, September 08, 2017	Sheet 16	of	30



TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"			
Page Contents: AIC3106			
Size: C	DOC NO: 518202	REV: A	
Date: Friday, September 08, 2017	Sheet 17	of	30



LVDS OUTPUT
OSCOUT PIN = OFF

CE = '1' = ON

OUTCLOCK = 100mHZ

DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

GP1[5] REPLACED

Reset Threhold 0.84 Volts

Reset Threhold 0.84 Volts

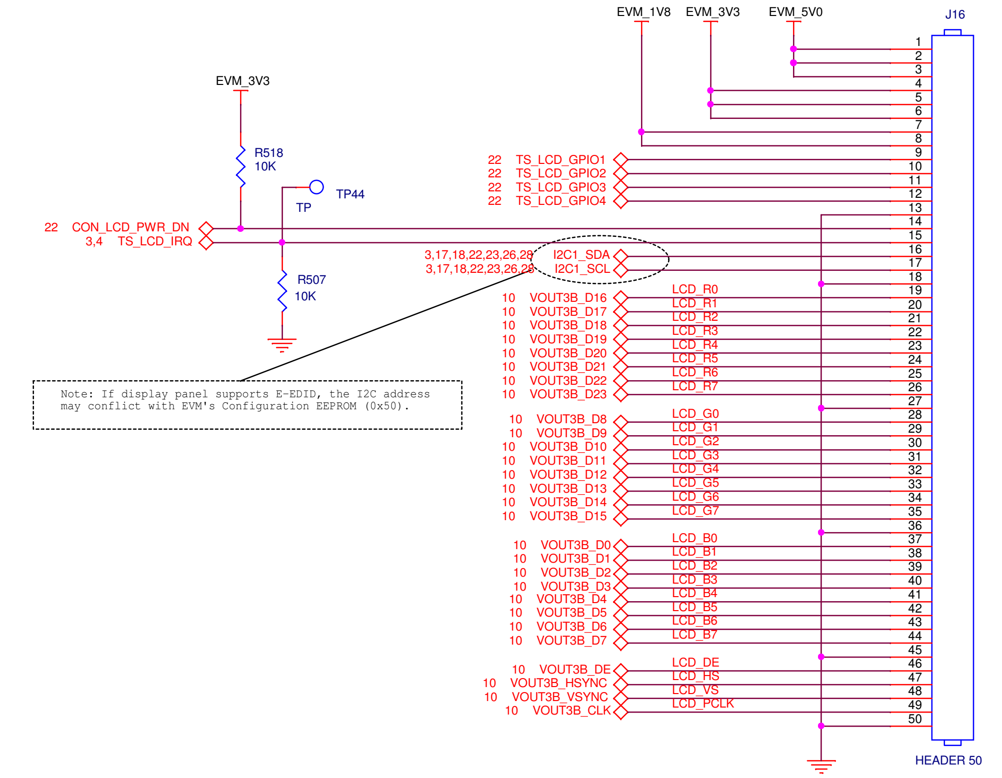
AC COUPLING CAP
PLACE BY CONNECTOR

Connector must be less than 2.25 inches
to board edge from key to board edge

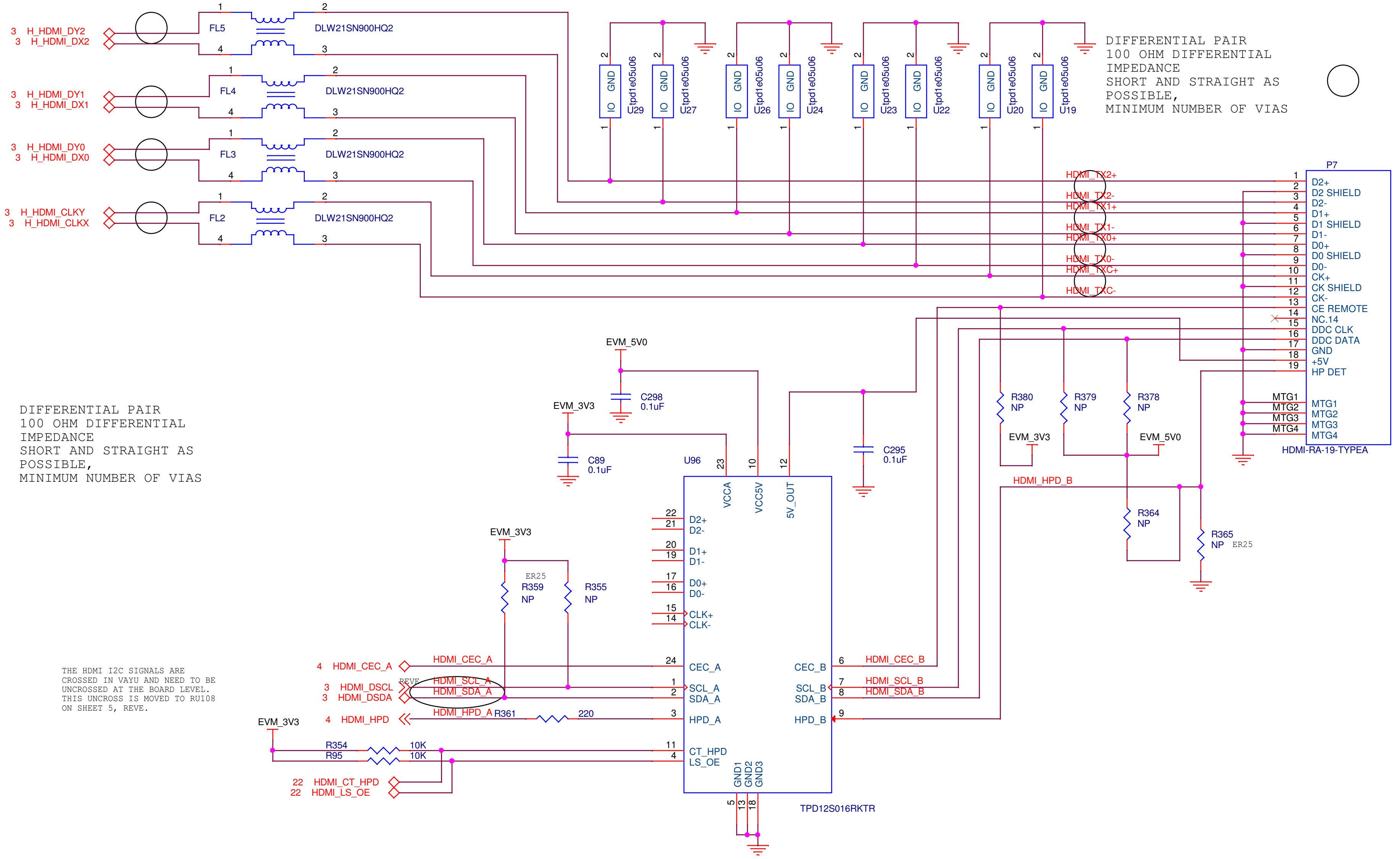
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

TEXAS INSTRUMENTS INCORPORATED

Title:	"DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"
Page Contents:	SERDES CLK/PCIe/MLB CONN
Size: C	DOC NO: 518202
REV:	A
Date:	Friday, September 08, 2017
Sheet	18 of 30



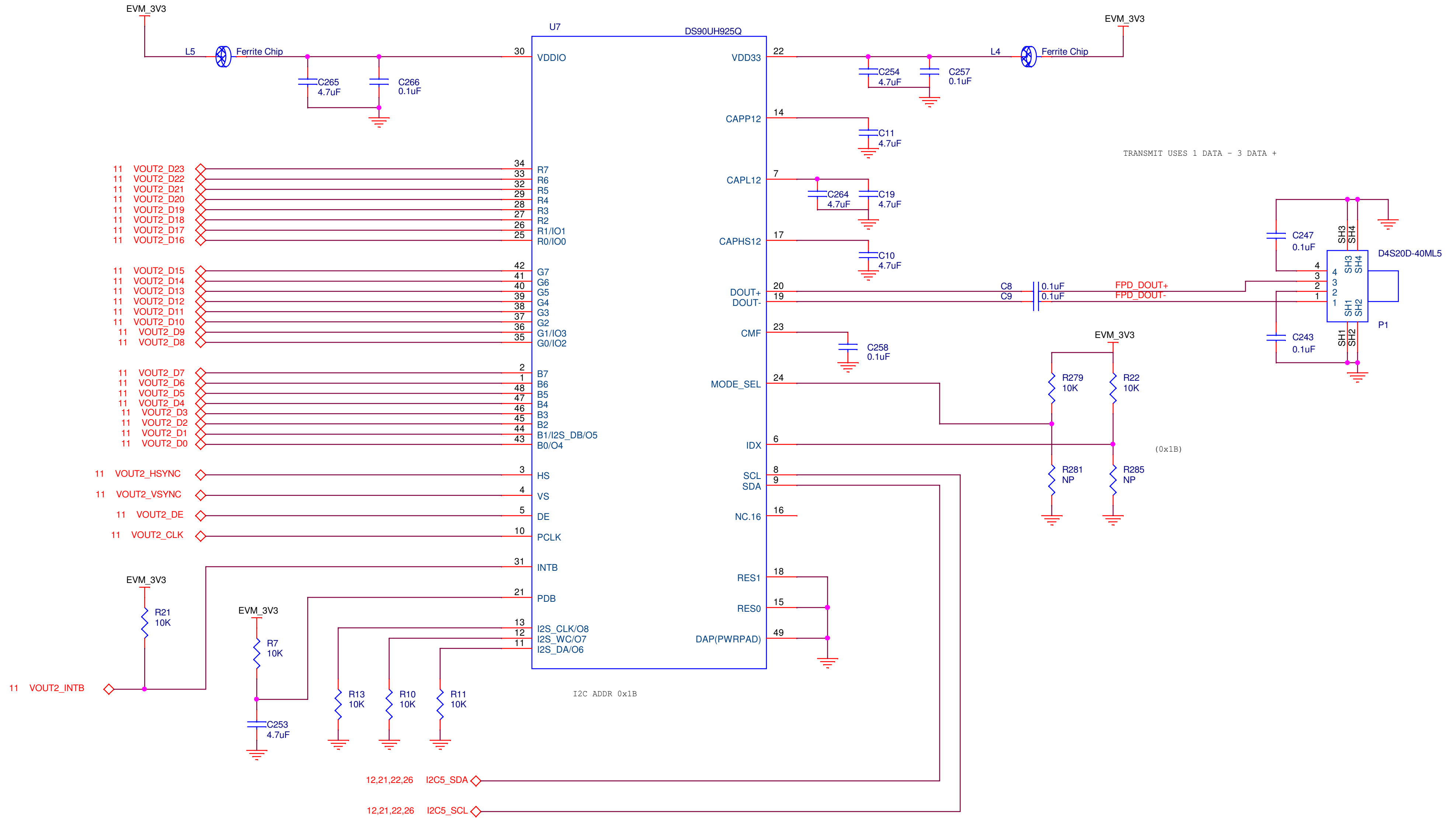
Note: If display panel supports E-EDID, the I2C address may conflict with EVM's Configuration EEPROM (0x50).



THE HDMI I2C SIGNALS ARE CROSSED IN VAYU AND NEED TO BE UNCROSSED AT THE BOARD LEVEL. THIS UNCROSS IS MOVED TO RU108 ON SHEET 5, REVE.

TEXAS INSTRUMENTS INCORPORATED

Title:	"DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents:	LCD/HDMI CONNECTORS		
Size: C	DOC NO: 518202	REV: A	
Date: Friday, September 08, 2017	Sheet 19	of	30



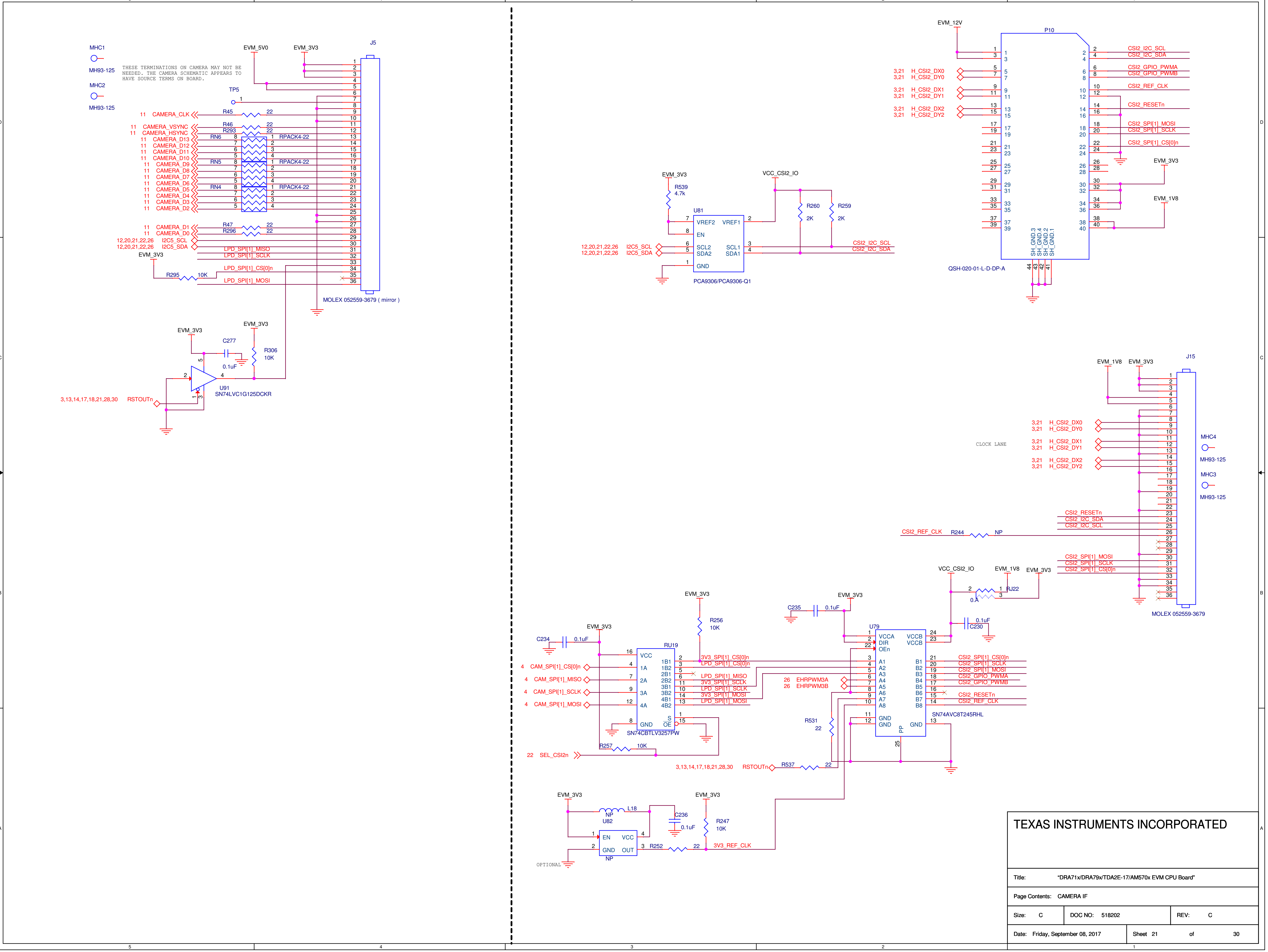
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: FPD LINK

Size: C
DOC NO: 518202
REV: A

Date: Friday, September 08, 2017
Sheet 20 of 30



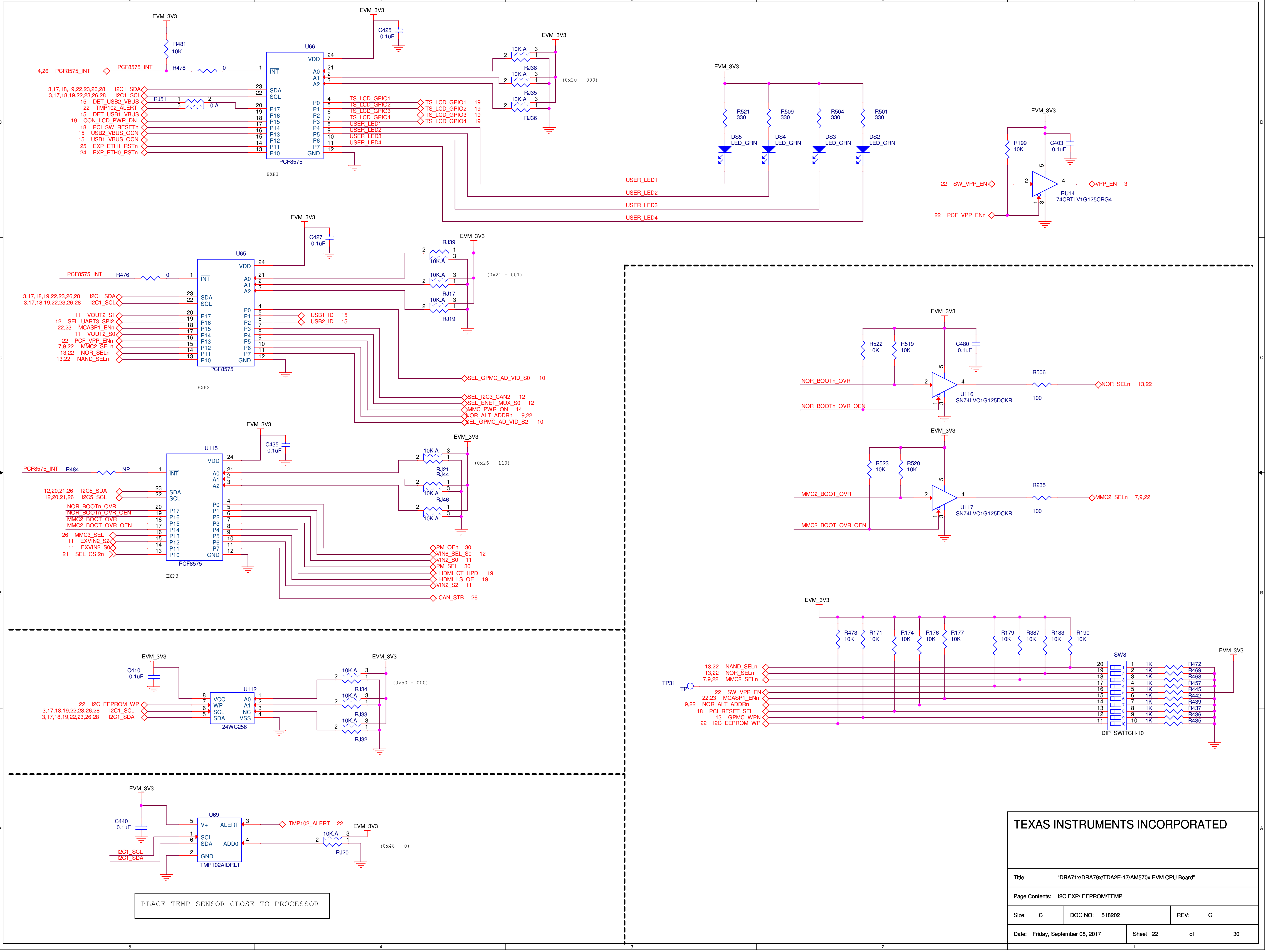
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: CAMERA IF

Size: C DOC NO: 518202 REV: C

Date: Friday, September 08, 2017 Sheet 21 of 30

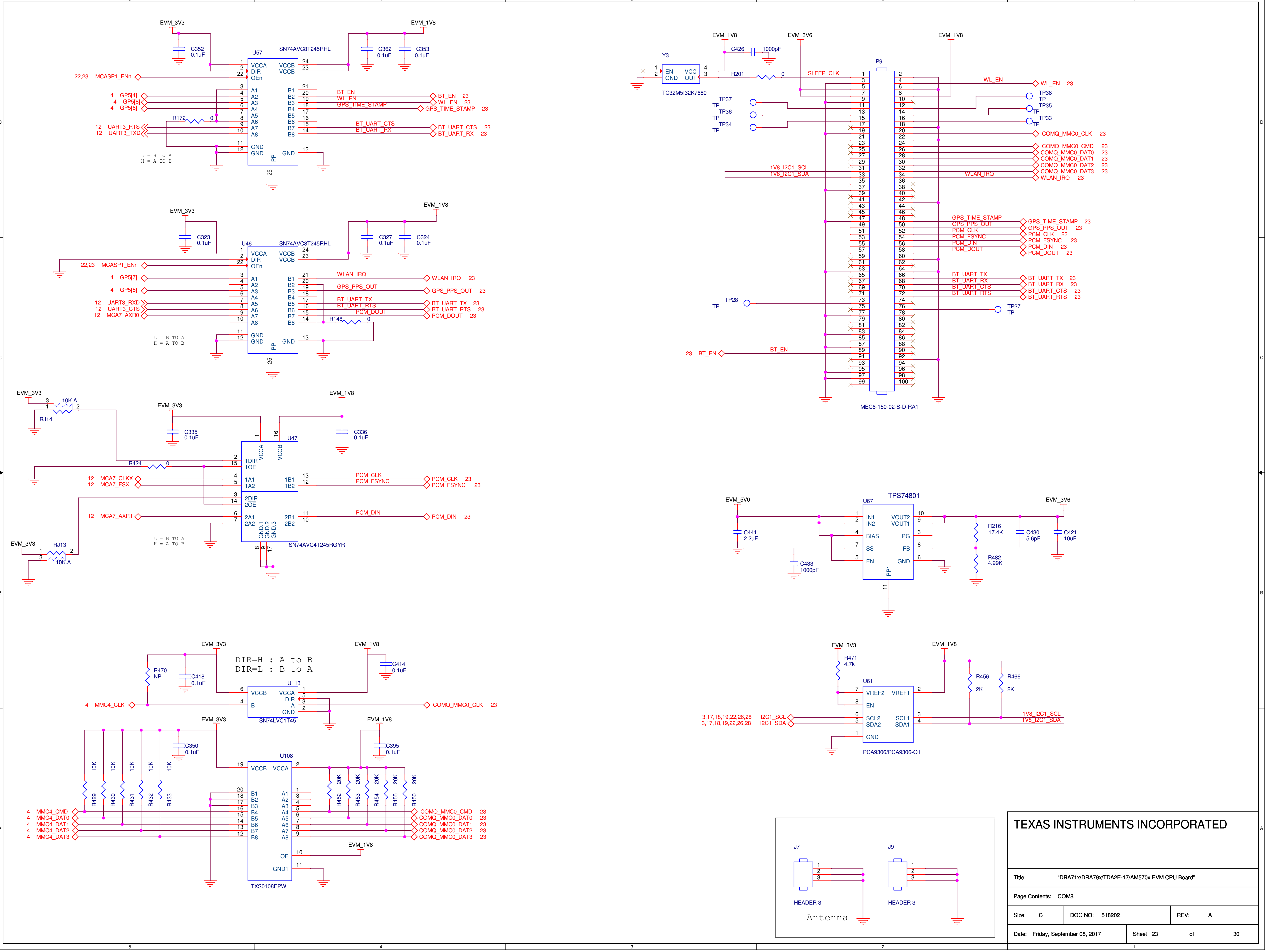


TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: I2C EXP/ EEPROM/TEMP

Size: C	DOC NO: 518202	REV: C
Date: Friday, September 08, 2017	Sheet 22 of 30	



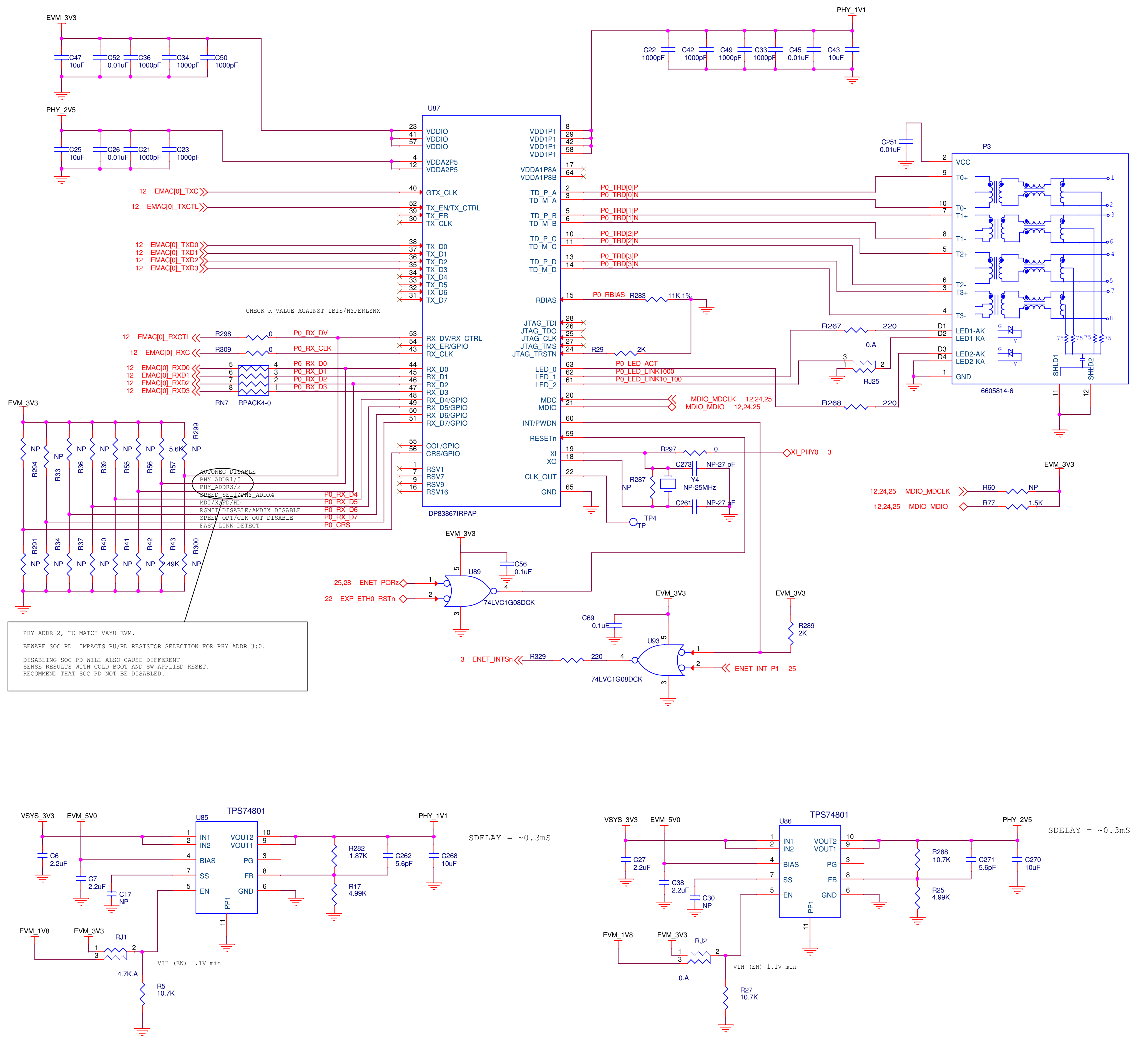
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: COM8

Size: C DOC NO: 518202 REV: A

Date: Friday, September 08, 2017 Sheet 23 of 30



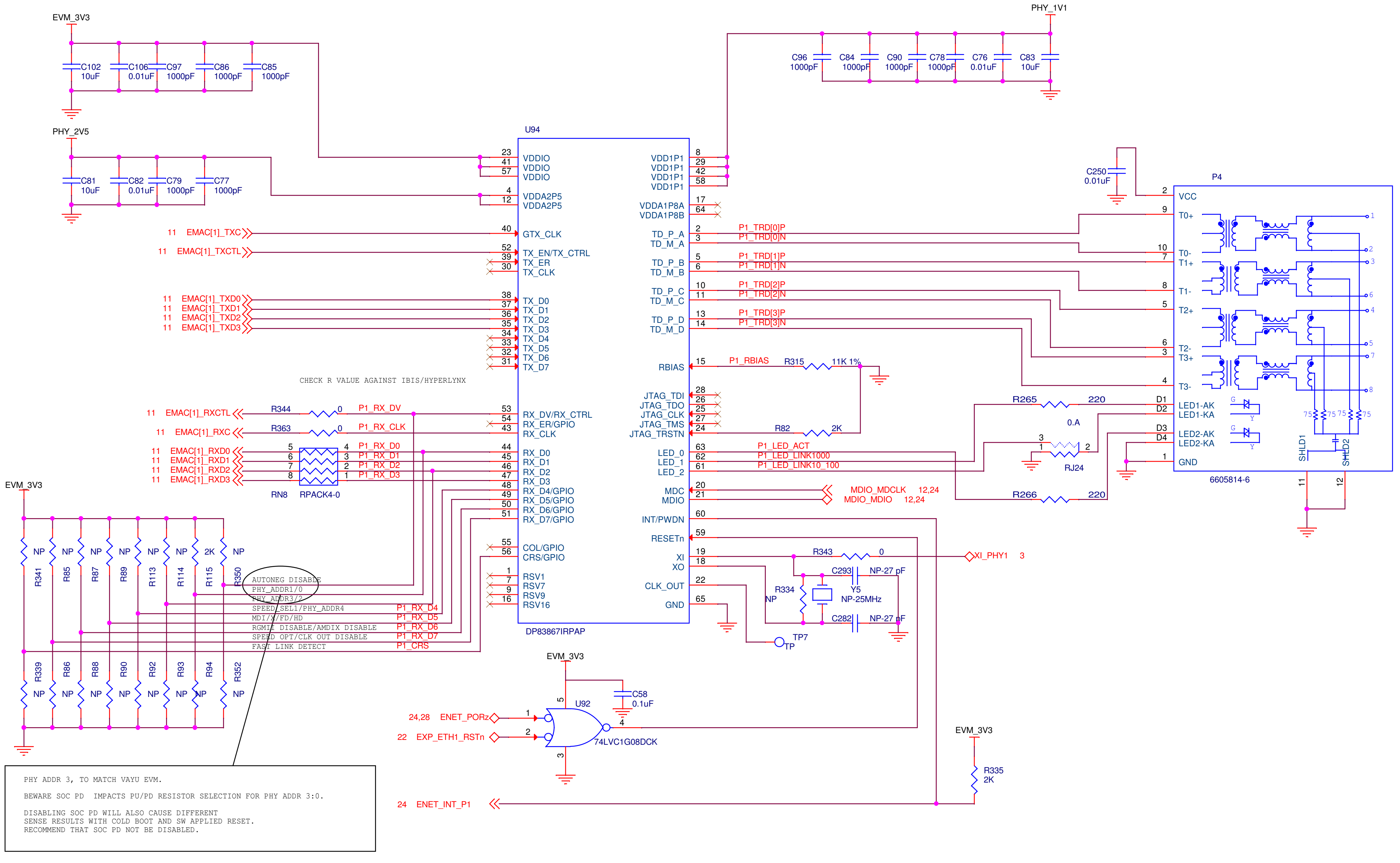
PHY ADDR 2, TO MATCH VAYU EVM.

BEWARE SOC PD IMPACTS PU/PD RESISTOR SELECTION FOR PHY ADDR 3:0.

DISABLING SOC PD WILL ALSO CAUSE DIFFERENT
SENSE RESULTS WITH COLD BOOT AND SW APPLIED RESET.
RECOMMEND THAT SOC PD NOT BE DISABLED.

TEXAS INSTRUMENTS INCORPORATED

Title:	"DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents:	ETHERNET PORT0		
Size: C	DOC NO: 518202	REV: A1	
Date: Friday, September 08, 2017	Sheet 24	of	30



CHECK R VALUE AGAINST IBIS/HYPERLYNX

PHY ADDR 3, TO MATCH VAYU EVM.

BEWARE SOC PD IMPACTS PU/PD RESISTOR SELECTION FOR PHY ADDR 3:0.

DISABLING SOC PD WILL ALSO CAUSE DIFFERENT
SENSE RESULTS WITH COLD BOOT AND SW APPLIED RESET.
RECOMMEND THAT SOC PD NOT BE DISABLED.

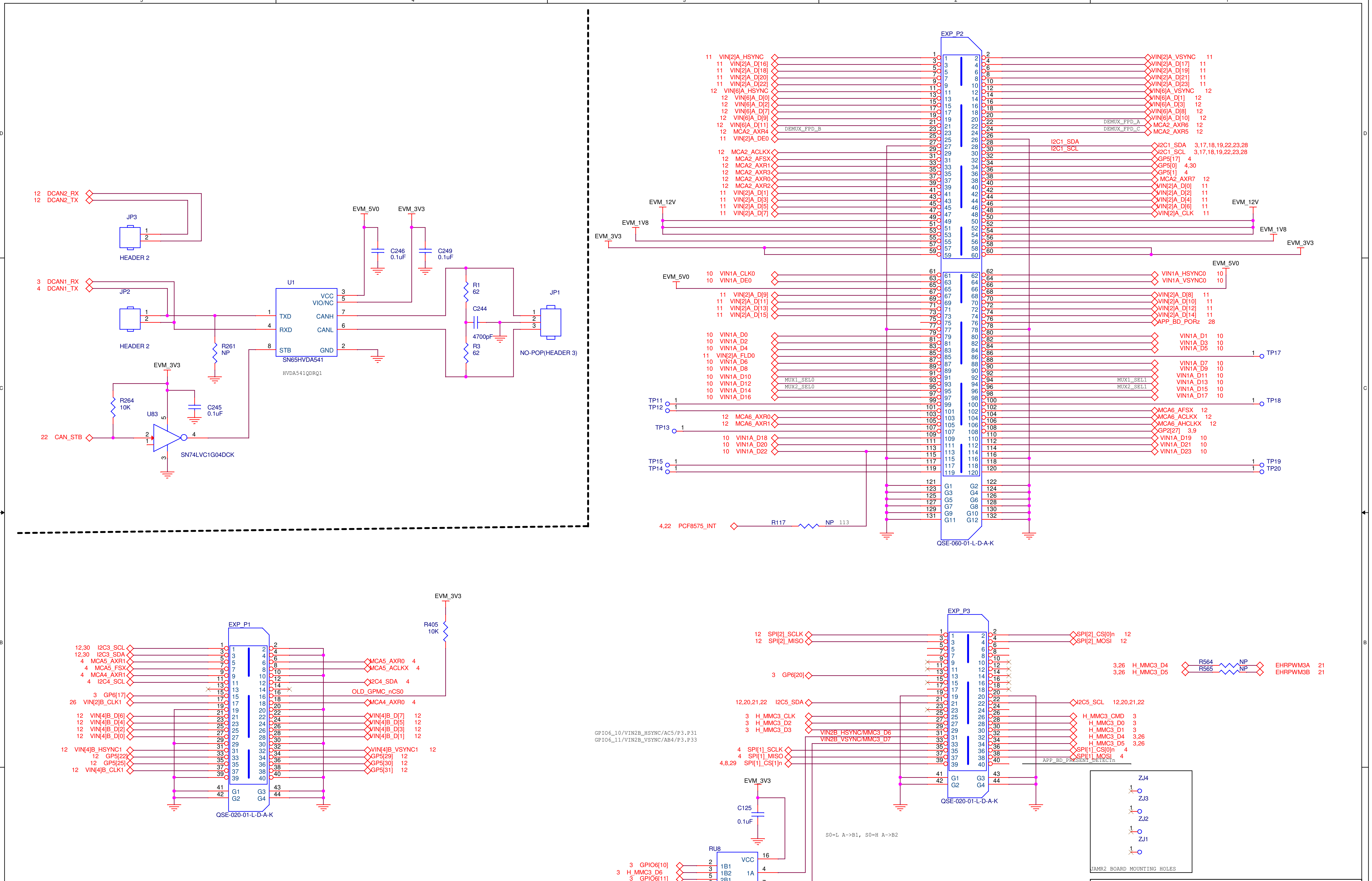
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: ETHERNET PORT1

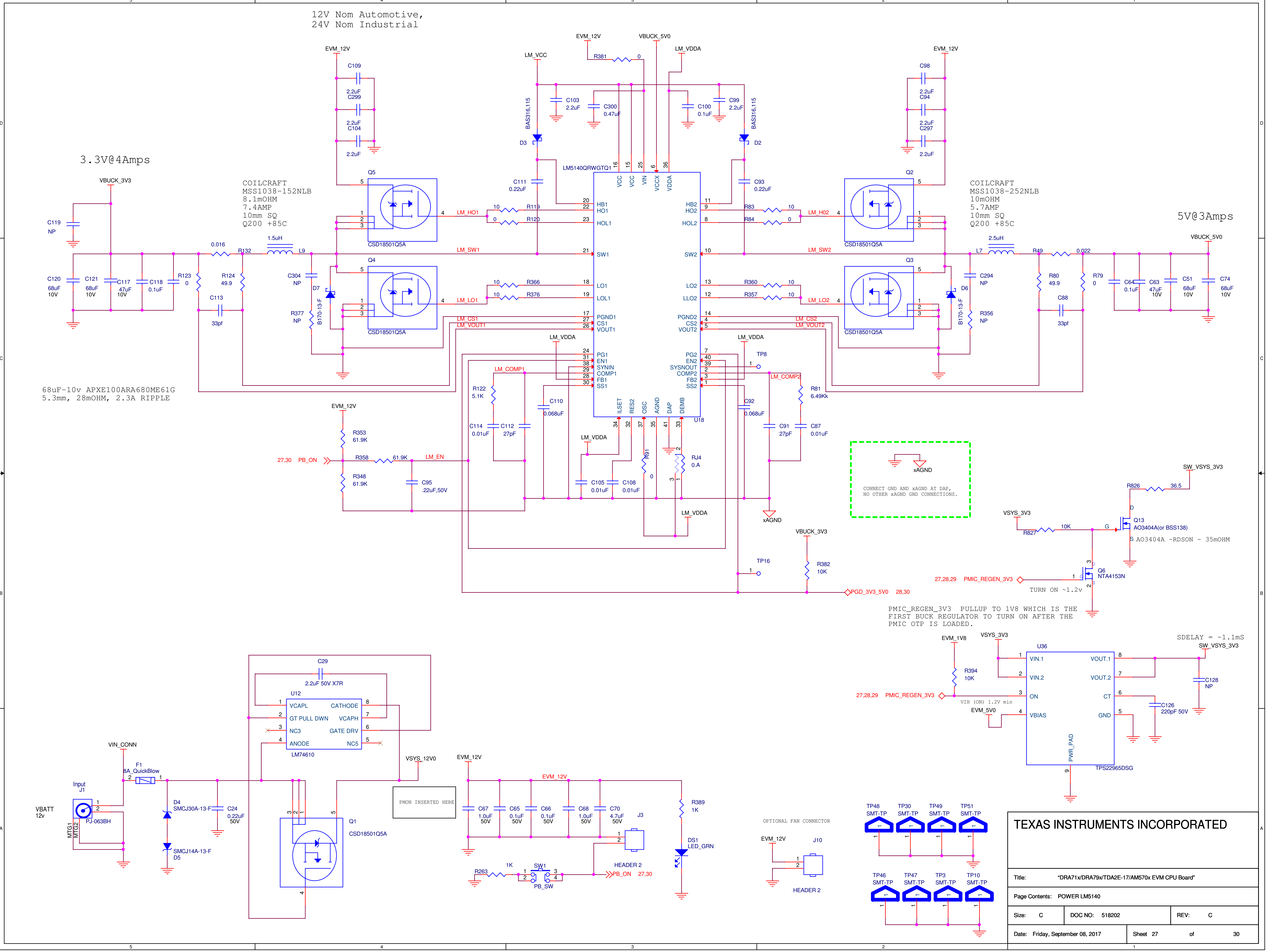
Size: C | DOC NO: 518202 | REV: A

Date: Friday, September 08, 2017 | Sheet 25 of 30



TEXAS INSTRUMENTS INCORPORATED

Title: “DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board”			
Page Contents: CAN/EXP CONNECTORS			
Size: C	DOC NO: 518202		REV: C
Date: Friday, September 08, 2017	Sheet 26	of	30



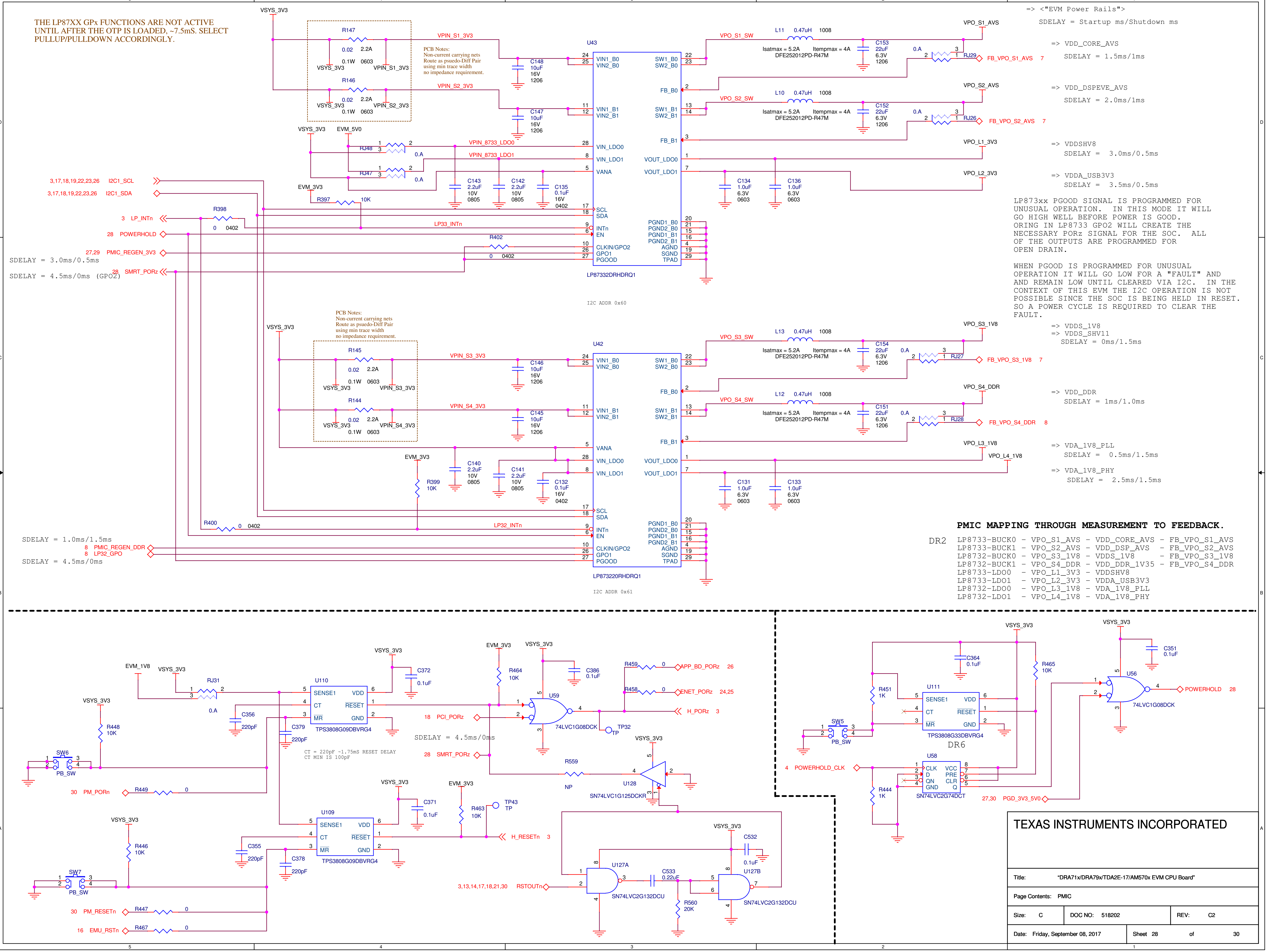
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: POWER LM5140

Size: C DOC NO: 518202 REV: C

Date: Friday, September 08, 2017 Sheet 27 of 30



=> <"EVM Power Rails">

SDELAY = Startup ms/Shutdown ms

=> VDD_CORE_AVS
SDELAY = 1.5ms/1ms

=> VDD_DSPEVE_AVS
SDELAY = 2.0ms/1ms

=> VDDSHV8
SDELAY = 3.0ms/0.5ms

=> VDDA_USB3V3
SDELAY = 3.5ms/0.5ms

LP873xx PGOOD SIGNAL IS PROGRAMMED FOR UNUSUAL OPERATION. IN THIS MODE IT WILL GO HIGH WELL BEFORE POWER IS GOOD. ORING IN LP8733 GPO2 WILL CREATE THE NECESSARY PORz SIGNAL FOR THE SOC. ALL OF THE OUTPUTS ARE PROGRAMMED FOR OPEN DRAIN.

WHEN PGOOD IS PROGRAMMED FOR UNUSUAL OPERATION IT WILL GO LOW FOR A "FAULT" AND AND REMAIN LOW UNTIL CLEARED VIA I2C. IN THE CONTEXT OF THIS EVM THE I2C OPERATION IS NOT POSSIBLE SINCE THE SOC IS BEING HELD IN RESET. SO A POWER CYCLE IS REQUIRED TO CLEAR THE FAULT.

=> VDDS_1V8
=> VDDS_SHV11
SDELAY = 0ms/1.5ms

=> VDD_DDR
SDELAY = 1ms/1.0ms

=> VDA_1V8_PLL
SDELAY = 0.5ms/1.5ms

=> VDA_1V8_PHY
SDELAY = 2.5ms/1.5ms

SDELAY = 3.0ms/0.5ms

SDELAY = 4.5ms/0ms (GPO2)

SDELAY = 1.0ms/1.5ms

SDELAY = 4.5ms/0ms

SDELAY = 4.5ms/0ms

PMIC MAPPING THROUGH MEASUREMENT TO FEEDBACK.

```
DR2  LP8733-BUCK0 - VPO_S1_AVS - VDD_CORE_AVS - FB_VPO_S1_AVS
     LP8733-BUCK1 - VPO_S2_AVS - VDD_DSP_AVS  - FB_VPO_S2_AVS
     LP8732-BUCK0 - VPO_S3_1V8 - VDDS_1V8     - FB_VPO_S3_1V8
     LP8732-BUCK1 - VPO_S4_DDR - VDD_DDR_1V35 - FB_VPO_S4_DDR
     LP8733-LDO0  - VPO_L1_3V3 - VDDSHV8
     LP8733-LDO1  - VPO_L2_3V3 - VDDA_USB3V3
     LP8732-LDO0  - VPO_L3_1V8 - VDA_1V8_PLL
     LP8732-LDO1  - VPO_L4_1V8 - VDA_1V8_PHY
```

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Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: PMIC

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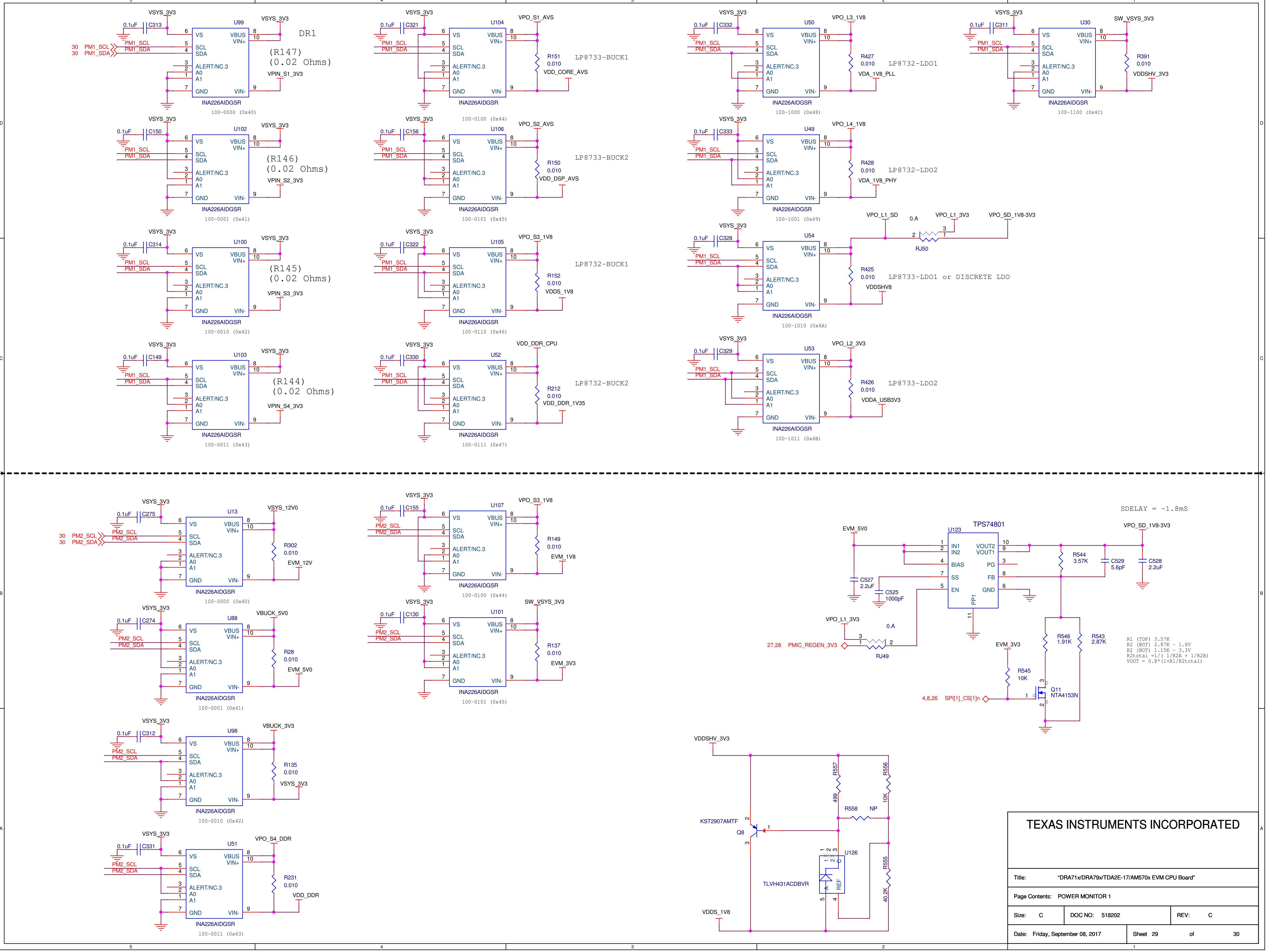

TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

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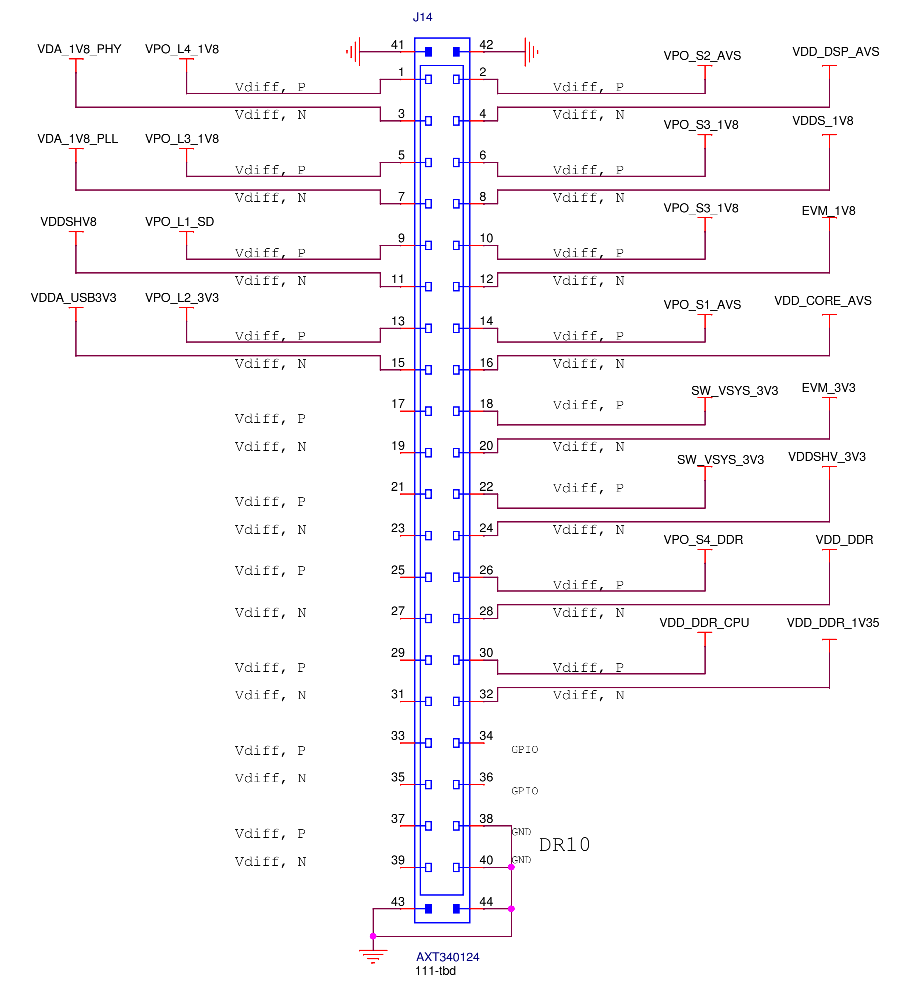
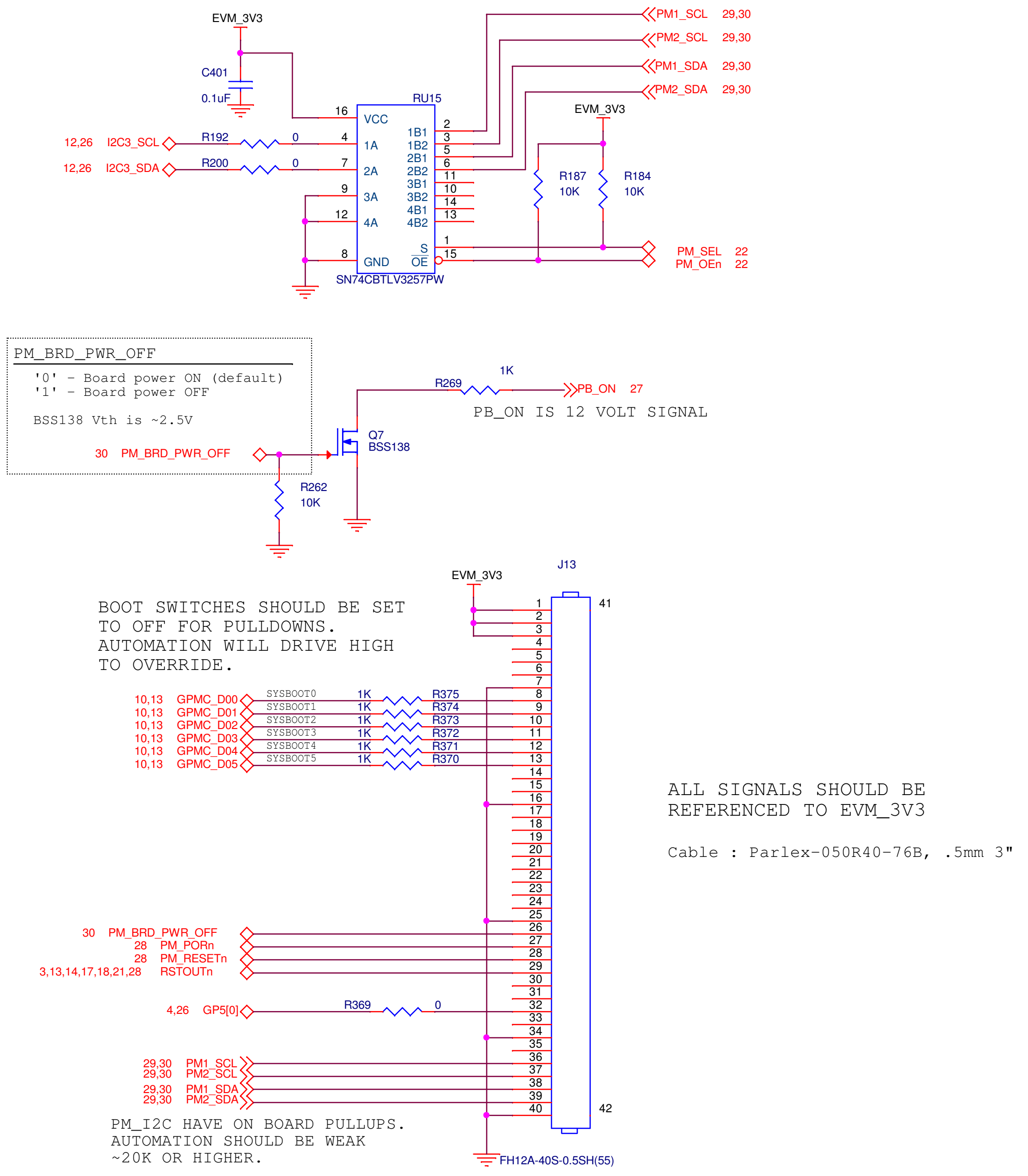
DARA Bd Interface Connector

DARA Bd can be interfaced to conduct more in-depth power measurements.

All Vdiff signal pairs (P & N) shown should be routed as pseudo-Diff Pair segments using min trace widths since these are low voltage sensing nets, not power delivery nets.



AUTOMATION INTERFACE



PM_BRD_PWR_OFF

'0' - Board power ON (default)
'1' - Board power OFF

BSS138 Vth is ~2.5V

PB_ON IS 12 VOLT SIGNAL

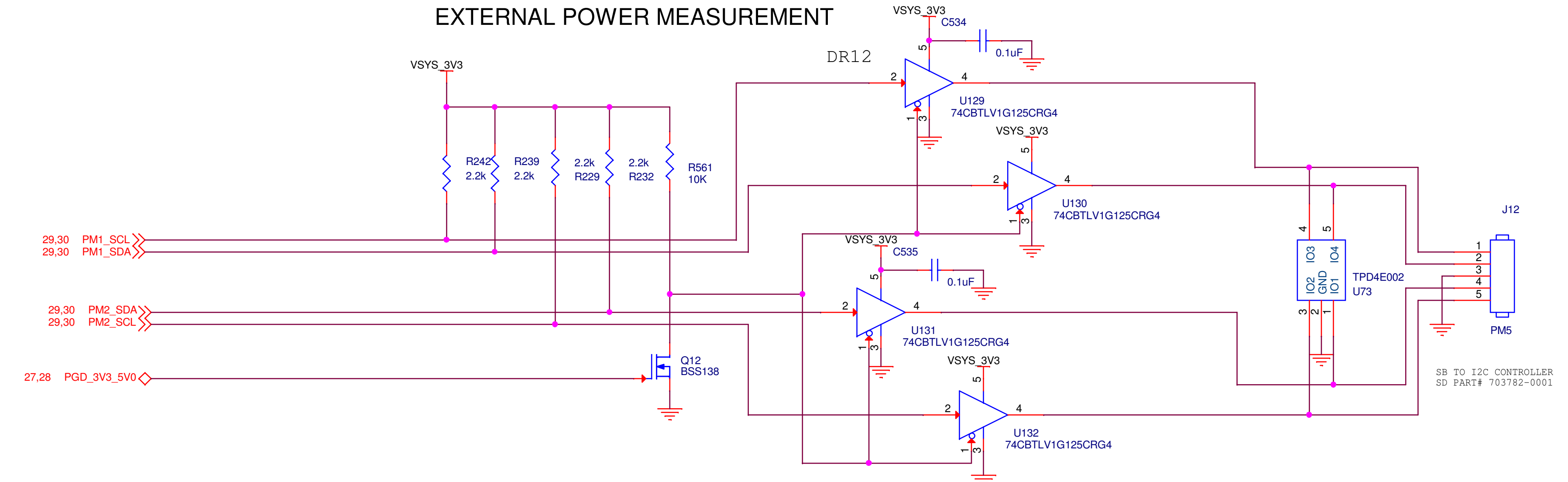
BOOT SWITCHES SHOULD BE SET TO OFF FOR PULLDOWNS. AUTOMATION WILL DRIVE HIGH TO OVERRIDE.

PM_I2C HAVE ON BOARD PULLUPS. AUTOMATION SHOULD BE WEAK ~20K OR HIGHER.

ALL SIGNALS SHOULD BE REFERENCED TO EVM_3V3

Cable : Parlex-050R40-76B, .5mm 3"

EXTERNAL POWER MEASUREMENT



SB TO I2C CONTROLLER
SD PART# 703782-0001

TEXAS INSTRUMENTS INCORPORATED

Title: “DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board”
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