Radiation Report

Single-Event Effects (SEE) Radiation Report of the F28377D-SEP Dual-Core Real-Time Microcontroller

ABSTRACT

The purpose of this study is to characterize the single-event effects (SEE) performance due to heavy-ion irradiation of the F28377D-SEP. Heavy-ions with LET_{EFF} of 45MeV·cm^2 /mg were used to irradiate three pre-production devices. Flux of ≅ 10^5ions×cm^2/s and fluence of ≅10^7 ions/cm^{2}for SEL and Flux of ≅ 10^4ions×cm^2/s fluence of ≅10^6 ions/cm^2 for SET per run were used for the characterization. The results demonstrated that the F28377D-SEP is SEL-free up to 45MeV·cm^2/mg at T = 125°C in addition to effects of SET at T = 25°C. SET transients performance was monitored during checking for excursions of >|3%| from the nominal output on independent GPIO outputs that were controlled by CPU1 and CPU2 respectively while code is executing during both SEL and SET testing.

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1 Introduction

The F28377D-SEP is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; and sensing and signal processing.

Performance analog and control peripherals are also integrated on the F28377D MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. The new sigma-delta filter module (SDFM) works in conjunction with the sigma-delta modulator to enable isolated current shunt measurements. The Comparator Subsystem (CMPSS) with windowed comparators allows for protection of power stages when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

While this document details the performance of the F28377D-SEP while exposed to heavy ions, there are many features on the device that can be used to mitigate the occurrence of transients due to radiation. Features like ECC and Parity on the memories, watchdog timers to detect deviations in code execution, interrupts to detect overflow events, are just a few of the HW mechanisms on-chip that help the F28377D-SEP robustness in a radiation environment. The *Functional Safety Manual for TMS320F2837xD, TMS320F2837xS, and TMS320F2807x* is an excellent resource to go into more detail on all the available resources on the device to achieve a more robust system.

The device is offered in a 176-pin plastic package. General device information and test conditions are listed in the overview information table. For more detailed technical specifications, user-guides, and application notes please go to device product page.

Table 1-1. Overview Information

DESCRIPTION(1)	DEVICE INFORMATION
TI Part Number	F28377D-SEP
Orderable Part Number	F28377DPTPSEP
VID/SMD Number	V62/25638
Device Function	32-bit Dual-Core Real-Time Microcontroller
Technology	F021 (65nm Flash CMOS)
Exposure Facility	Radiation Effects Facility, Cyclotron Institute, Texas A&M University (25MeV/nucleon)
Heavy Ion Fluence per Run	1.00×10^6 – 1.00×10^7 ions/cm^2
Irradiation Temperature	25°C (for SET testing), and 125°C (for SEL testing)

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2 Single-Event Effects (SEE)

The primary concern for the F28377D-SEP is the robustness against the destructive single-event effects (DSEE): single-event latch-up (SEL).

SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-sub and n-well and n+ and p+ contacts) [1,2]. The parasitic bipolar structure initiated by a single-event creates a high-conductance path (inducing a steady-state current that is typically orders-of-magnitude higher than the normal operating current) between power and ground that persists (is “latched”) until power is removed, the device is reset, or until the device is destroyed by the high-current state. The F28377D-SEP was tested for SEL at the maximum recommended operating conditions of 3.46V (VDDIO) and 1.26V (VDD). The flash memory of the device was programmed with code used to enable all peripherals as well as both CPU cores; and the device was placed into flash boot mode. Two GPIO outputs with a 100kHz square wave, controlled by CPU1 and CPU2 respectively, were monitored to indicate normal CPU behavior. During testing of the 3 devices, the F28377D-SEP did not exhibit any SEL with heavy-ions with LET_{EFF} = 45MeV·cm^2 /mg at flux ≈10^5 ions×cm^2/s , fluence of ≈10^7 ions/cm^2, and a die temperature of 125°C.

The F28377D-SEP was characterized for SET at flux of ≈10^4 ions/cm^2, fluences of ≈10^6 ions/cm^2, and room temperature. The device was characterized at VDDIO/VDD of 3.3V/1.2V. Heavy-ions with LET_{EFF} of 8.5 - 45MeV·cm^2/mg were used to characterize the transient performance. To see the SET results of the F28377D-SEP, please refer to Single-Event Transients (SET).

3 Device and Test Board Information

The F28377D-SEP is packaged in a 176-pin plastic package as shown in Figure 3-1. The F28377D-SEP evaluation module(EVM) was used to evaluate the performance and characteristics of the F28377D-SEP under heavy ion radiation. The F28377D-SEP EVM is shown in Figure 3-2. The schematic is shown in Figure 3-3.

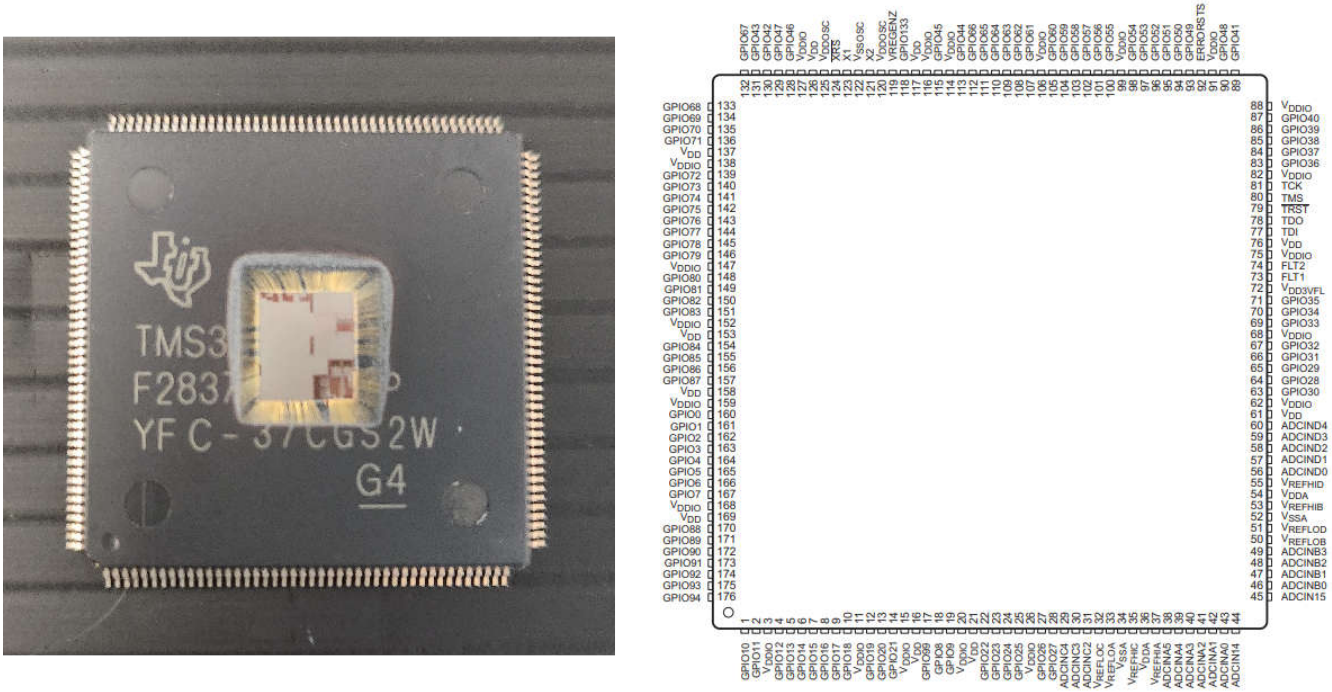
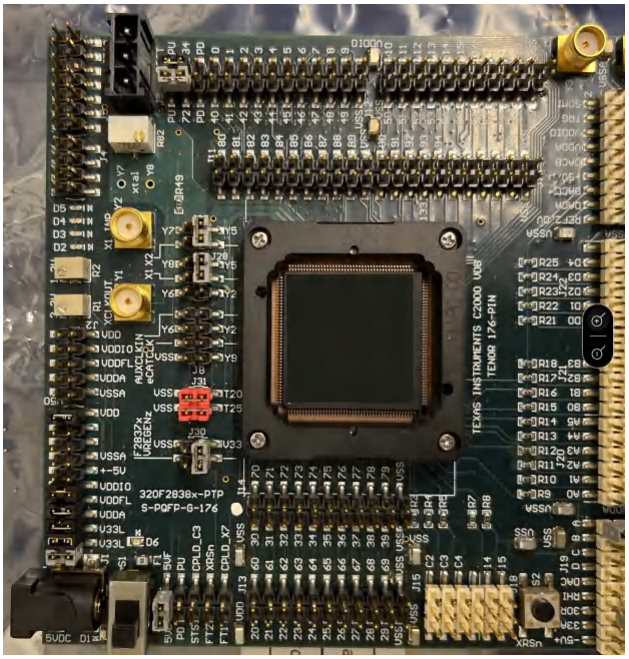


Figure 3-1. Photograph of Delidded F28377D-SEP[Left] and Pinout Diagram [Right]

Note: The package was delidded/decapped to reveal the die face for all heavy-ion testing.

Figure 3-2. F28377D-SEP EVM Top View



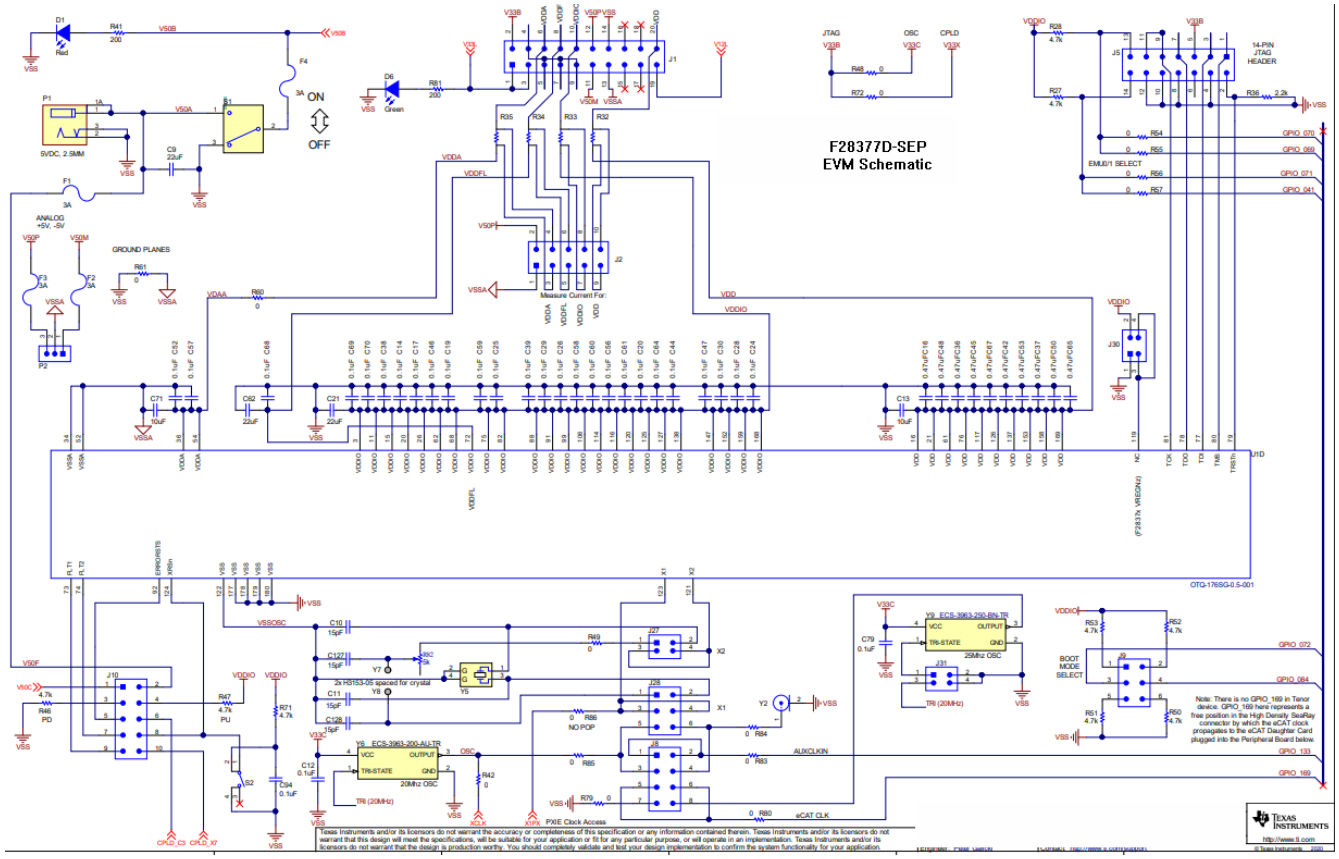


Figure 3-3. F28377D-SEP EVM Schematics

4 Irradiation Facility and Setup

The heavy-ion species used for the SEE studies on this product were provided and delivered by the TAMU Cyclotron Radiation Effects Facility using a superconducting cyclotron and an advanced electron cyclotron resonance (ECR) ion source. At the fluxes used, ion beams had good flux stability and high irradiation uniformity over a 1-in diameter circular cross-sectional area for the in-air station. Uniformity is achieved by magnetic defocusing. The flux of the beam is regulated over a broad range spanning several orders of magnitude. For these studies, ion flux of 10^4-10^5 ions×cm^2/s were used to provide heavy-ion fluences of 10^6-10^7 ions×cm^2/s

For the experiments conducted on this report, there were 2 ions used, ^{109}Ag and ^{40}Ar. ^{109}Ag was used to obtain LET_{EFF} of 45MeV·cm^2/mg. ^{40}Ar was used to obtain LET_{EFF} of 8MeV·cm^2/mg. The total kinetic energys for each of the ions were:

- ^{109}Ag = 1.27 GeV (15MeV/nucleon)
  - Ion uniformity for these experiments was on average 91%
- ^{40}Ar = 536.9MeV (15MeV/nucleon)
  - Ion uniformity for these experiments was on average 94%

Figure 4-1 shows the F28377D EVM used for the data collection at the TAMU facility. Although not visible in this photo, the beam port has a 1-mil Aramica window to allow in-air testing while maintaining the vacuum within the accelerator with only minor ion energy loss. The in-air gap between the device and the ion beam port window was maintained at 40mm for all runs.

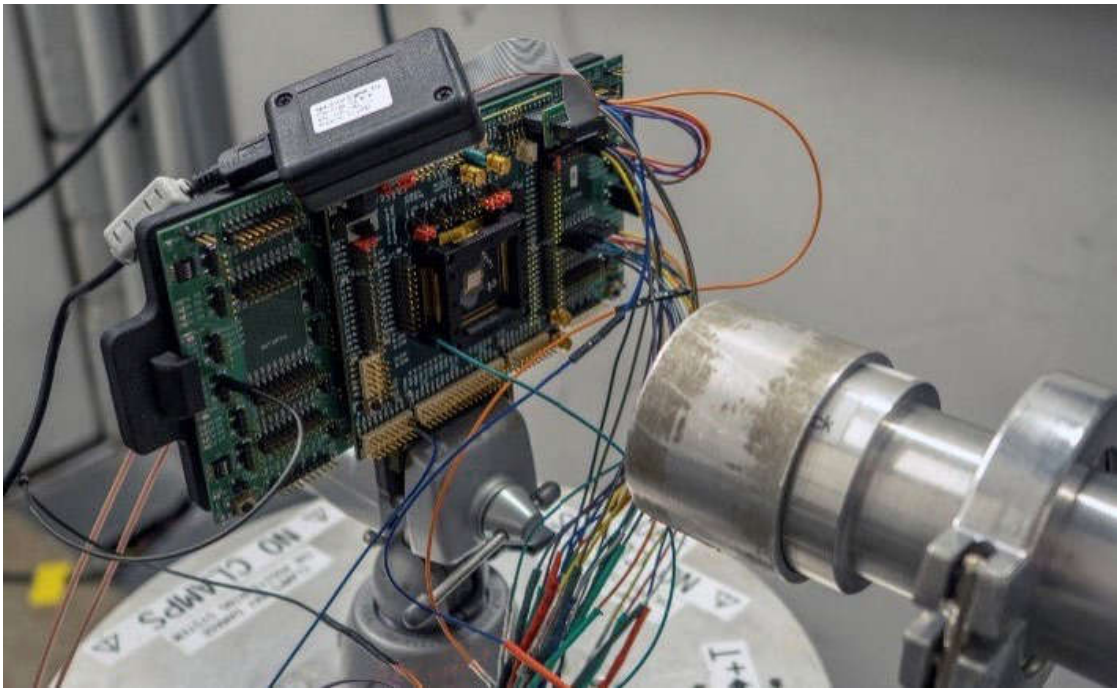


Figure 4-1. Photograph of the F28377D-SEP EVM in Front of the Heavy-Ion Beam Exit Port at the Texas A&M Cyclotron

5 Depth, Range, and LET_{EFF} Calculation

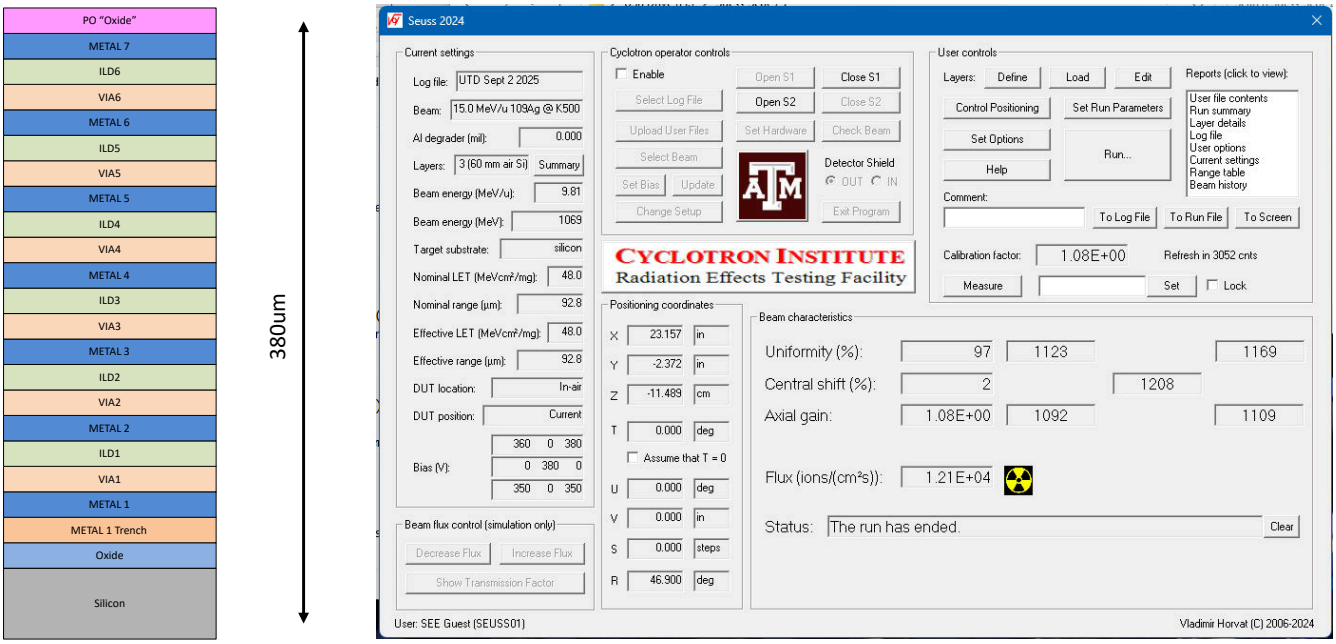


Figure 5-1. Generalized Cross-Section of the F021 Technology BEOL Stack on the F28377D-SEP[Left] and SEUSS 2020 Application Used to Determine Key Ion Parameters [Right]

The F28377D-SEP is fabricated in the TI CMOS 65nm process with a back-end-of-line (BEOL) stack consisting of 7 levels of standard thickness aluminum. The total stack height from the surface of the passivation to the silicon surface is 380µm based on nominal layer thickness as shown in Figure 5-1. Accounting for energy loss through the 1-mil thick Aramica beam port window, the 40-mm air gap, and the BEOL stack over the F28377D-SEP, the effective LET (LET_{EFF}) at the surface of the silicon substrate and the depth was determined with the

SEUSS 2020 Software (provided by the Texas A&M Cyclotron Institute and based on the latest SRIM-2013 [7] models). The results are shown in Ion LET_{EFF}, Depth, and Range in Silicon.

Table 5-1. Ion LET_{EFF}, Depth, and Range in Silicon

ION TYPE	Beam Energy (MeV/nucleon)	ANGLE OF INCIDENCE	DEGRADER STEPS (#)	DEGRADER ANGLE	RANGE IN SILICON (µm)	LET_{EFF} (MeV·cm²/mg)
^{109}Ag	15	0	0	0	111.2	45
^{40}Ar	15	0	0	0	196.8	8

6 Test Setup and Procedures

There were two input supplies used to power the F28377D-SEP which provided V_{DDIO}, V_{DDA} (3.3V nominal) and V_{DD} (1.2V nominal). The V_{DDIO} and V_{DDA} for the device was provided via an Agilent E36311A power module and ranged from 3.46V for the SEL to 3.3V for the SET testing. The V_{DD} for the device was provided by an Agilent E36311A power module and ranged from 1.26V for SEL to 1.2V for the SET testing.

For SEL testing two primary signals were monitored to detect a transient event, 2 GPIOs on the device with a 100kHz "Heartbeat" controlled via FW using the on-chip CPU Timers on each CPU. The XRSn signal was also monitored to correlate if the reset was activated when the Heartbeat signals went out of specification. Both Heartbeats were monitored using a NI PXIe-5172 Scope. Auxiliary signals were monitored with multiple Saleae Logic Pro 16's logic analyzers to record the state of the ERRORSTS pin, as well as GPIOs that were used to show the state of the Reset Cause Register and NMI Reset Cause Register. For SET testing a NI PXIe 4135 SMU was used to supply the F28377D-SEP with power and monitor its current consumption. The Saleae Logic Pro 16's were re-used in the same manner as the SEL testing.

The following modules on the F28377D-SEP device were active during the SEL testing

- CPU1
  - Executing from Flash, exercising below peripherals
  - PWM: ePWM1-ePWM12 running at 400kHz output on GPIO
  - eCAP1-6 enabled
  - XCLKOUT on GPIO
  - ADC: All 4 ADC running continuous conversions
  - DAC: All 3 DACs outputting a voltage up/down at 150kHz
  - CMPSS: All active with internal ramp generator running
  - McBSP clocked at 1MHz and active
  - I2C running with 100kHz output clock
  - USB active
  - DCAN active
  - SCI running loopback at 115.2kbps
  - SPI running at 4Mbps
  - CLA in use, executing tasks
  - DMA transferring data
- CPU2
  - Executing from Flash, running various FPU/TMU/VCU instructions
  - CLA in use, executing tasks
  - DMA transferring data

All equipment except the Saleae Logic Pro 16 and NI PXIe 4135 were controlled and monitored using a custom-developed LabVIEW™ program (PXI-RadTest) running on a HP-Z4 desktop computer. The computer communicates with the PXI chassis via an MXI controller and NI PXIe-8381 remote control module. The Logic Analyzers and SMU were controlled via laptop PCs

Equipment Settings and Parameters Used During the SEE Testing of the *F28377D-SEP* shows the connections, limits, and compliance values used during the testing. Figure 6-1 shows a block diagram of the setup used for SEE testing of the F28377D-SEP.

Table 6-1. Equipment Settings and Parameters Used During the SEE Testing of the *F28377D-SEP*

PIN NAME	EQUIPMENT USED	CAPABILITY	COMPLIANCE	RANGE OF VALUES USED
V_{DDIO}/V_{DDA}	Agilent E36311A	6V, 5A	5-A	3.3V-3.46V
V_{DD}	Agilent E36311A	6V, 5A	5-A	1.2V-1.26V
GPIO62	PXIe-5172 (1)	100MS/s	3%	100 MS/s
GPIO78	PXIe-5172 (1)	100MS/s	3%	100 MS/s
XRSn	PXIe-5172 (2)	100MS/s	—	100 MS/s

All boards used for SEE testing were fully checked for functionality. Dry runs were also performed to verify that the test system was stable under all bias and load conditions prior to being taken to the TAMU facility. During the heavy-ion testing, the LabVIEW control program powered up the F28377D-SEP device and set the external sourcing and monitoring functions of the external equipment. After functionality and stability was confirmed, the beam shutter was opened to expose the device to the heavy-ion beam. The shutter remained open until the target fluence was achieved (determined by external detectors and counters). During irradiation, the NI scope cards continuously monitored the signals. When the device heartbeat went undetected from the device, those events were logged as transient upsets. In all cases recovery from those transients occurred, typically via automatic device reset due to the internal watchdog or NMI functions on the device. No sudden increases in current were observed (outside of normal fluctuations) on any of the test runs and indicated that no SEL events occurred during any of the tests.

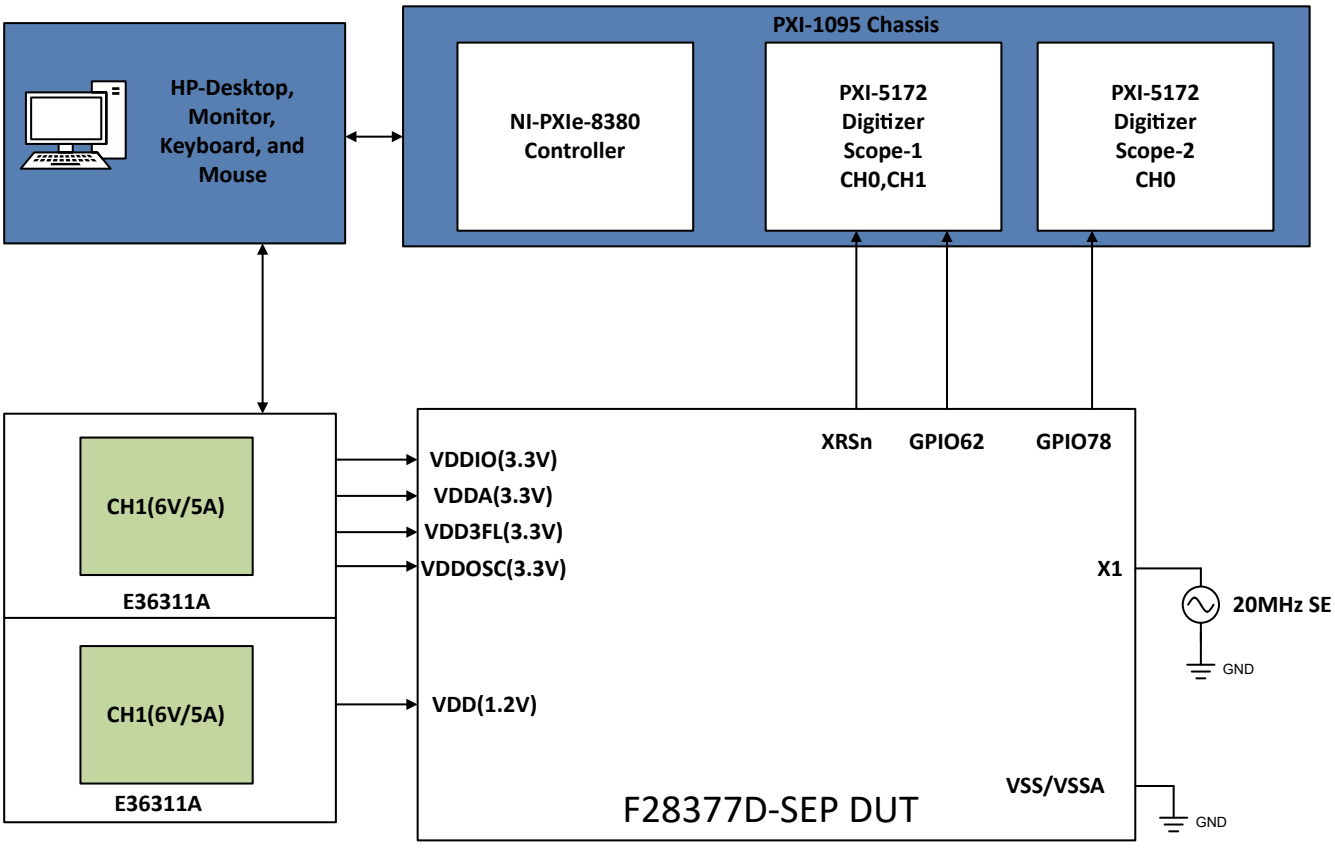


Figure 6-1. Block Diagram of the SEE Test Setup for the F28377D-SEP

7 Destructive Single-Event Effects (DSEE)

7.1 Single-Event Latch-up (SEL) Results

During the SEL tesing the device was heated to 125°C by using a Closed-Loop PID controlled heat gun (MISTRAL 6 System (120V, 2400W)). The temperature of the die was verified using thermal camera prior to exposure to heavy ions.

The species used for the SEL testing was Silver ^{109}Ag at 15MeV/nucleon). For the ^{109}Ag ion an angle of incidence of 0° was used to achieve an LET_{EFF} = 45MeV·cm^2/mg (for more details refer to Ion LET_{EFF}, Depth, and Range in Silicon). The kinetic energy in the vacuum for this ions is 1.634GeV. Flux of approximately ≅10^{5}ions×cm^2/s and a fluence of approximately ≅10e^{7}ions per run was used. Run duration to achieve this fluence was approximately 2 minutes. The 3 F28377D-SEP devices were powered up and exposed to the heavy-ions using the maximum recommended input voltage of 3.63V/1.26V. Each device was ran twice to maintain a total fluence during full operation of the device equal to or greater than 10e^7 ions. No SEL events were observed during all six runs, indicating that the F28377D-SEP is SEL-free up to 45MeV·cm^2/mg.Table 7-1 shows the SEL test conditions and results. Current versus Time for Run #11 of the F28377D-SEP at T = 125°C shows a plot of the current vs time for run #11. The periodic drops in supply current are a result of transients activating a reset condition from the on-chip monitors. The increase in current in the VDDIO domain is likely due to increased activity on the GPIO bus caused by an upset that resolved itself. Reset was self released, and the devices proceeded to reboot and correct resume execution from flash memory.

Table 7-1. Summary of F28377D-SEP

Run #	Unit #	Facility	Ion	LET_{EFF} (MeV·cm^2/mg)	Flux (ions·cm^2/mg)	Fluence (# ions)	V_{IN}	I_{OUT} (A)	SEL (# Events)
6	2	TAMU	^{109}Ag	44.8	8.12x 10^4	1 x 10^7	3.63V/1.26V	85mA/ 300mA	0
7	2	TAMU	^{109}Ag	44.8	9.89 x 10^4	1 x 10^7	3.63V/1.26V	85mA/ 300mA	0
9	3	TAMU	^{109}Ag	44.8	1.01 x 10^5	9.99 x 10^6	3.63V/1.26V	85mA/ 300mA	0
11	3	TAMU	^{109}Ag	44.8	1.03 x 10^5	9.95 x 10^6	3.63V/1.26V	85mA/ 300mA	0
12	4	TAMU	^{109}Ag	44.8	1.05 x 10^5	1.05 x 10^7	3.63V/1.26V	85mA/ 300mA	0
13	4	TAMU	^{109}Ag	44.8	1.06 x 10^5	9.98 x 10^6	3.63V/1.26V	85mA/ 300mA	0

Using the MFTF method described in *Single-Event Effects (SEE) Confidence Interval Calculations* application report and combining (or summing) the fluences of the six runs at 125°C (*10* × 10^7), the upper-bound cross-section (using a 95% confidence level) is calculated as:

$\sigma_{SEL} \leq 6.33 \times 10^{-8}$ cm^2/device for LET_{EFF} = 45MeV·cm^2/mg and T = 125°C.

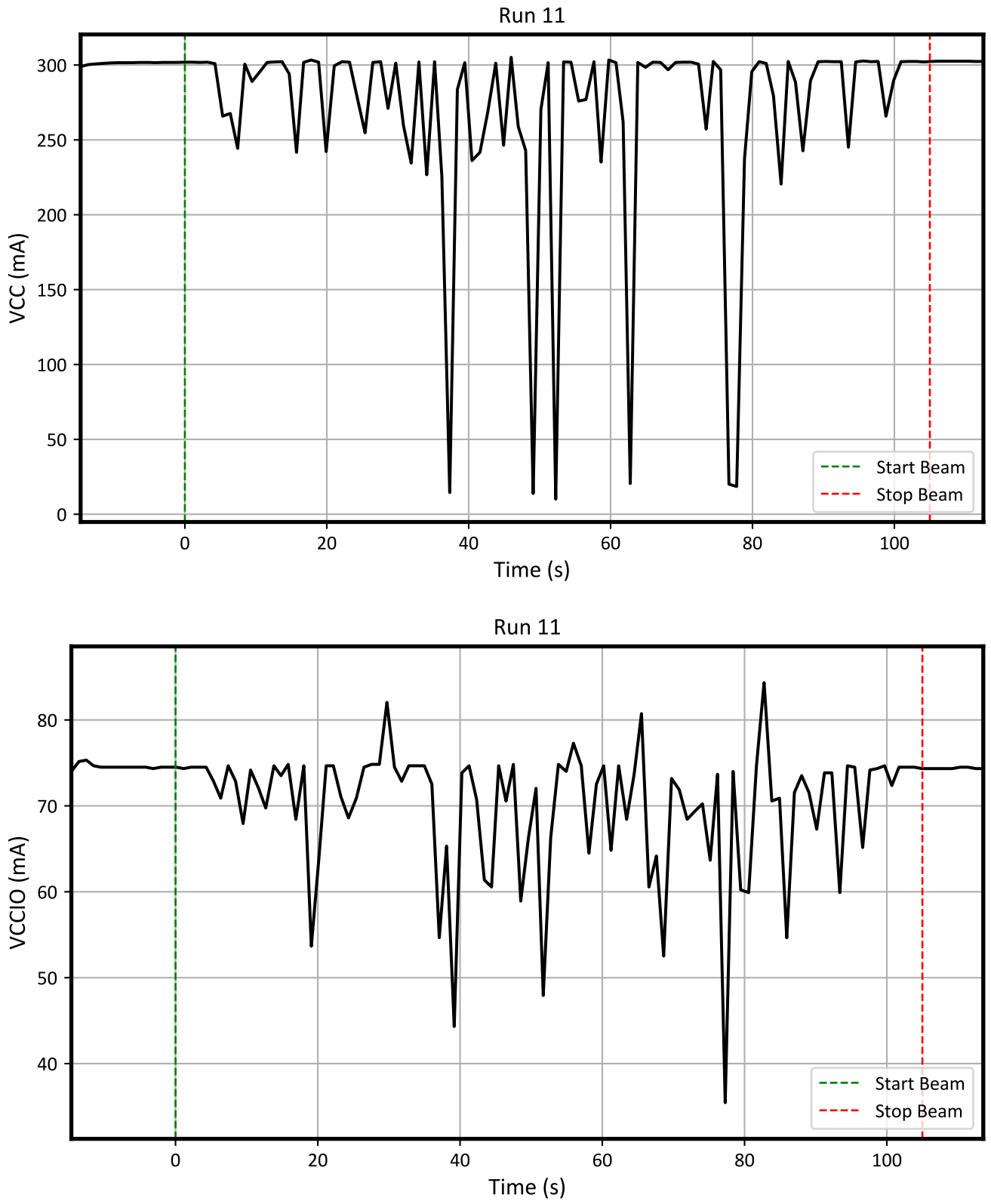


Figure 7-1. Current versus Time for Run #11 of the F28377D-SEP at T = 125°C

8 Single-Event Transients (SET)

SET are defined as heavy-ion-induced transients upsets effecting the logic and/or outputs of the F28377D-SEP device.

Testing was performed at room temperature (no external temperature control applied). The heavy-ions species used for the SET testing were Silver (^{109}Ag),and Argon(^{40}Ar) for an LET_{EFF} = 45MeV·cm^2/m and 8MeV·cm^2/m respectively for more details refer to Ion LET_{EFF}, Depth, and Range in Silicon. Flux of ≅10^4 ions×cm^2/s and a fluence of ≅10^6 ions/cm^2, per run were used for the SET's characterization discussed on this chapter.

The following logic on the F28377D-SEP was tested for SET:

- GPIO input and output
- ePWM output
- SRAM
- Flash

Two Saleae Logic Pro 16 Logic Analyzers were used to capture relevant data, in addition data was also exported via the console of Code Composer Studio IDE for certain tests.

8.1 *GPIO Testing and Results*

The GPIO on the F28377D-SEP device provide the basic transport mechanism for all of the other peripherals on the device. Either inputs or outputs, from outputting PWM waveforms, to using communication protocols for input/output, to basic toggling for status updates the GPIO boundary ultimately controls data into and out of the device.

The following test results focus on the integrity of the GPIOs while under Ion beam stimulus, and SEU and SEFI observed.

8.1.1 GPIO Test Setup

The test setup for GPIO SET testing is shown in Block Diagram for GPIO Test Configuration.

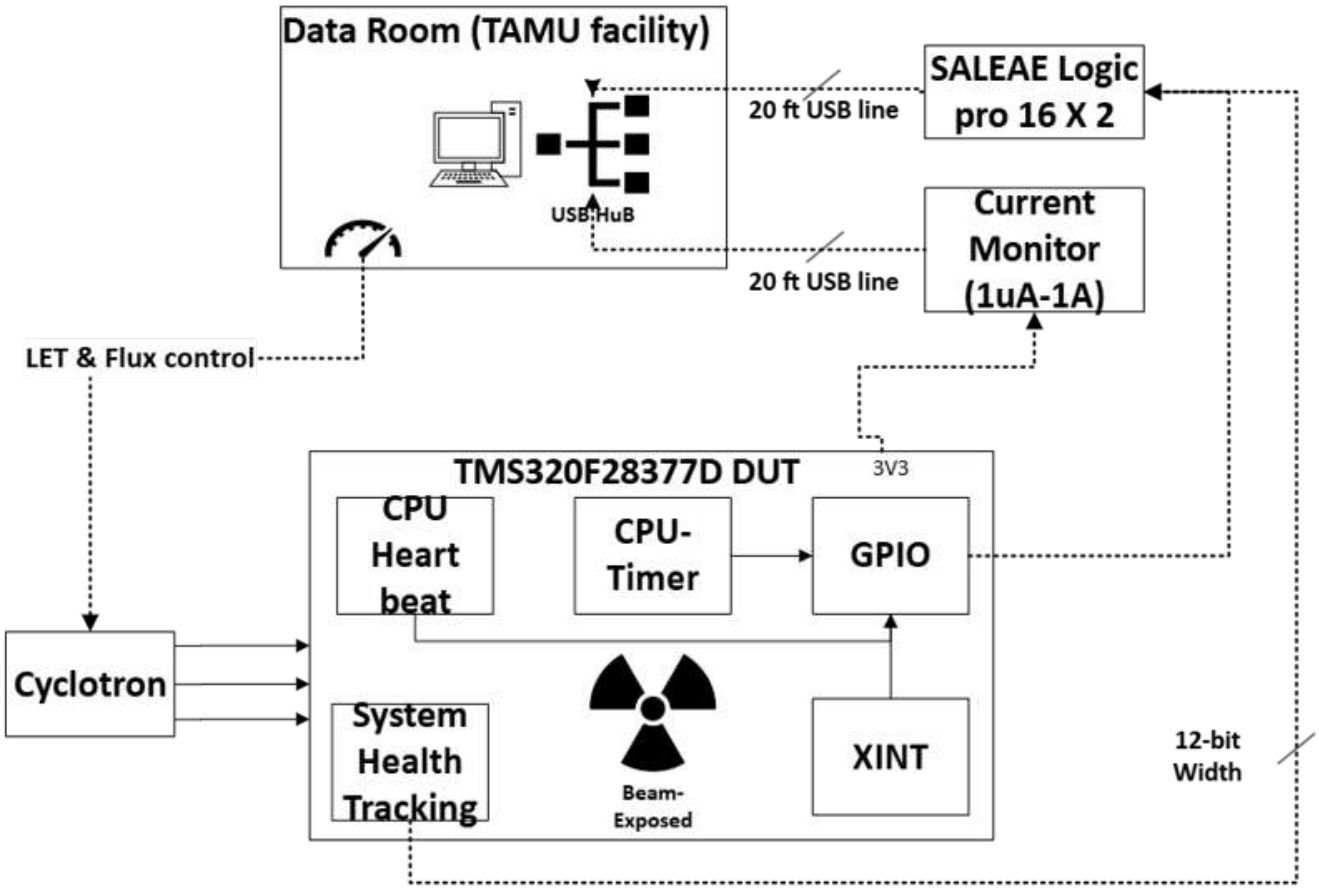


Figure 8-1. Block Diagram for GPIO Test Configuration

The execution code was loaded into the flash memory of the F28377D device, giving the device ability to re-boot into the test code should a fault occur within the code execution itself, relying on the internal watchdog and NMI logic of the device. A "heartbeat" signal at was also brought out in the GPIOs in order to determine if the code was executing correctly. This signal served a dual purpose, both to measure during Ion beam exposure, but also show that the device can recover from a transient event. The GPIOs on the F28377D-SEP device were configured and tested as follows:

- Output
  - GPIO output toggled at various frequencies using CPU timer to identify the susceptibility of various timed events in the space mission that potentially employ the CPU timer.
  - GPIO output held at a static value of “0” or “1” to identify the data retention capability of the GPIO data registers. This configuration also helps in identifying the transient effects induced on the pin due to heavy ions.
  - •GPIO output toggled using a software timer in the program code. The main goal of this configuration is to validate the continuous CPU execution analogous to a heartbeat
- Input
  - XINT triggered by rising and falling edges of the input signal fed into the pins using signal generator at varying frequencies. This configuration tests how well the input fed through the pins is read during the operation. This also evaluates how well time critical external interrupts are serviced in the radiation prone service environment.

Table 8-1. GPIO System Test Configuration Details

Runs	Channels	Pin Function	Test Focus	Test Frequency Range
3	4	Output	CPU Timer and GPIO	1kHz, 10kHz, 100kHz
	4	Output	Static Output	Static
	3	Output	Continuous CPU Execution	1kHz, 10kHz, 100kHz
	4	Input	External Interrupt	1kHz, 10kHz, 100kHz

The fault modeling for each of the tests can be seen in the following figures; CPU Timer Fault Modeling, Figure 8-3, and Figure 8-4.

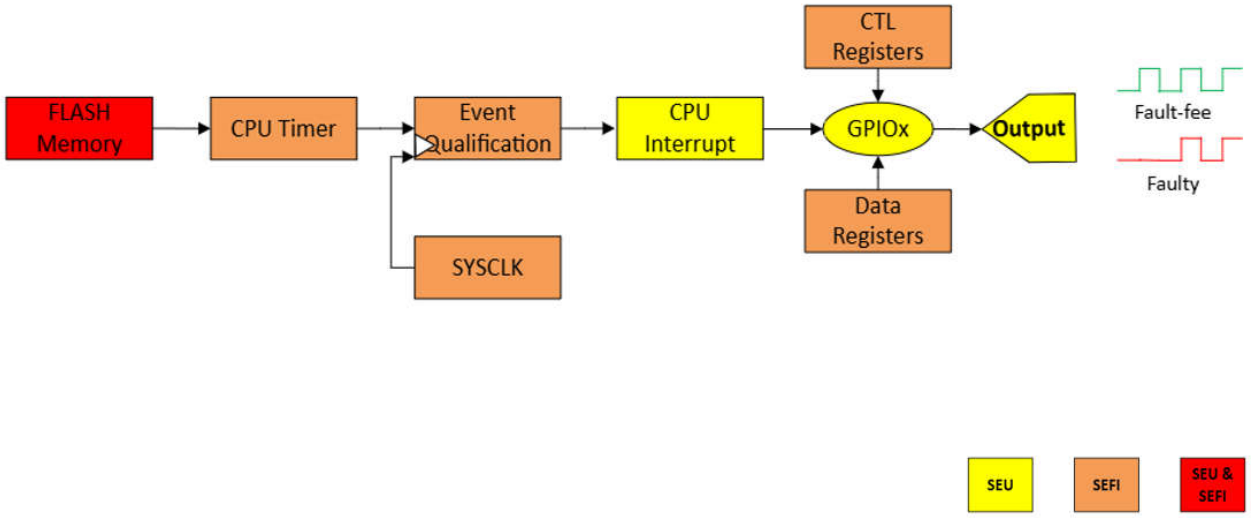


Figure 8-2. CPU Timer Fault Modeling

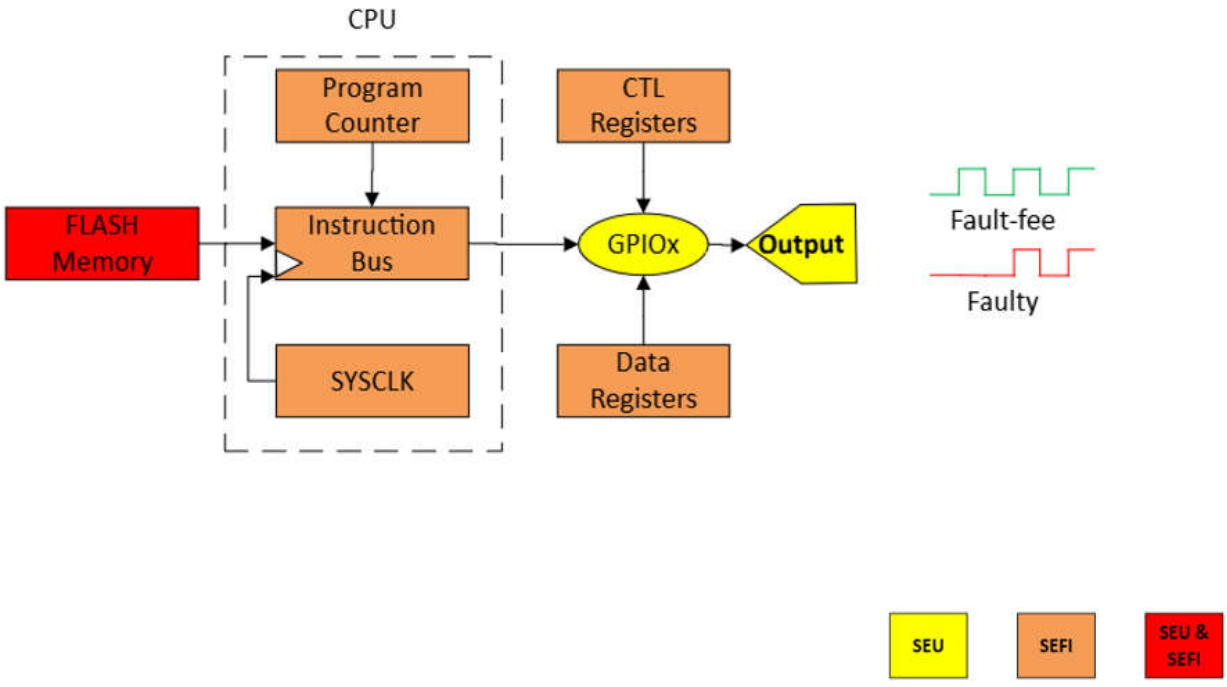


Figure 8-3. CPU Heartbeat Fault Modeling

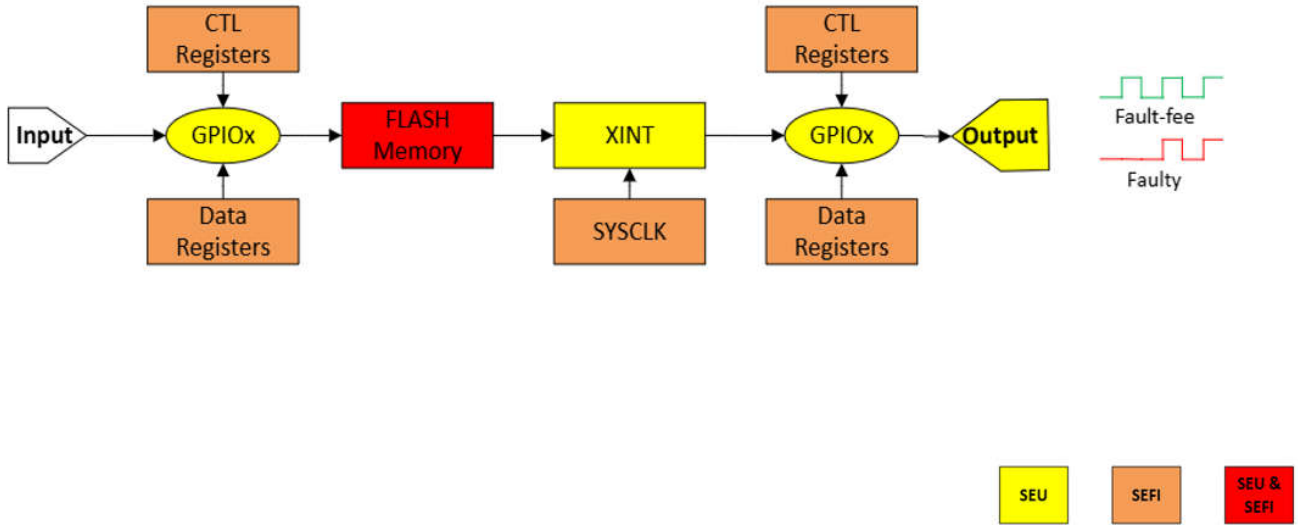


Figure 8-4. Fault Modeling for External Interrupt (XINT) Response

8.1.2 GPIO SET Analysis

Two types of transients were observed during testing of the GPIOs. These are referred to in subsequent sections as Type 1 and Type 2 upsets respectively.

Type 1 upsets occurred local to the GPIO, either in combination with other IOs or as a singular event. In either case these resolved either immediately or after some time duration as shown in Figure 8-5.

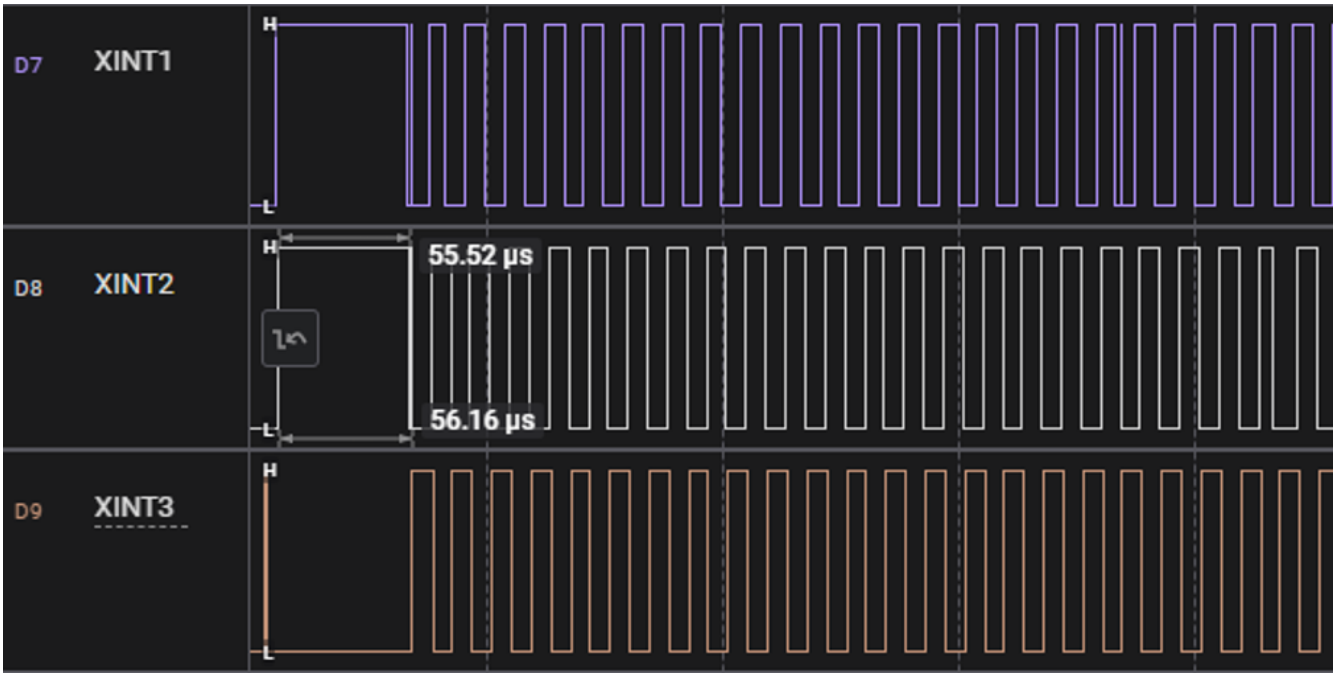


Figure 8-5. Type 1 Transient(SEU) For GPIO

Type 2 upsets were a result of impact to the system code execution, which in turn led to a trigger of the on-chip Watchdog or NMI Watchdog, meant to reset the system in case of a fault. In this case no fault handling was in place for these events, such that if the watchdog timed out or there was a system level NMI, the system was allowed to reset, and subsequently re-boot to flash. In all cases of a Type 2 upset, the system recovered and GPIO output resumed as expected.

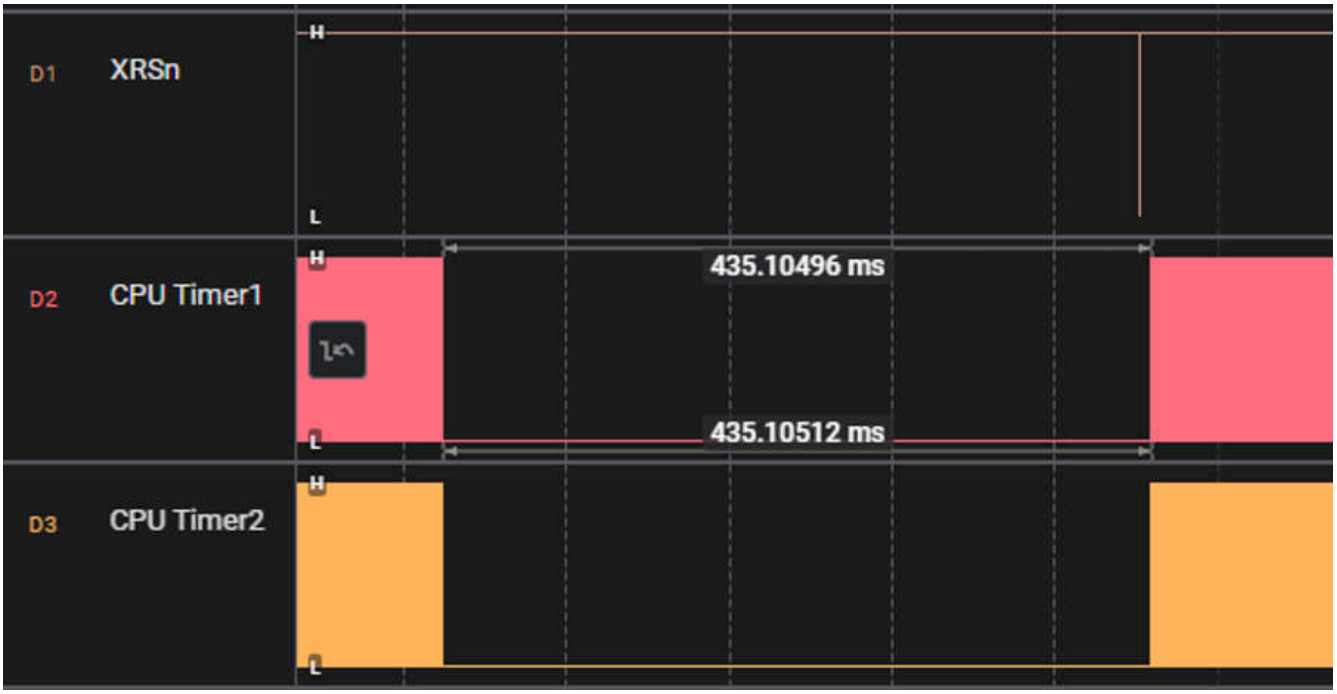


Figure 8-6. Type 2 Transient (Recoverable SEFI) For GPIO

8.1.3 GPIO SET Summary

The transient event counts and event cross sections are shown in Table 8-2 for the different test procedures outlined previously. Key takeaways as follows:

- All faults observed are either temporary or were recoverable with a reset to the system
- The values written to the GPIO data registers, internal to the device, during the static output test were not-effected/did not show correlation to the output state change in the IO. This implies that the SET was local to the output/input buffer itself, versus to the internal logic that controls the IO signal.

Table 8-2. GPIO Transient Upset Summary

Test Pattern	LET_{EFF}(MeV·cm^2/mg	Ion Type	Transient Type	Event Count	Fluence (# of ions)	Cross Section(Event Count/LET_{EFF}
CPU Timer	45	^{109}Ag	Type 1	23	1.01 E^5	2.29 E^{-5}
CPU Timer	8.5	^{40}Ar	Type 1	20	1.00 E^5	1.98 E^{-5}
CPU Timer	45	^{109}Ag	Type 2	83	1.01 E^5	8.26 E^{-5}
CPU Timer	8.5	^{40}Ar	Type 2	25	1.00 E^5	2.44 E^{-5}
HB	45	^{109}Ag	Type 1	54	1.01 E^5	5.37 E^{-5}
HB	8.5	^{40}Ar	Type 1	13	1.00 E^5	1.26 E^{-5}
HB	45	^{109}Ag	Type 2	65	1.01 E^5	6.47 E^{-5}
HB	8.5	^{40}Ar	Type 2	19	1.00 E^5	1.84 E^{-5}
XINT	45	^{109}Ag	Type 1	294	1.01 E^5	2.92 E^{-4}
XINT	8.5	^{40}Ar	Type 1	14	1.00 E^5	1.38 E^{-5}
XINT	45	^{109}Ag	Type 2	105	1.01 E^5	1.04 E^{-4}
XINT	8.5	^{40}Ar	Type 2	19	1.00 E^5	1.88 E^{-5}

8.2 ePWM Testing and Results

EPWM modules are highly programmable, extremely flexible, and easy to use, while being capable of generating complex pulse width waveforms with minimal CPU overhead or intervention. Each EPWM module is identical with two PWM outputs, EPWMxA and EPWMxB. Multiple EPWM modules can be synchronized to operate

together as needed within a system (please refer to your device's documentation on the specific order of the EPWM module synchronization scheme). The generated PWM waveforms are available as outputs on GPIO pins on the microcontroller.

The EPWM module can also interact closely with other peripherals. For example, EPWM's can trigger ADC start-of-conversion (SOC) signals, and EPWM's can generate interrupts to the interrupt controller block. External signals can also be used to alter an EPWM output, if needed, as well as generate interrupts. Additionally, the outputs of comparators on the device can be used as inputs to the EPWM by leveraging connectivity through the EPWM X-BAR module.

8.2.1 ePWM Testing Setup

The test setup for ePWM SET testing is show in Figure 8-7.

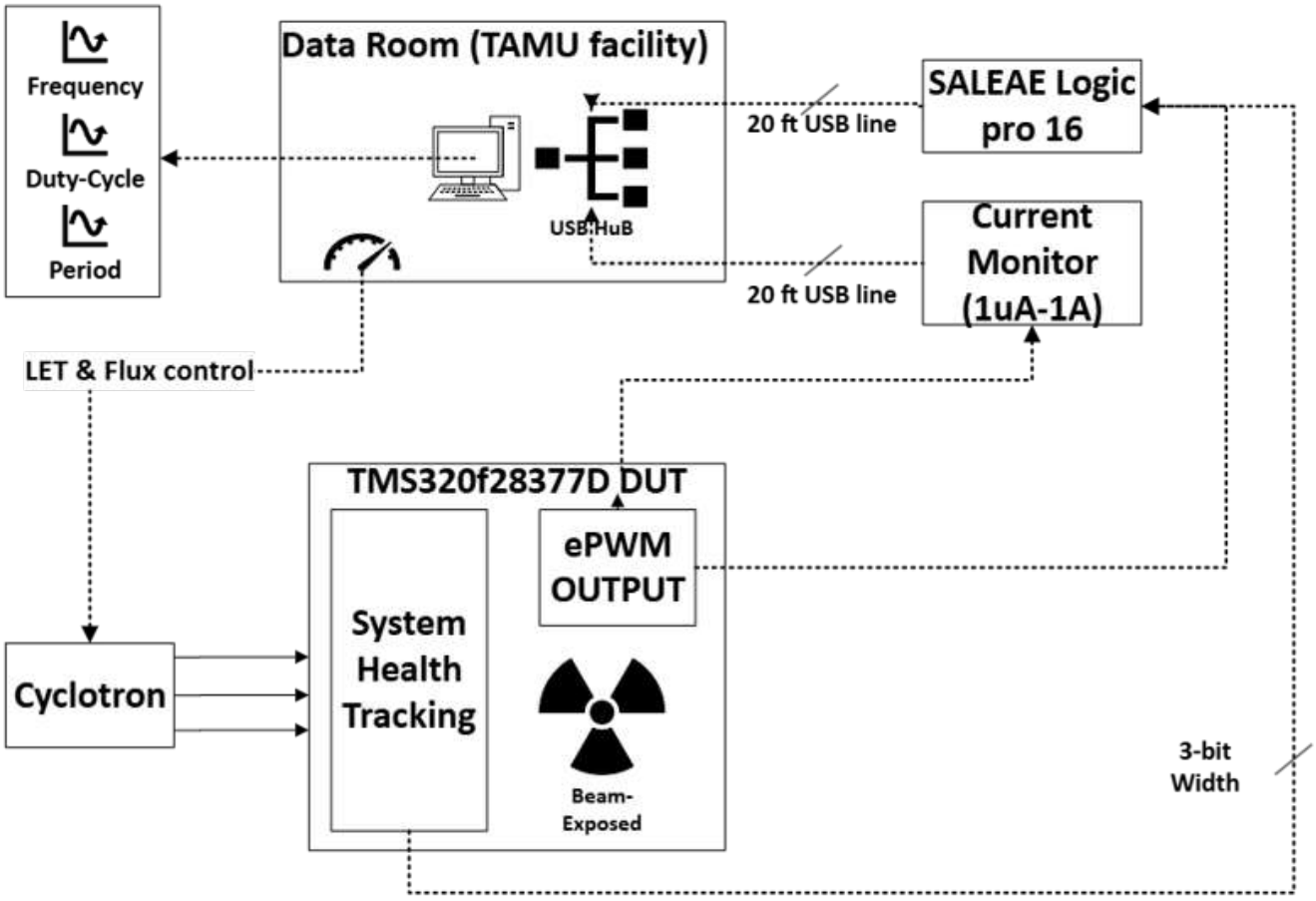


Figure 8-7. Block Diagram for ePWM Test Configuration

The execution code was loaded into the flash memory of the F28377D device, giving the device ability to re-boot into the test code should a fault occur within the code execution itself, relying on the internal watchdog and NMI logic of the device. A "heartbeat" signal at was also brought out in the GPIOs in order to determine if the code was executing correctly. This signal served a dual purpose, both to measure during Ion beam exposure, but also show that the device can recover from a transient event.

Twelve PWM signals were brought to the device pins, consisting of 6 PWM modules with the A and B channels of each module comprising the 12 signals. The phase of wave A is complementary to wave B, and both were monitored for consistency to one another in addition to the correct frequency.

Deadband of 200ns was inserted on channels 4B and 7B on the falling edge of the A output to test the deadband logic. The summary of the different test runs are shown in Table 8-3.

Table 8-3. GPIO System Test Configuration Details

Runs	PWM Channels	Frequency	Duty Cycle	Dead Band Inserted
3	12	1kHz	10	No
			50	
			90	
	2	1kHz	10	200ns
			50	
			90	
	12	10kHz	10	No
			50	
			90	
	2	10kHz	10	200ns
			50	
			90	
	12	100kHz	10	No
			50	
			90	
	2	100kHz	10	200ns
			50	
			90	

The fault modeling for the PWM testing is shown below Figure 8-8.

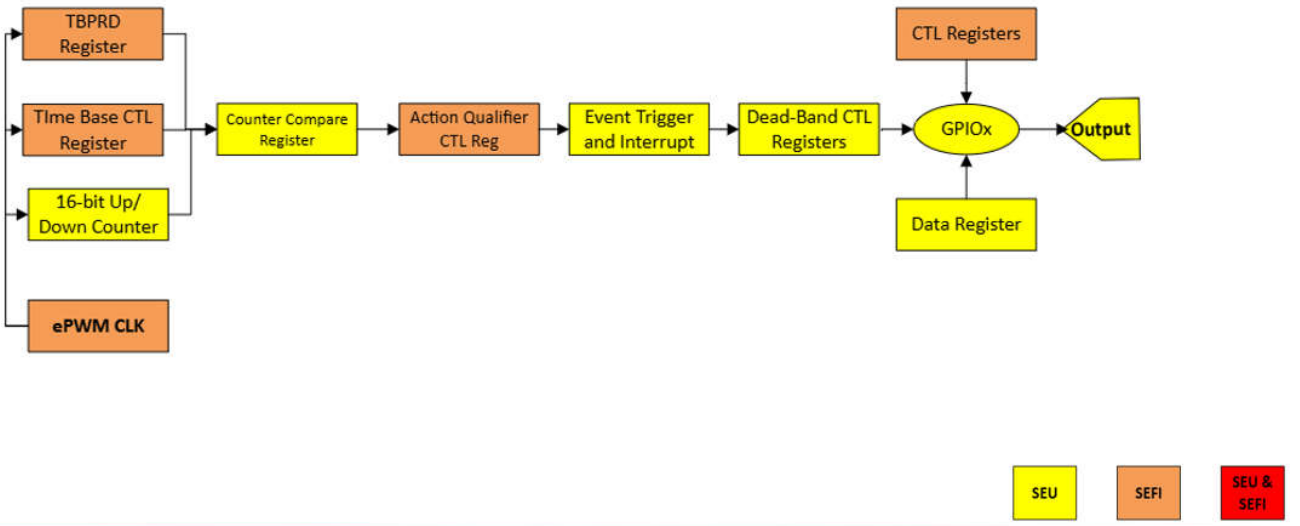


Figure 8-8. PWM Fault Modeling

8.2.2 ePWM SET Analysis

Three types of transients were observed during testing of the ePWMs. These are referred to in subsequent sections as Type 1, Type 2, and Type 3 upsets respectively.

Type 1 upsets occurred local to the PWM, across the pairs of PWM outputs Figure 8-9. This error was self corrected without intervention from the CPU, CPU watchdog or NMI watchdog modules.

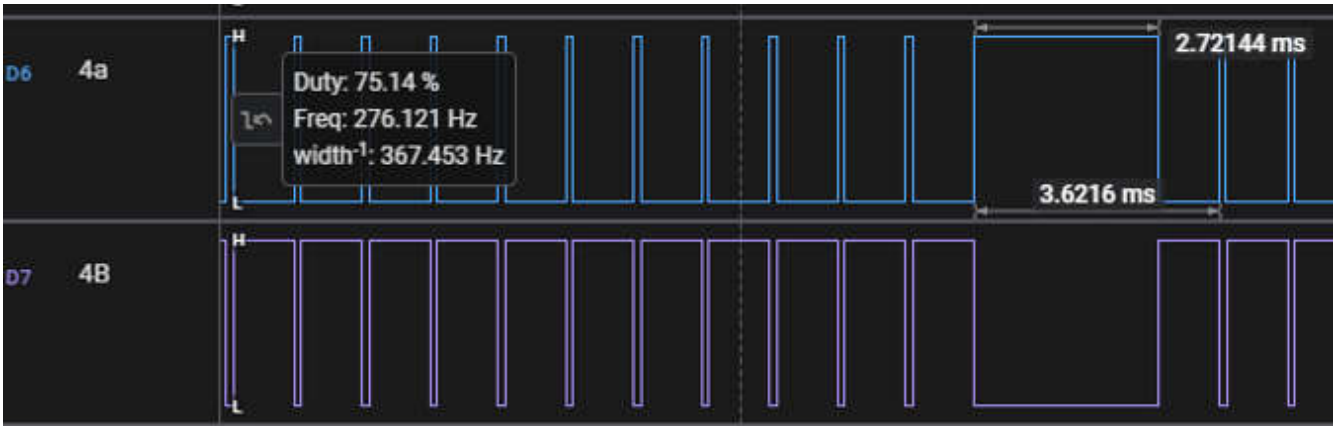


Figure 8-9. Type 1 Transient (SEU) Dual Channel Event

Type 2 upsets did not resolve on their own independent of a CPU reset event, caused by either a Watchdog or NMI Watchdog, meant to reset the system in case of a fault. During this testing no fault handling was in place for these events, such that if the watchdog timed out or there was a system level NMI, the system was allowed to reset, and subsequently re-boot to flash. In all cases of a Type 2 upset, after reboot, the system recovered and PWM output resumed as expected. This is not a PWM fault per se, but rather a system upset. The time duration shown in Figure 8-10 is the result of the maximum/default value of the NMI Watchdog resulting boot up time of the device. Figure 8-11 illustrates the effect of change in duty cycle on the complement of PWM 3, that was not corrected until an automatic reset event occurred. It is important to note that due to the critical nature of PWMs complementary outputs, typically driving separate FETs that should not be turned on at the same time, the external FET driver needs to be capable of detecting this illegal condition and not pass the raw PWM to the FET itself. The TPS7H36015-SEP gate driver from TI has interlock protection and can be used in combination with the F28377D-SEP to provide this protection.

Figure 8-10. Type 2 Transient Dual Channel Event

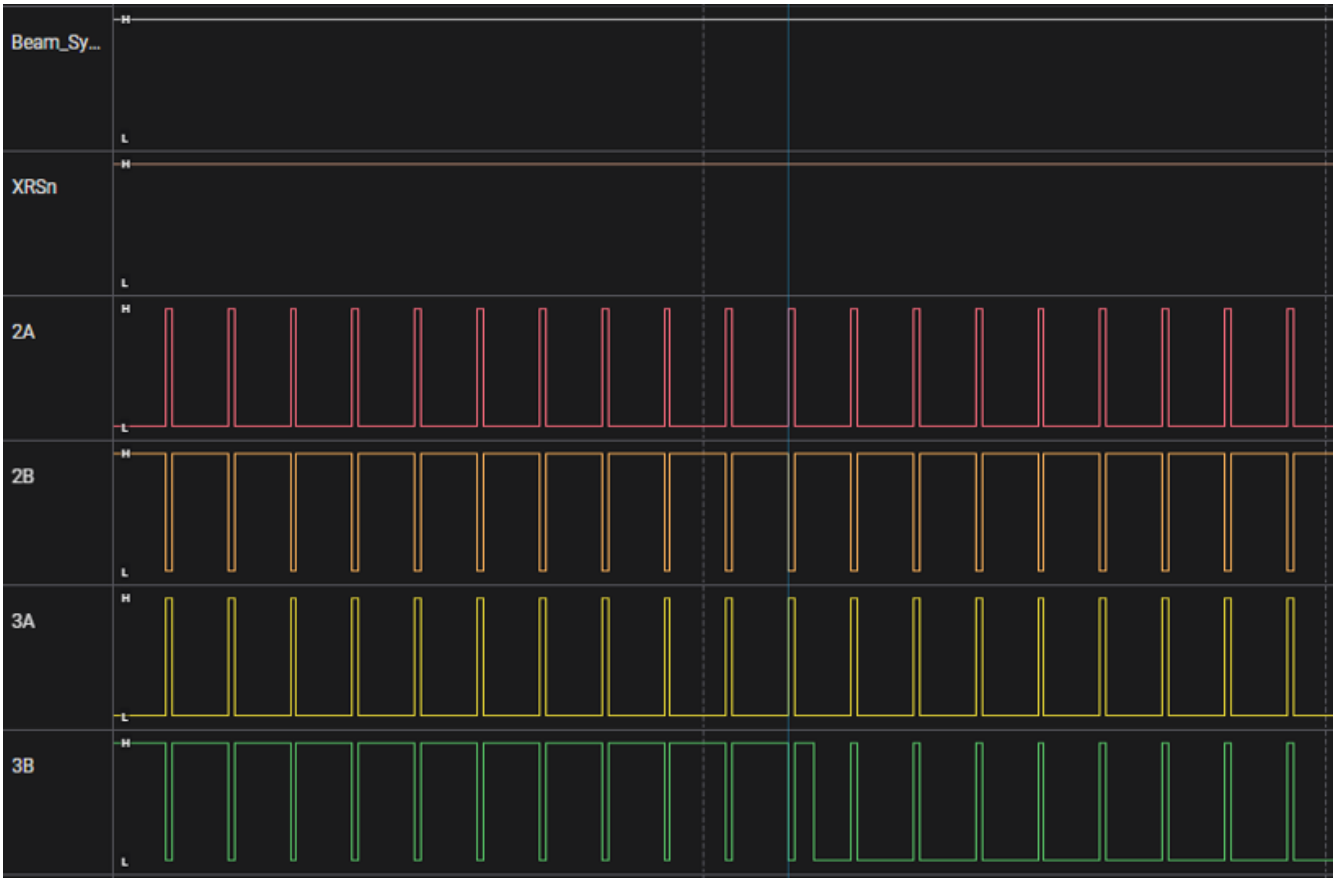


Figure 8-11. Type 2 Transient Duty Cycle Event

Type 3 upsets were unique in that a SEFI occurred, but neither self corrected, nor was corrected by one of the system monitors as in Type 2 upsets. These upsets were rare, however, need to be accounted for in a system design. There was no damage to the device, but the device state was not recovered automatically. Figure 8-12 demostrates the output captured for a Type 3 event, in which both PWM2 outputs go inactive and do not recover by the end of the test run.Figure 8-13 demonstrates another Type 3 event where the ePWM deadband is impacted periodically, but persists for the duration of the SET test.

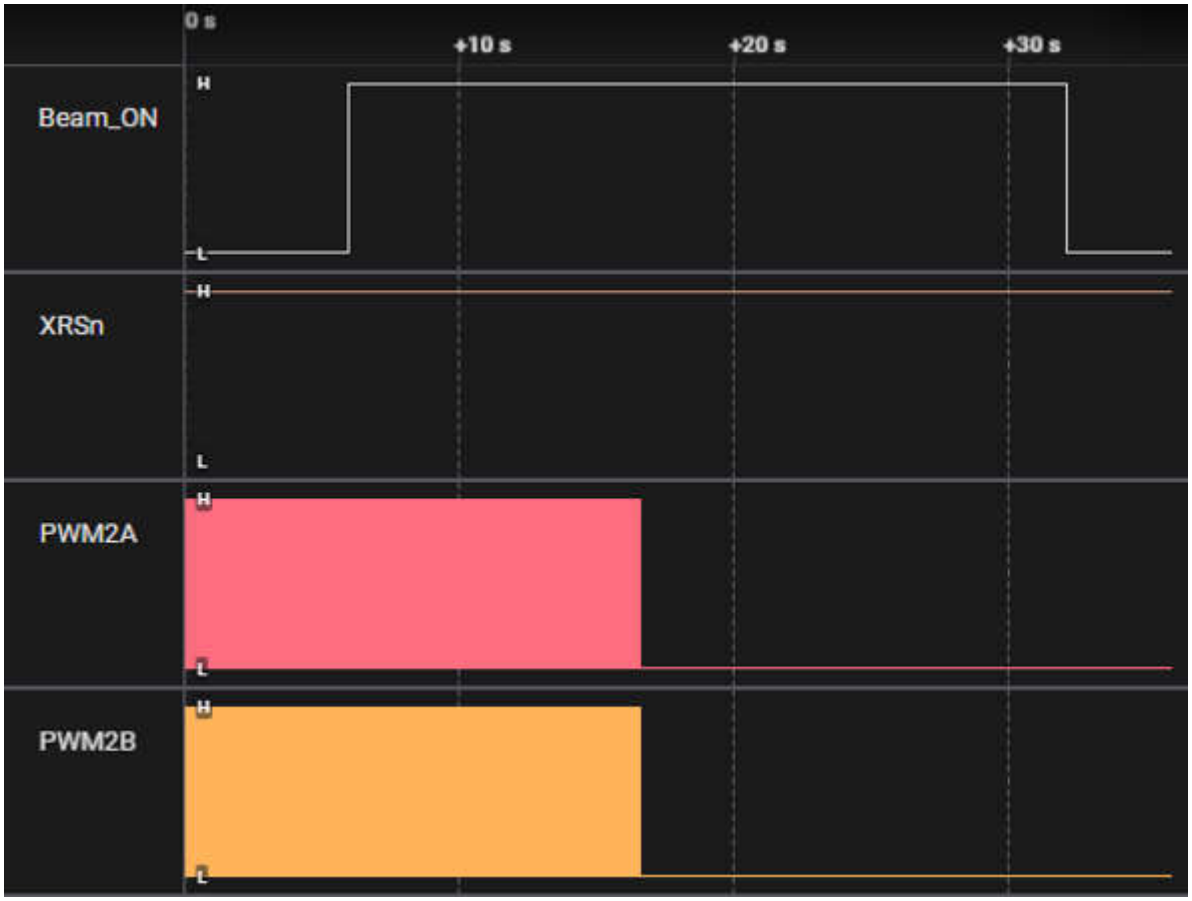


Figure 8-12. Type 3 Non-Recoverable SEFI

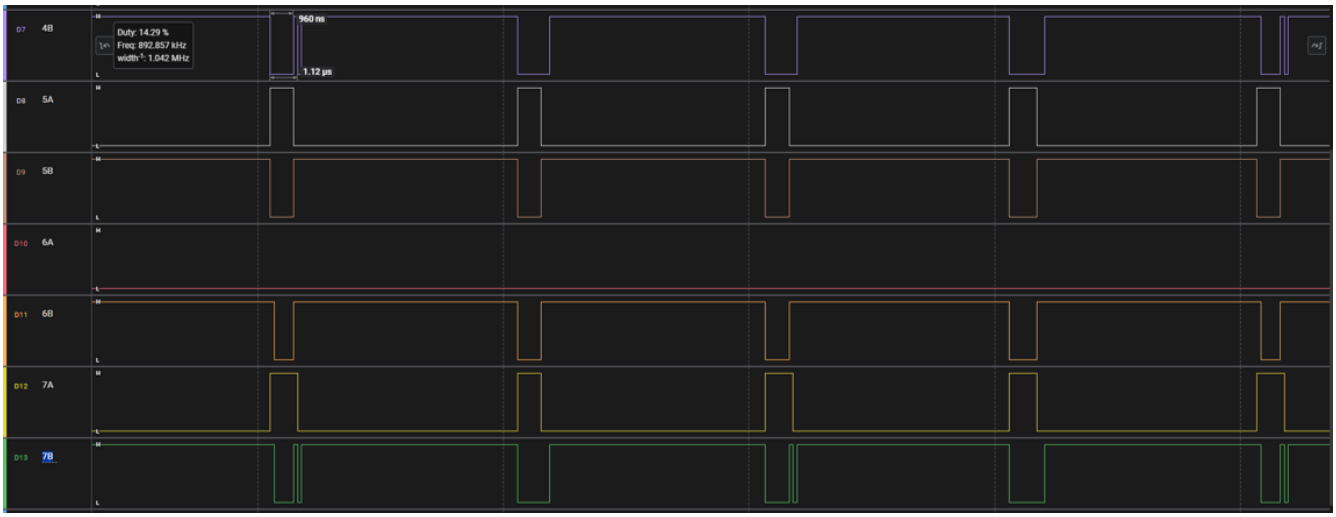


Figure 8-13. Type 3 Non-Recoverable SEFI on PWM Deadband

8.2.3 ePWM SET Summary

The ePWM transient event counts and event cross sections are shown in Table 8-4. Key takeaways from this testing are as follows:

- Type 1 and Type 2 faults have similar occurrence rates versus Type 3 faults, which are an order of magnitude less likely to occur

- In all cases, there is potential for a PWM primary output and complementary output (A and B outputs) to be un-evenly effected by radiation effects. Due to this it is recommended to choose a gate driver that has interlock protection.

Table 8-4. ePWM Transient Upset Summary

Test Pattern	LET_{EFF}(MeV·cm²/mg	Ion Type	Transient Type	Event Count	Fluence (# of ions)	Cross Section(Event Count/LET_{EFF} [1]
ePWM	45	^{109}Ag	Type 1	100	9.95 E^{5}	1.37 E^{-4}
ePWM	8.5	^{40}Ar	Type 1	9	9.96 E^{5}	4.70 E^{-6}
ePWM	45	^{109}Ag	Type 2	62	1.01 E^{6}	5.93 E^{-5}
ePWM	8.5	^{40}Ar	Type 2	12	9.96 E^{5}	3.26 E^{-6}
ePWM	45	^{109}Ag	Type 3	2	8.13 E^{5}	4.35 E^{-7}
ePWM	8.5	^{40}Ar	Type 3	1	7.44 E^{5}	1.49 E^{-6}

1. Some runs had no recorded transients, as such an assumed MFTF was substituted for those runs and the average cross section calculation for this transient.

8.3 SRAM Testing and Results

C2000 controllers, in general have 4 groups of SRAMs:

- M0/M1 RAMs: Dedicated to the C28x CPU core
- Pie Vector Table RAM: RAM used to hold the ISR Vectors
- LSx RAMs: Local Shared RAM, Accessible by both the C28x and CLA
- GSx RAMs: Global Shared RAM, Accessible by the C28x and DMA
- Message RAMs: RAM used to communicate between mutliple CPU subsystems.

The F28377D-SEP device also includes additional RAM blocks based on the IP on the device.

- CAN Message RAM: RAM local to the CAN IP used to buffer message traffic
- UPP TX/RX Message RAM: RAM local to the UPP IP used to buffer message traffic

Additionally, different RAM types have ECC(Error Correction Code) or Parity to correct or detect errors. ECC is SECDED implementation, Single (Bit) Error Correction, Dual (Bit) Error Detection. This is valid on every 32-bits for RAM and includes the address. Parity implementation is single bit error detect on every 32-bits This is useful in the radiation environment due to both soft and hard errors caused by ion strikes.

The SRAM on the F28377D-SEP also provides access protection logic in HW that can both block and alert to unplanned CPU accesses(either data or program) into specific memory addresses. This can be useful to prevent an ion upset/transient from disrupting code execution.

The below table Table 8-5 provides information on the various SRAM type on the F28377D-SEP device. For additional information on the memory subsystem please refer to the Memory Controller Module section of the device TRM.

Table 8-5. F28377D RAM Types

Memory Type	Size Each (KB)	ECC-Capable	Parity	Access Protection
M0,M1	2KB	Yes	-	-
D0, D1	4KB	Yes	-	Yes
LSx	4KB	-	Yes	Yes
GSx	8KB	-	Yes	Yes
MSG RAM	2KB	-	Yes	Yes
PIE Vect RAM	1KB	-	-	-

Note

While the PIE Vector RAM does not have traditional ECC or parity protection, there exists a full backup/duplication of the RAM and a comparison between both values is done on a vector fetch. This is intended to provide coverage for any inconsistencies in the RAM.

8.3.1 SRAM Test Setup

The test setup for SRAM is shown in Figure 8-14.

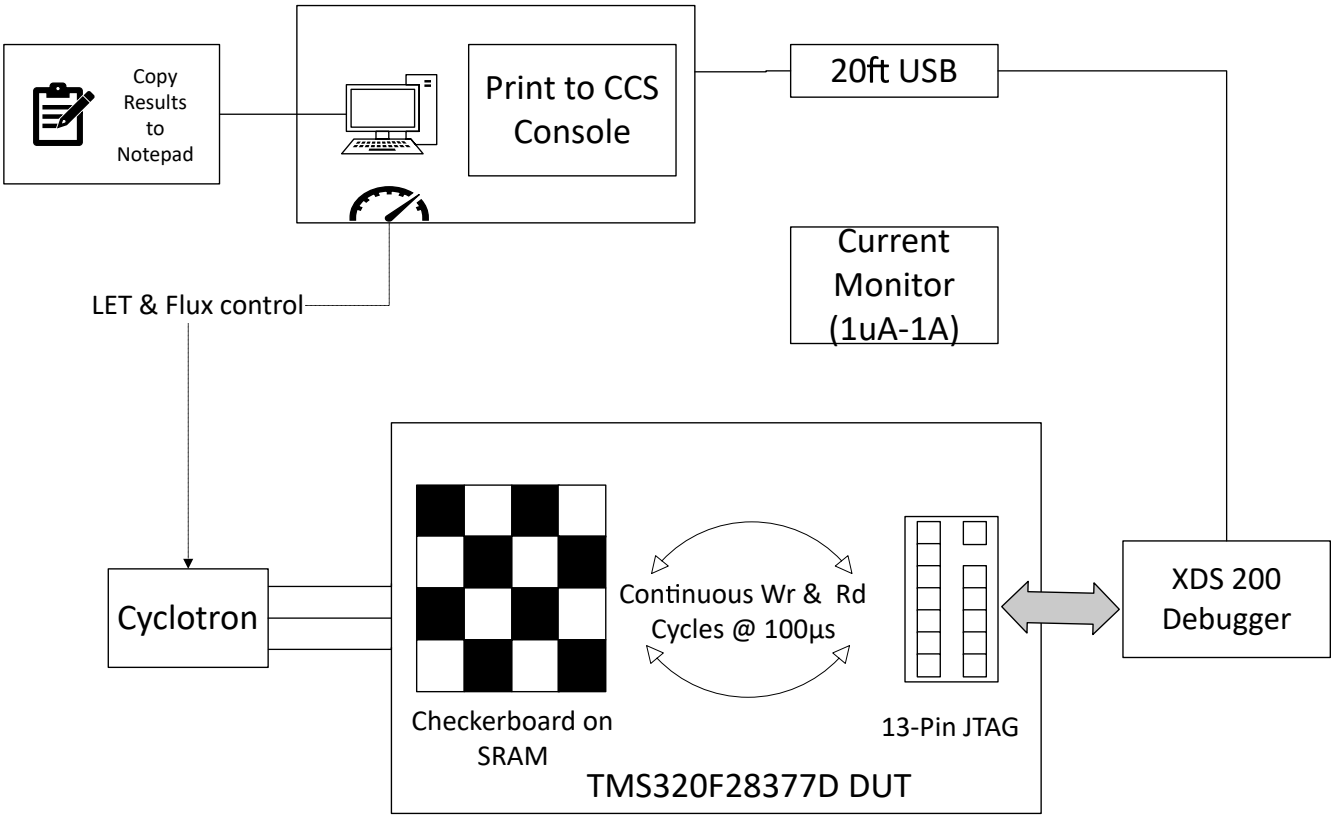


Figure 8-14. Block Diagram for SRAM Test Configuration

For this test, the C28x CPU was used to read and write to the SRAM. To avoid transient upsets to that logic as well as any other logic not under test, a mask was used to block the ion beam from any other logic other than the SRAM under test. The F28377D-SEP does not allow for ECC or Parity disable for the on-chip SRAM. In the case of parity protected SRAMs this would not limit the detected errors, for ECC protected errors, any single bit error, for example a correctable error, is ignored from the failure rate. Both scenarios match the end use case, and as such the data can be used directly to determine the failure rate during mission. Table 8-6 gives the details of the various tests that were ran during the transient testing.

Table 8-6. SRAM Test Configuration

Runs	Test Type	Target Memory	WR+RD Frequency
3	Dynamic	MX and DX RAM	Write and Read all SRAMs every 100µs
3	Dynamic	GX RAM	Write and Read all SRAMs every 100µs

8.3.2 SRAM SET Summary

The SRAM transient event count is shown in Table 8-7 Key takeaways from the data are:

- ECC protected SRAM(Mx and Dx RAMs) are two orders of magnitude less susceptible to transient upsets. This implies that during the read/write duration the majority of upsets are single bit correctable errors

- Due to the nature of ECC implementation on SRAMs, a correctable error is not only corrected prior to use by the CPU, but the corrected value is also written back to the SRAM avoiding aggregated errors
- Parity protected SRAM(LSx and GSx), while observing more failures than the ECC protected RAMs, will be able to detect most transients due to their single bit nature.
- While all SRAMs are constructed similarly, it is important to keep in mind that due to size and number of instances that GSx SRAM will have a higher probability of transient events based on its on die area.

Table 8-7. SRAM Transient Upset Summary

SRAM Type	LET_{EFF}(MeV·cm^2/mg	Ion Type	Bit Flips	Bit Total	Fluence (# of ions)	Cross Section(Event Count/LET_{EFF}
Mx and Dx (ECC) RAMs	45	^{109}Ag	0	98304	1.00 E^6	1.85 E^{-6} 1
Mx and Dx (ECC) RAMs	8.5	^{40}Ar	0	98304	1.01 E^6	6.07 E^{-7} 1
LSx and GSx(Parity) RAMs	45	^{109}Ag	3230	1,245,84	1.00 E^6	2.27 E^{-4}
LSx and GSx(Parity) RAMs	8.5	^{40}Ar	521	1,245,84	1.01 E^6	3.47 E^{-5}

1. Since there were no upsets observed the cross section for this section is calculated as a Mean Fluence To Fail (MFTF) at 95% confidence interval based on the average fluence of the runs. See *Single-Event Effects Confidence Interval Calculations* for more information on this calculation.

8.4 Flash Memory Testing and Results

The F28377D-SEP has a total of 1MB of non-volatile flash memory. The memory is divided evenly between the 2 CPUs, 512KB available for each CPU. The flash is further divided into 13 sectors with two sizes; either 16KB or 64KB. All flash memory has optional ECC protection, allowing for single bit correction and dual bit detection on 64-bit data word boundaries. There is also data cache and prefetch buffers to increase the throughput of flash execution. While the relative size of both of these buffers is relatively small, there is no error correction or detection on these memories.

8.4.1 Flash Test Setup

The test setup for flash is shown in Figure 8-15.

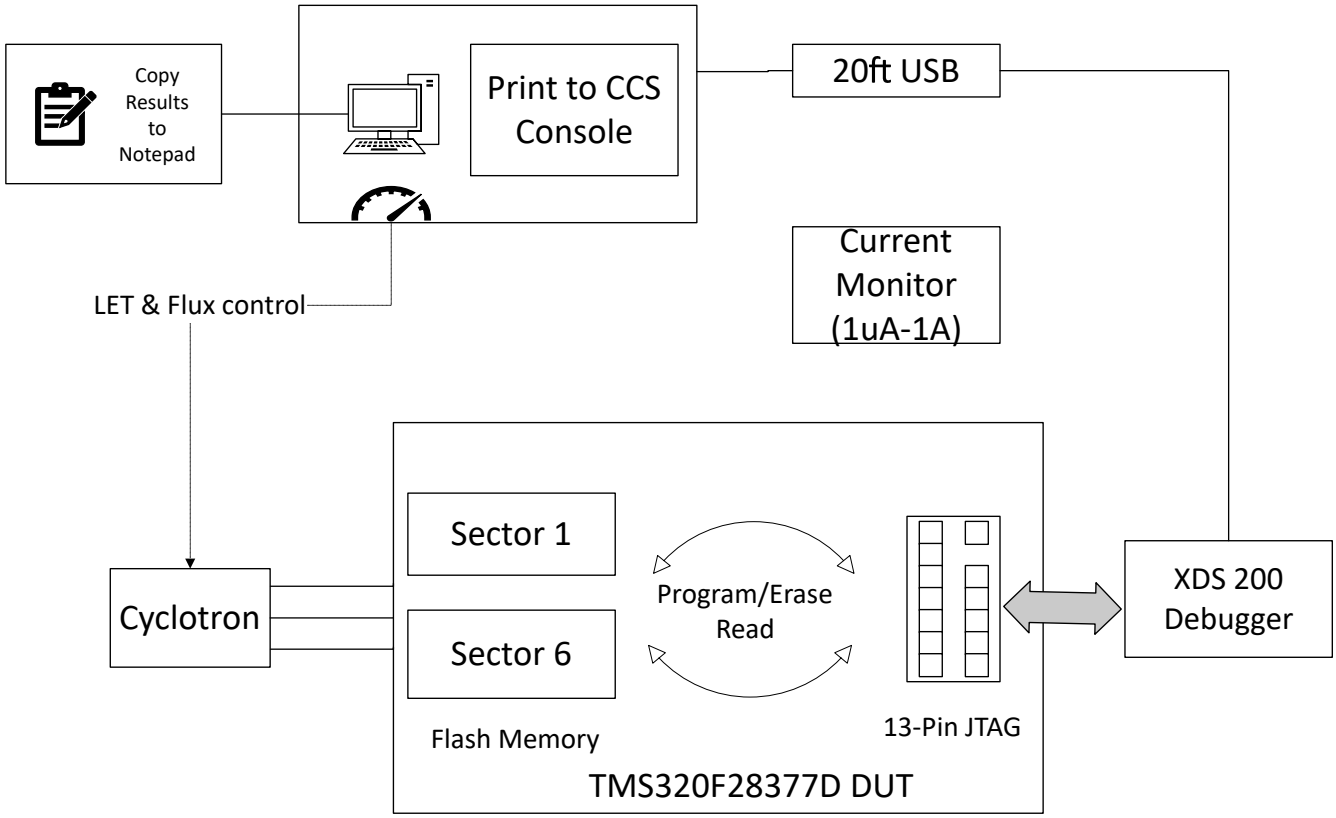


Figure 8-15. Block Diagram for Flash Test Configuration

Table 8-8 shows the various tests that were conducted for transient analysis of the flash memory. The term "clear" refers to setting all bits in the sector to a logical zero. The term "erase" refers to setting all bits in the sector to a logic one. Sector 1 and sector 8 were choses to be representative of the two difference size flash banks, 16KB and 64KB respectively.

Two main types of tests were conducted:

- Static Tests: Tests where the flash was programmed prior to ion beam exposure, exposed to the ion beam, and then contents of the flash were read back
- Dynamic Tests: Tests where the flash was either programmed during ion beam exposure or simply read back during ion beam exposure

Table 8-8. Flash Tests

Runs	Test Type	Target Memory	Test Description
3	Static Zeros	Sector 1 and Sector 8	• Write all zeros to both sectors • Expose flash to ion beam • Read back sectors after ion beam exposure
3	Static Ones	Sector 1 and Sector 8	• Write all ones to both sectors • Expose flash to ion beam • Read back sectors after ion beam exposure
3	Dynamic Writing Zeros	Sector 1 and Sector 8	• All below during ion beam exposure • Repeatedly clear/erase flash • Check for clear

Table 8-8. Flash Tests (continued)

Runs	Test Type	Target Memory	Test Description
3	Dynamic Writing Ones	Sector 1 and Sector 8	• All below during ion beam exposure • Repeatedly erase/clear flash • Check for erase
3	Dynamic Reading Zeros	Sector 1 and Sector 8	• Write zeros to all sectors • Repeatedly read back sectors while ion beam is on
3	Dynamic Reading Zeros	Sector 1 and Sector 8	• Write ones to all sectors • Repeatedly read back sectors while ion beam is on

8.4.2 Flash SET Summary

Flash SET summary is shown in Table 8-9. For flash memory only the Silver Ion (45MeV) was tested thus far. There were no transients/upsets observed during flash testing. As such the cross section has been calculated using a 95% confidence interval and Mean Fluence To Fail approach.

Table 8-9. Flash Test Summary

Test	Number of Runs	Avg Fluence(ions/cm^2)	Results	Cross Section(Event Count/LET$_{EFF}$ [1]
Static zeros	3	1.00 E^6	No read errors seen post ion beam	3.69 E^{-6}
Static ones	3	1.00 E^6	No read errors seen post ion beam	3.69 E^{-6}
Dynamic writing zeros	3	1.00 E^6	20 consecutive writes per run while under beam, no errors detected	3.69 E^{-6}
Dynamic writing ones	3	1.00 E^6	5 consecutive writes per run while under beam, no errors detected	3.69 E^{-6}
Dynamic reading zeros	3	1.00 E^6	1500 reads of both sectors while under beam, no errors detected	3.69 E^{-6}
Dynamic reading ones	3	1.00 E^6	1500 reads of both sectors while under beam, no errors detected	3.69 E^{-6}

1. Since there were no upsets observed the cross section for this section is calculated as a Mean Fluence To Fail (MFTF) at 95% confidence interval based on one device under test. See *Single-Event Effects Confidence Interval Calculations* for more information on this calculation.

9 Summary

The purpose of this study was to characterize the effect of heavy-ion irradiation on the single-event effect (SEE) performance of the F28377D-SEP 32-bit real-time control MCU. Heavy-ions with LET_{EFF} = 8 to 45MeV·cm^2/mg were used for the SEE characterization campaign. Flux of ≈10^4 to 10^5 ions/cm^2 ·s and fluences of ≈10^6 to 10^7 ions/cm^2 per run were used for the characterization. The SEE results demonstrated that the F28377D-SEP is free of destructive SEL LET_{EFF} = 45MeV·cm^2/mg and across the full electrical specifications. Transients at LET_{EFF} = 8 to 45MeV·cm^2 /mg are presented and discussed.

A Total Ionizing Dose from SEE Experiments

The production F28377D-SEP is rated to a total ionizing dose (TID) of 30 krad(Si). In the course of the SEE testing, the heavy-ion exposures delivered ≈10 krad(Si) per 10^7 ions/cm^2 run. The cumulative TID exposure was controlled below 30krad (Si) per unit. All six F28377D-SEP devices used in the studies described in this report stayed within specification and were fully-functional after the heavy-ion SEE testing was completed.

B References

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