Application Note

AM62P DSS Overview

Aradhya Bhatia, Krunal Bhargav, Divyansh Mittal

ABSTRACT

This application note details the Linux-based configuration of key display interfaces on Sitara™ AM62P processors, including Display Parallel Interface (DPI), Display Serial Interface (DSI), and OpenLDI/LVDS. The AM62P System-on-Chip (SoC) is built with two Display SubSystems (DSS), each containing two Video Ports (VPs), which can be flexibly routed through integrated DSI and OLDI bridges. This document explores the various supported output configurations, demonstrating how to drive up to three displays simultaneously. Furthermore, since the DSS module in related Sitara processors (AM62x, AM62A, AM62L) is a subset of the AM62Ps, mastering the configuration enables engineers to efficiently implement display solutions across the broader Sitara AM6x product line.

Table of Contents

Trademarks

1 Introduction

1.1 DSS Components

Figure 1-1 shows the flow diagram of data within the DSS. Table 1-1 gives a brief overview for each of the components inside DSS.

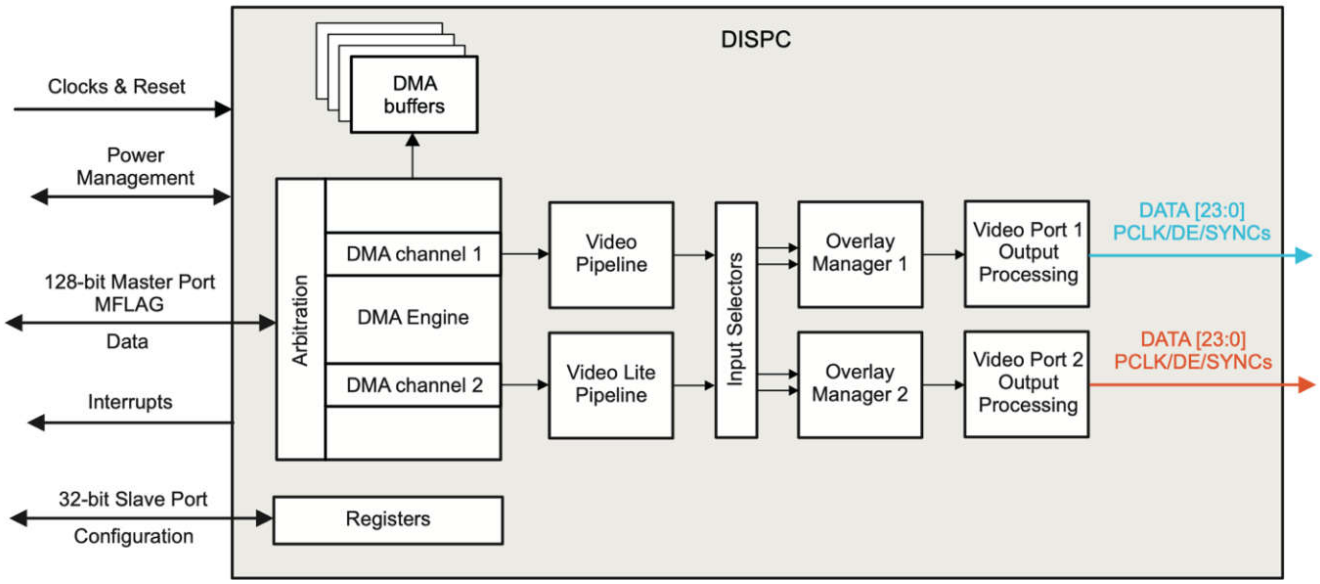

Figure 1-1. DISPC Architecture Overview

Table 1-1. DSS Components Overview

Component Name	Description	Supported Features
DMA Engine	Allows direct access to the frame buffer located inside the device system memory.	**Multiple DMA Internal Buffers:** 2 DMA buffers and each supports size of 40 KB **1D transfers only** **Self refresh mode**: Data is fetched once into the DMA buffer and then the following frames re-use the DMA channels to display on the screen.
Video Pipeline (VID) / Video Lite Pipeline (VIDL)	DSS has 2 pipelines: Video pipeline and Video-lite pipeline. These pipelines are the frame processing entity of the DSS. They carry out operations directly on the frames fetched by the DMA Engine.	**Supports all Pixel Formats** All the BITMAP, YUV and RGB pixel formats are supported. **Color Space Conversion** Converts pixels from YUV color-space to RGB color-space. **Video Color Look-Up Table** • Convert BITMAP pixels to RGB • Inverse gamma correction **Scaler Polyphase Filters*** • Up-sample or Down-sample the pixels • Anti-aliasing Reduction • Chrominance Resampling **Luma Key** Make pixels whose luminance falls under a certain range transparent. The video-lite pipeline does not have scaler filters, but has dedicated Chrominance Upsamplers.

Table 1-1. DSS Components Overview (continued)

Component Name	Description	Supported Features
Overlay (OVL) Manager	Compositing selected input layers together to generate the final display output frame.	**Note**: OVL Managers only accepts RGB formats for inputs and outputs in RGB formats. **Programmable Background Color** DSS is capable of writing a solid color in the background image. **Composition** Composite multiple layers (VID and/or VIDL) on top of the background color **Transparency Color Key** Source color transparency: Top layer pixel that meets the source transparency color check is made transparent. Destination color transparency: Top layer pixel is made transparent, only if the bottom layer pixel does not meet the destination transparency color check. **Alpha Blending** Global alpha and per pixel alpha modes supported. **Z ordering** Determines the order in which the selected layers are blended. **Color Bar Test** Ability to generate a color bar pattern for testing.
Video Port (VP)	Receives the final frame as input from Overlay Managers and generates video signals	**Output Format** • RGB – RGB-444/565/666/888 • YUV – BT.1120 and BT.656 Modes **Color Space Conversion / Color Phase Rotation** • Converts pixels from RGB color-space to YUV color-space. • Change the phases of the RGB output to either GBR or BRG. **Temporal Dithering** Minimizes the color banding when displaying the data on an LCD panel with color-depth lower than 24-bits. **Multiple Cycle Output Format (using TDM)** Pixels are transmitted on a lesser number of video-output lines in 1 to 3 cycles.
Safety	For safety critical system applications, DSS supports various safety features in hardware.	**Data correctness check** To verify intended data is shown correctly on the display. **Freeze frame detection** To notify a possible frame freeze, when there is no change in the display frame over multiple frame periods.

Table 1-1 lists a high level overview of the various features. For more details, see the DSS chapter in the TRM.

1.2 PLL and Output Routing with DSS

As shown in Figure 1-2, AM62P features two DSS controllers and three PLLs and the device can drive up to three displays simultaneously. To drive a specific interface, users must configure the DSS Video Port (VP) and the PLLs correctly to achieve the desired output. This application note summarizes the correct configuration for VP and PLL.

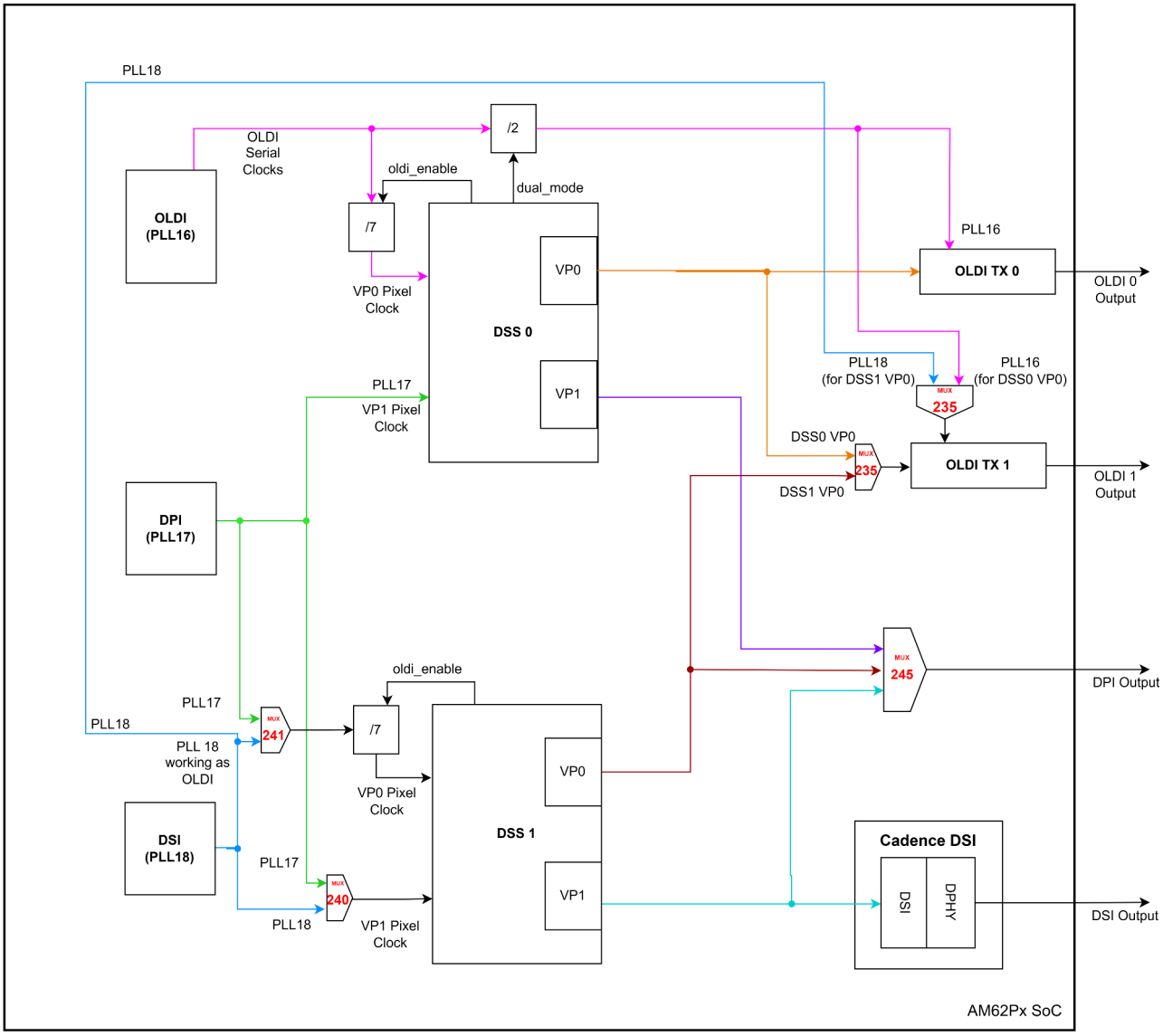

Figure 1-2. DSS to Output Routing

2 Configuring Individual Displays

2.1 Configuring OLDI

There are five possible ways of driving OLDI and the OLDI is controlled by Mux 235.

1. Single-Link OLDI controlled by DSS0 VP0 operating at maximum 165MHz pixel clock.
2. Single-Link OLDI controlled by DSS1 VP0 operating at maximum 100MHz pixel clock.
3. Two independent single-link OLDI, one controlled by DSS0 VP0 operating at maximum 165MHz pixel clock and other controlled by DSS1 VP0 operating at maximum. 100MHz pixel clock.
4. Two cloned single-link OLDI, both controlled by DSS0 VP0 operating at maximum 165MHz pixel clock.
5. Dual-link OLDI controlled by DSS0 VP0 operating at maximum 300MHz pixel clock.

Table 2-1. OLDI Configurations

Display Interface	DSS VP Config				PLL Config			Max. Pixel Frequency	MUX	Summary
	DSS0 VP0	DSS0 VP1	DSS1 VP0	DSS1 VP1	PLL16	PLL17	PLL18			
OLDI(SL) [OLDI TX0]	✓				✓			165MHz	N/A	
OLDI(SL) [OLDI TX1]			✓				✓	100MHz	Mux 235	Mux 235 controls the OLDI1 Input and PLL Clock. Value of 0 means DSS0 VP0 + PLL16 and Value of 1 means DSS1 VP0 + PLL 18. For more information, see CFG0_OLDI1_CLKSEL in the TRM
2x OLDI(SL) [OLDI TX0 & OLDI TX1]	✓		✓		✓		✓	165MHZ and 100MHZ	Mux 235	Mux 235 controls the OLDI1 Input and PLL Clock. Value of 0 means DSS0 VP0 + PLL16 and Value of 1 means DSS1 VP0 + PLL 18. For more information, see the CFG0_OLDI1_CLKSEL in TRM
Clone Mode [OLDI TX0 and OLDI TX1]	✓				✓			165MHz	N/A	Do not need to configure other DSS and drives the DSS
OLDI(DL) [OLDI TX0 and OLDI TX1]	✓				✓			300MHz	N/A	

2.2 Configuring DPI

There are three possible ways of driving DPI and all operating at maximum 165MHx pixel clock using multiple mux configurations.

1. Using DSS0 VP1
2. Using DSS1 VP0
3. Using DSS1 VP1

For more information, please see CFG0_DPI0_OUT_SEL.

Table 2-2. DPI Configurations

Display Interface	DSS VP Config				PLL Config			Max. Pixel Frequency	Mux	Summary
	DSS0 VP0	DSS0 VP1	DSS1 VP0	DSS1 VP1	PLL 16	PLL 17	PLL 18			
DPI		✓				✓		165MHz	N/A	
			✓			✓		165MHz	Mux 241and Mux 245	Mux 241: Select 1 -> PLL17 For more information, please refer to: CFG0_DSS1_DISPC0_CLKSEL(bit16) Mux 245: Select 1 -> DSS1 VP0 For more information, see CFG0_DPI0_OUT_SEL
				✓		✓		165MHz	Mux 240 and Mux 245	Mux 240: Select 1 -> PLL17 For more information, please refer to: CFG0_DSS1_DISPC0_CLKSEL (BIT18) Mux 245: Select 2-> DSS1 VP1 For more information, see: CFG0_DPI0_OUT_SEL

2.3 Configuring DSI

There are 2 possible ways of driving DSI controlled by Mux 240

1. Using PLL 18 at maximum 300MHz pixel clock.
2. Using PLL 17 at maximum 165MHz pixel clock.

Display Interface	DSS VP Config				PLL Config			Maximum Pixel Frequency	Mux	Summary
	DSS0 VP0	DSS0 VP1	DSS1 VP0	DSS1 VP1	PLL 16	PLL 17	PLL 18			
DSI				✓			✓	300MHz	N/A	
				✓		✓		165MHz	Mux 240	Mux 240: Select 1 -> PLL 17. For more information, see CFG0_DSS1_DISPC0_CLKSEL(bit18)

3 Configuring Simultaneous Displays

Table 3-1 lists various VP and PLL configs if multiple displays are being used simultaneously.

Table 3-1. Configuring Simultaneous Displays

Display 1 (PLL 16)		Display 2 (PLL 17)		Display 3 (PLL 18)		Summary
Output	Source	Output	Source	Output	Source	
OLDI (DL) [or] OLDI(SL) clone [or] OLDI0 (SL)	DSS0 VP0	DPI	DSS0 VP1 [or] DSS1 VP0	DSI	DSS1 VP1	3x Displays running in Parallel
OLDI0 (SL)	DSS0 VP0	DPI	DSS0 VP1 [or] DSS1 VP1	OLDI1 (SL)	DSS1 VP0	
OLDI0 (SL)	DSS0 VP0	DSI	DSS1 VP1	OLDI1 (SL)	DSS1 VP0	
OLDI (DL) [or] OLDI(SL) clone [or] OLDI0 (SL)	DSS0 VP0	DPI	DSS0 VP1 [or] DSS1 VP0 [or] DSS1 VP1	-	-	2x Displays running in Parallel
OLDI (DL) [or] OLDI(SL) clone [or] OLDI0 (SL)	DSS0 VP0	-	-	DSI	DSS1 VP1	
OLDI0 (SL)	DSS0 VP0	-	-	OLDI1 (SL)	DSS1 VP0	
-	-	DPI	DSS0 VP1 [or] DSS1 VP1	OLDI1 (SL)	DSS1 VP0	
-	-	DSI	DSS1 VP1	OLDI1 (SL)	DSS1 VP0	
-	-	DPI	DSS0 VP1 [or] DSS1 VP0	DSS	DSS1 VP1	

4 Software Configuration

4.1 OLDI (Dual Link)

Use the following dts overlay (.dtso) to enable dual link OLDI. The code is also available at: Texas Instruments kernel source page.

```
// SPDX-License-Identifier: GPL-2.0-or-later OR MIT
/**
 * Microtips integrated OLDI panel (MF-101HIEBCAF0) and touch DT overlay for AM62P5-SK
 *
 * Panel data sheet: https://simplespec.microtipsusa.com/uploads/spec/datasheetFile/
2588/13-101HIEBCAF0-S_V1.1_20221104.pdf
 *
 * Copyright (C) 2024 Texas Instruments Incorporated - http://www.ti.com/
 */

/dts-v1/;
/plugin/;

#include <dt-bindings/gpio/gpio.h>
#include <dt-bindings/interrupt-controller/irq.h>

&{/} {
    display {
        compatible = "microtips,mf-101hiebcaf0", "panel-simple";

        /*
        * Note that the OLDI TX 0 transmits the odd set of pixels
        * while the OLDI TX 1 transmits the even set. This is a
        * fixed configuration in the IP integration and is not
        * changeable. The properties, "dual-lvds-odd-pixels" and
        * "dual-lvds-even-pixels" have been used to merely
        * identify if a Dual Link configuration is required.
        * Swapping them will cause an error in the dss oldi driver.
        */
        ports {
            #address-cells = <1>;
            #size-cells = <0>;

            port@0 {
                reg = <0>;
                dual-lvds-odd-pixels;

                lcd_in0: endpoint {
                    remote-endpoint = <&oldi0_dss0_out>;
                };
            };

            port@1 {
                reg = <1>;
                dual-lvds-even-pixels;

                lcd_in1: endpoint {
                    remote-endpoint = <&oldi1_dss0_out>;
                };
            };
        };
    };
};

&dss0 {
    status = "okay";
};

&oldi0_dss0 {
    status = "okay";
    ti,companion-oldi = <&oldi1_dss0>;
};

&oldi1_dss0 {
    status = "okay";
    ti,secondary-oldi;
};

&oldi0_dss0_ports {
```

```
    #address-cells = <1>;
    #size-cells = <0>;

    port@0 {
        reg = <0>;

        oldi0_dss0_in: endpoint {
            remote-endpoint = <&dss0_dpi0_out0>;
        };
    };

    port@1 {
        reg = <1>;

        oldi0_dss0_out: endpoint {
            remote-endpoint = <&lcd_in0>;
        };
    };
};

&oldi1_dss0_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    port@0 {
        reg = <0>;

        oldi1_dss0_in: endpoint {
            remote-endpoint = <&dss0_dpi0_out1>;
        };
    };

    port@1 {
        reg = <1>;

        oldi1_dss0_out: endpoint {
            remote-endpoint = <&lcd_in1>;
        };
    };
};

&dss0_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    /* VP1: Output to OLDI */
    port@0 {
        reg = <0>;
        #address-cells = <1>;
        #size-cells = <0>;

        dss0_dpi0_out0: endpoint@0 {
            reg = <0>;
            remote-endpoint = <&oldi0_dss0_in>;
        };

        dss0_dpi0_out1: endpoint@1 {
            reg = <1>;
            remote-endpoint = <&oldi1_dss0_in>;
        };
    };
};

&main_i2c0 {
    #address-cells = <1>;
    #size-cells = <0>;

    touchscreen@41 {
        compatible = "ilitek,ili251x";
        reg = <0x41>;
        interrupt-parent = <&exp1>;
        interrupts = <0 IRQ_TYPE_EDGE_FALLING>;
        reset-gpios = <&exp2 20 GPIO_ACTIVE_LOW>;
    };
};
```

1. Every LCD vendor has a unique timing parameter and for Microtips LCD. A compatible field is defined in the DTS file as shown above. The compatible field maps to a file called panel-simple.c and the field is located

under the Kernel directory *drivers/gpu/drm/panel*. In the panel-simple.c file, the timing parameter is defined by SK-LCD1 vendor.
2. For dual link OLDI, use dss0 to drive the video signals to both OLDI TX0 and OLDI TX1. In dual link mode, both olditx IPs are enabled, and as a result, use two endpoints under dss0 vp0.
3. There is a display node and within the display node, there are two ports (port@0 and port@1).
4. The flags *dual-lvds-odd-pixels* and *dual-lvds-even-pixels* identify that the panel that is configured is Dual link OLDI panel.
5. SK-LCD1 has touch IC integrated and communicates on bus address 0x41. Based on custom hardware designs, users must change the I2C bus, interrupt and reset-gpio signals.
6. For more information on the DT, see Texas Instruments kernel source page for AM625 and Texas Instrument's kernel source page for AM65x.

4.2 OLDI (Single Link - Cloned Mode)

Use the following example dts overlay (.dtso) to enable single link OLDI in cloned mode. The code is also available Beyond SDK github page.

```
// SPDX-License-Identifier: GPL-2.0-or-later OR MIT
/**
 * Rocktech Panel (single-link lvds) with AM62P-SK EVM in cloned mode
 *
 * AM62P-SKEVM: https://www.ti.com/tool/SK-AM62P-LP
 *
 * Copyright (C) 2024 Texas Instruments Incorporated - http://www.ti.com/
 */

/dts-v1/;
/plugin/;

#include <dt-bindings/gpio/gpio.h>
#include <dt-bindings/interrupt-controller/irq.h>

&{/} {
    display0 {
        compatible = "rocktech,rk101ii01d-ct", "panel-simple";
        port {
            lcd0_in: endpoint {
                remote-endpoint = <&oldi0_dss0_out>;
            };
        };
    };

    display1 {
        compatible = "rocktech,rk101ii01d-ct", "panel-simple";
        port {
            lcd1_in: endpoint {
                remote-endpoint = <&oldi1_dss0_out>;
            };
        };
    };
};

&dss0 {
    status = "okay";
};

&oldi0_dss0 {
    status = "okay";
    ti,companion-oldi = <&oldi1_dss0>;
};

&oldi1_dss0 {
    status = "okay";
    ti,secondary-oldi;
};

&oldi0_dss0_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    port@0 {
        reg = <0>;
        oldi0_dss0_in: endpoint {
```

```
            remote-endpoint = <&dss0_dpi0_out0>;
        };
    };

    port@1 {
        reg = <1>;
        oldi0_dss0_out: endpoint {
            remote-endpoint = <&lcd0_in>;
        };
    };
};

&oldi1_dss0_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    port@0 {
        reg = <0>;
        oldi1_dss0_in: endpoint {
            remote-endpoint = <&dss0_dpi0_out1>;
        };
    };

    port@1 {
        reg = <1>;
        oldi1_dss0_out: endpoint {
            remote-endpoint = <&lcd1_in>;
        };
    };
};

&dss0_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    /* VP1: Output to OLDI */
    port@0 {
        reg = <0>;
        #address-cells = <1>;
        #size-cells = <0>;

        dss0_dpi0_out0: endpoint@0 {
            reg = <0>;
            remote-endpoint = <&oldi0_dss0_in>;
        };
        dss0_dpi0_out1: endpoint@1 {
            reg = <1>;
            remote-endpoint = <&oldi1_dss0_in>;
        };
    };
};
```

- Every LCD vendor has a unique timing parameter and for (an example) Rocktech LCD, a compatible field is defined in the DTS file as shown above. The compatible field maps to a file called panel-simple.c. The file is located under the Kernel directory *drivers/gpu/drm/panel*. In the panel-simple.c file, the timing parameter is defined by SK-LCD1 vendor.
- For single link OLDI in cloned mode, use dss0 drives the video signals to both OLDI TX0 and OLDI TX1. In cloned mode, both olditx IPs are enabled and as a result, there are two endpoints under dss0 vp0.
- What differentiates this mode from OLDI (Dual Link) mode is the abscence of *dual-lvds-odd-pixels* and *dual-lvds-even-pixels*, while retaining the companion node, which enforces Single Link Cloned mode.
- There are two separate display nodes and each of them has a single port (port@0).

4.3 OLDI (Single Link - Independent Mode)

Use the following example dts overlay (.dtso) to enable 2x single link OLDI in independent mode. The code is also available at Beyond SDK Github.

```
// SPDX-License-Identifier: GPL-2.0-or-later OR MIT
/**
 * Rocktech Panel (single-link lvds) with AM62P-SK EVM in independent mode
 *
 * AM62P-SKEVM: https://www.ti.com/tool/SK-AM62P-LP
 *
 * Copyright (C) 2024 Texas Instruments Incorporated - http://www.ti.com/
 */

/dts-v1/;
/plugin/;

#include <dt-bindings/gpio/gpio.h>
#include <dt-bindings/interrupt-controller/irq.h>

&{/} {
    display0 {
        compatible = "rocktech,rk101ii01d-ct", "panel-simple";

        port {
            lcd0_in: endpoint {
                remote-endpoint = <&oldi0_dss0_out>;
            };
        };
    };

    display1 {
                compatible = "rocktech,rk101ii01d-ct", "panel-simple";

        port {
            lcd1_in: endpoint {
                remote-endpoint = <&oldi1_dss1_out>;
            };
        };
    };
};

&dss0 {
    status = "okay";
};

&dss1 {
    status = "okay";
    assigned-clocks = <&k3_clks 235 7>,
                      <&k3_clks 241 0>;
    assigned-clock-parents = <&k3_clks 235 9>, /* OLDI TX1 driven by PLL18 and DSS1 VP0 */
                             <&k3_clks 241 1>;  /* PLL18 for DSS1 VP0 */
};

&oldi0_dss0 {
    status = "okay";
};

&oldi1_dss1 {
    status = "okay";
};

&oldi0_dss0_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    port@0 {
        reg = <0>;

        oldi0_dss0_in: endpoint {
            remote-endpoint = <&dss0_dpi0_out0>;
        };
    };

    port@1 {
        reg = <1>;
```

```
        oldi0_dss0_out: endpoint {
            remote-endpoint = <&lcd0_in>;
        };
    };
};

&oldi1_dss1_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    port@0 {
        reg = <0>;

        oldi1_dss1_in: endpoint {
            remote-endpoint = <&dss1_dpi0_out1>;
        };
    };

    port@1 {
        reg = <1>;

        oldi1_dss1_out: endpoint {
            remote-endpoint = <&lcd1_in>;
        };
    };
};

&dss0_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    /* DSS0 VP1: Output to OLDI0 */
    port@0 {
        reg = <0>;

        dss0_dpi0_out0: endpoint {
            remote-endpoint = <&oldi0_dss0_in>;
        };
    };
};

&dss1_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    /* DSS1 VP1: Output to OLDI1 */
    port@0 {
        reg = <0>;

        dss1_dpi0_out1: endpoint {
            remote-endpoint = <&oldi1_dss1_in>;
        };
    };
};
```

'

- Every LCD vendor has a unique timing parameter and for (an example) Rocktech LCD, a compatible field is defined in the DTS file as shown above. The compatible field maps to a file called panel-simple.c and is located under the Kernel directory *drivers/gpu/drm/panel*. In panel-simple.c file, the timing parameter is defined by the SK-LCD1 vendor.
- For single link OLDI in independent mode, use dss0 and dss1 to drive OLDI TX0 and OLDI TX1 separately. In independent mode, both olditx IPs are enabled, but one endpoint under dss0 vp0 and other is under dss0 vp1.
- For information on MUX configuration, see TISCI documents for AM62P.
- This mode is differentiated from OLDI (Single Link - cloned mode) mode because of the the absence of companion node which couple OLDI TX0 and OLDI TX1.
- There are two separate display nodes and each of them has a single port (port@0).

4.4 DPI / HDMI

1. On TI SK-AM62P EVMs, an external-to-SoC Sii902x HDMI bridge is interfaced at DPI output to convert DPI signals to HDMI. Relevant DPI and bridge integration DTS code can be found at Texas Instruments' kernel source page.
2. For a custom board, if HDMI is not needed (directly DPI is required), then remove the sii902x bridge nodes from the above dts file and interface the relevant dss<x> vp<y> to your DPI_in.

```
hdmi0: connector-hdmi {
        compatible = "hdmi-connector";
        label = "hdmi";
        type = "a";
        port {
            hdmi_connector_in: endpoint {
                remote-endpoint = <&sii9022_out>;
            };
        };
    };
:
:
sii9022: bridge-hdmi@3b {
        compatible = "sil,sii9022";
        reg = <0x3b>;
        interrupt-parent = <&exp1>;
        interrupts = <16 IRQ_TYPE_EDGE_FALLING>;
        #sound-dai-cells = <0>;
        sil,i2s-data-lanes = < 0 >;

        hdmi_tx_ports: ports {
            #address-cells = <1>;
            #size-cells = <0>;

            /*
             * HDMI can be serviced with 3 potential VPs -
             * (DSS0 VP1 / DSS1 VP0 / DSS1 VP1).
             * For now, service with DSS0 VP1.
             */
            port@0 {
                reg = <0>;

                sii9022_in: endpoint {
                    remote-endpoint = <&dss0_dpi1_out>;
                };
            };

            port@1 {
                reg = <1>;

                sii9022_out: endpoint {
                    remote-endpoint = <&hdmi_connector_in>;
                };
            };
        };
    };
:
:
&dss0_ports {
    /* DSS0-VP2: DPI/HDMI Output */
    hdmi0_dss: port@1 {
        reg = <1>;

        dss0_dpi1_out: endpoint {
            remote-endpoint = <&sii9022_in>;
        };
    };
};
```

3. To drive DPI/HDMI from another DSS/VP, change the clock MUXes in accordance to possible configurations shown at Configuring DPI. See TISCI document for AM62P for more information.

4.5 DSI

Use the following example dts overlay (.dtso) to enable DSI. The code is also available Texas Instruments' kernel source page.

```
// SPDX-License-Identifier: GPL-2.0-or-later OR MIT
/**
 * DT Overlay for RPi 7inch touchscreen panel interfaced with DSI on
 * AM62P5-SK EVM.
 *
 * RPi DSI Panel: https://www.raspberrypi.com/products/raspberry-pi-touch-display/
 *
 * Copyright (C) 2024 Texas Instruments Incorporated - https://www.ti.com/
 */

/dts-v1/;
/plugin/;

#include <dt-bindings/gpio/gpio.h>
#include <dt-bindings/interrupt-controller/irq.h>

#include "k3-pinctrl.h"

&{/} {
    panel0 {
        compatible = "raspberrypi,7inch-dsi", "simple-panel";
        backlight = <&display_reg>;
        power-supply = <&display_reg>;

        port {

            panel_in: endpoint {
                remote-endpoint = <&panel_bridge_out>;
            };
        };
    };

    bridge_reg: bridge-regulator {
        compatible = "regulator-fixed";
        regulator-name = "bridge-reg";
        gpio = <&display_reg 0 0>;
        vin-supply = <&display_reg>;
        enable-active-high;
    };
};

&dphy_tx0 {
    status = "okay";
};

&main_i2c0 {
    #address-cells = <1>;
    #size-cells = <0>;

    display_reg: regulator@45 {
        compatible = "raspberrypi,7inch-touchscreen-panel-regulator";
        reg = <0x45>;
        gpio-controller;
        #gpio-cells = <2>;
    };
};

&dss1 {
    status = "okay";
};

&dss1_ports {
    #address-cells = <1>;
    #size-cells = <0>;

    /* DSS1-VP1: DSI Output */
    port@1 {
        reg = <1>;

        dss1_dpi1_out: endpoint {
            remote-endpoint = <&dsi0_in>;
        };
```

```
    };
};

&dsi0 {
    status = "okay";
    #address-cells = <1>;
    #size-cells = <0>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        port@0 {
            reg = <0>;

            dsi0_out: endpoint {
                remote-endpoint = <&panel_bridge_in>;
            };
        };

        port@1 {
            reg = <1>;

            dsi0_in: endpoint {
                remote-endpoint = <&dss1_dpi1_out>;
            };
        };
    };

    bridge@0 {
        status = "okay";
        compatible = "toshiba,tc358762";
        reg = <0>;
        vddc-supply = <&bridge_reg>;

        ports {
            #address-cells = <1>;
            #size-cells = <0>;

            port@0 {
                reg = <0>;

                panel_bridge_in: endpoint {
                    remote-endpoint = <&dsi0_out>;
                };
            };

            port@1 {
                reg = <1>;

                panel_bridge_out: endpoint {
                    remote-endpoint = <&panel_in>;
                };
            };
        };
    };
};
```

- The DSI output is derived through a Cadence DSI/DPHY bridge interfaced with the DPI output from DSS1 VP1. Details about this bridge driver is located at Texas Instruments' kernel source page. This bridge is internal to the SoC.
- The DSI output is connected to the DSI_in of the Raspberry Pi DSI panel,which uses a Toshiba bridge internally to convert DSI to DPI. Implement the driver in the same dtso. See Texas Instruments' kernel source page for additional documentation.

5 Summary

This application note serves as a technical guide for configuring the display subsystem of the system, providing engineers with the required guidelines to drive one or more display panels simultaneously.

The document details the operational modes and performance capabilities for the three primary display interfaces. The document explains how each interface can be set up in various ways, offering a different balance between support for high-resolution screens and the ability to run multiple displays.

A key focus of this application note is to clarify the rules and limitations when using several displays at the same time. The document highlights different permutations of DSS-specific resource allocation, making sure designers can make informed choices to achieve a stable and functional multidisplay setup that meets application specific requirements.

For getting help in debugging display-related issues, see this Debug Guide and then post queries on e2e.ti.com if the issue still persists.

6 References

- Texas Instruments, *AM62P*, product folder.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265