Application Note

Robust and Simple TCM Totem Pole PFC Control Using C2000 and GaN

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ABSTRACT

To maximize efficiency and power density, there is a trend with using triangular current mode (TCM) totem pole PFCs with GaN to push for high switching frequency in power design. However, there are also challenges in the software control logic and the hardware circuit design. This application note discusses how to design robust PWM control logic with C2000™ microcontrollers and simplify the hardware circuits with the intelligent features of TI GaN.

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Trademarks

1 Introduction

Requirements for PFCs have undergone considerable changes over the last few years due to increasing demands for smaller size and higher efficiency. The challenge to meet premium levels of 80 plus standards requires very high efficiency over wide operating input and output ranges. This requirement for high efficiency has generated considerable interest in bridgeless topologies for the PFC stage (including totem pole PFC) that can push efficiency above 99%. Compared with hard switching control, a TCM totem pole PFC is increasingly popular due to the merits of zero-voltage switching (ZVS). With the addition of a gallium nitride (GaN) high electron mobility transistor (HEMT), the switching frequency of the TCM totem pole PFC can be pushed to MHz. To optimize system performance, TI also released intelligent GaN with integrated zero crossing detection (ZCD) functions to help reduce BOM cost and simplify software control.

This paper discusses how to leverage advanced features of the C2000 microcontroller (MCU) and the ZCD features of TI GaN to achieve robust and simple software control and system design, including techniques on how to implement interleaving control.

2 Potential Risks with Traditional PWM Configuration

Figure 2-1 shows a basic totem pole PFC structure. In *Optimized Control Schemes for Totem Pole PFC with Digital Controller*, the document discusses the control configurations for the continuous-conduction mode (CCM) control with fixed switching frequency. TCM control requires more complicated logic design for variable switching frequencies.

To achieve ZVS to improve power efficiency, the TCM totem pole PFC relies on an inductor current zero crossing event to implement cycle by cycle control. Normally, external ZCD circuits are required for the inductor current. For a single phase totem pole PFC as shown in Figure 2-1, the high frequency FETs (Q1 and Q2) alternately work as a PFC active FET or sync FET, while slow frequency FETs (Q3 and Q4) switch at grid frequency.

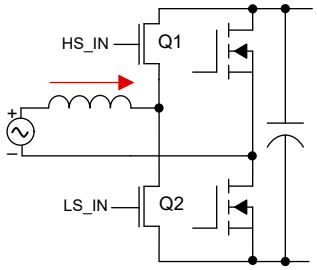

Figure 2-1. Totem Pole PFC Structure

Figure 2-2 shows a common PWM configuration logic with C2000 as an example of positive cycle operation. When the AC input voltage is high (specifically if the input voltage larger than half of the PFC output voltage), generating extra negative inductor current so that switch node voltage discharges to 0V is required to achieve ZVS. According to Figure 2-2, several key configurations are summarized in the following steps.

1. ZCD signal (rising edge) is used to generate the synchronized event to reset the PWM counter.
2. Action qualifier (AQ) submodule setting:
   a. PWM for active FET: set high at CTR results in a zero event. Clear low at CTR results in a CMPA event.
   b. PWM for sync FET: set high at CTR results in a CMPB event. Clear low at CTR results in a zero event
3. Dead band (DB) submodule setting:
   a. Enable the rising edge delay for the active FET PWM and the falling edge delay for the sync FET PWM.

With the configurations shown, the two dead times between the active FET and the sync FET must be defined carefully, which means that the rising edge delay value must be always larger than the falling edge delay value, and the CMPB value must be always larger than the CMPA value. During normal operation, the duration of the negative current is controlled by the rising edge delay value, while the duty cycle is calculated by the CMPA value. These four registers are required to calculate and change in every control loop processing cycle. Updating all the registers at the same time is critical. Otherwise, this can cause disastrous short circuit issues during the power stage.

Theoretically, the global load and one-shot load scheme in the Type-4 EPWM are designed to make sure multiple PWM registers update at the same global event. However, when the register update frequency (which is normally the same as the control loop ISR frequency) is higher than the switching frequency, asynchronous update risks for multiple PWM registers can occur. The detailed root cause and workarounds can be found in *Handling PWM Challenges in Resonant Converters*. However, the current workarounds do not apply for the TCM totem pole PFC control, since it is required to determine when to update the registers based on the present switching period. Since the switching period is decided by the hardware events for TCM control, the switching periods are unable to be predicted in advance.

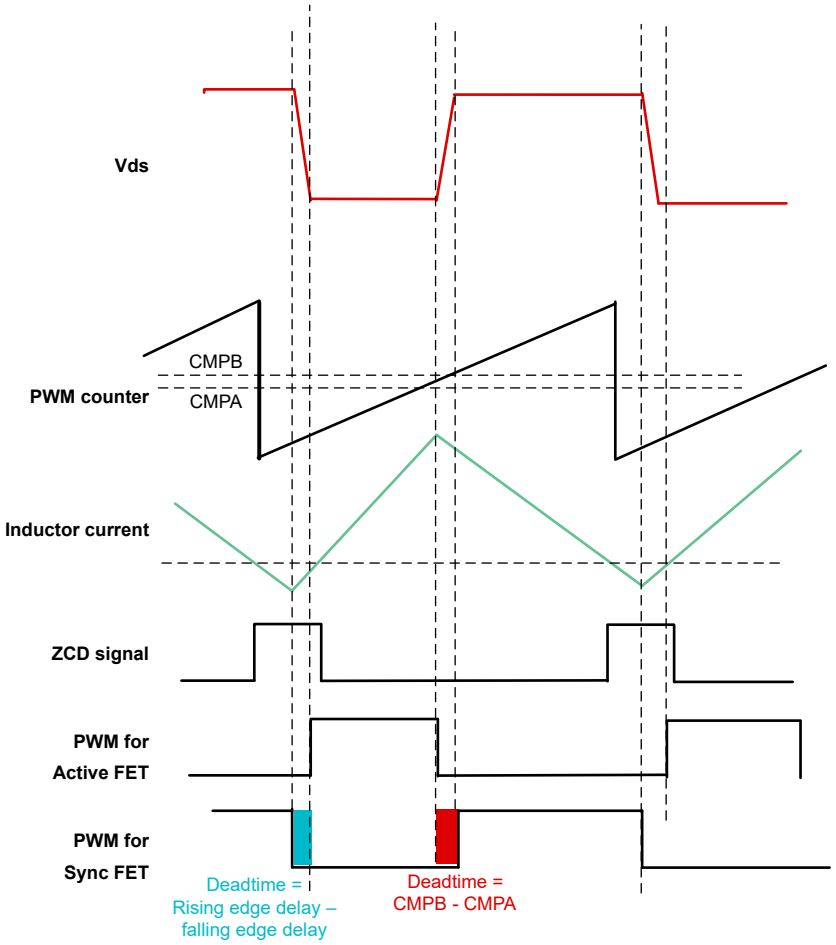

Figure 2-2. Common PWM Configuration Logic

3 PWM Configurations for Robust Control

A PWM configuration logic as shown in Figure 3-1 addresses the risks in traditional configurations . Key configurations are highlighted in the following steps:

1. The falling edge of sync FET with additional delay (highlighted in green) is used to reset the PWM counter. This delay represents the dead time of two FETs.
2. AQ submodule setting:
   a. ZCD signal (rising edge) is configured as a T1 event
   b. PWM for active FET: set high at CTR results in a zero event; clear low at CTR results in a CMPA event
   c. PWM for sync FET: set high at CTR results in a CMPA event; clear low at T1 event
3. DB submodule setting:
   a. Enable both rising edge delay and falling edge delay for the sync FET PWM. The rising edge delay represents the dead time of two FETs, while the falling edge delay defines the duration of the negative inductor current.

In this way, the two dead times between active FET and sync FET are decided by a single register separately, which completely avoids shoot through issues because of overlapping registers. Only the falling edge delay and CMPA registers are required to be updated during normal operation.

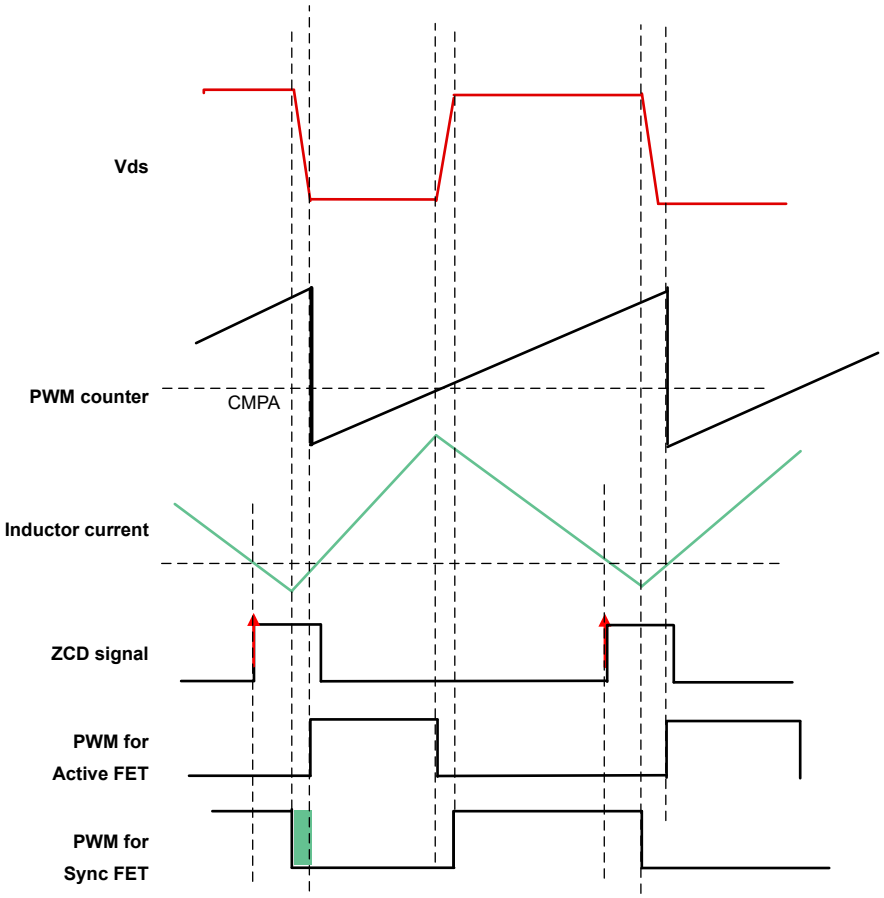

Figure 3-1. PWM Configuration Logic

The following sections describe the details on how to configure the PWM logic.

3.1 Create Additional Delay for the Sync Event for the PWM Counter

The falling edge of sync FET PWM is defined as a DCxEVT1 event (active low), through input XBAR, EPWM XBAR and digital compare (DC) submodule, since a DCxEVT1 event can be used to generate a synchronization event for the PWM counter. Figure 3-2 shows how the edge filter function inside the DC submodule is leveraged to create additional delay for a DCxEVT1 event, as shown in the following steps.

1. Select a DCxEVT1 event as the input to the edge filter block.
2. Enable valley capture mode (VCAPCTL[VCAPE])
3. Select *CTR = Zero* to restart the edge filter (VCAPCTL[TRIGSEL])
4. Configure the edge filter to capture one edge (DCFCTL[EDGECOUNT])
5. Enable the configure for the required delay for the DCxEVT1 signal (SWVDELVAL), which represents the additional delay for the PWM counter sync event.

```
EPWM_setDigitalCompareFilterInput (base, EPWM_DC_WINDOW_SOURCE_DCAEVT1);
EPWM_enableDigitalCompareEdgeFilter(base);
EPWM_enableValleyCapture(base);
EPWM_setValleyTriggerSource(base, EPWM_VALLEY_TRIGGER_EVENT_CNTR_ZERO);
EPWM_setDigitalCompareEdgeFilterEdgeCount(base, EPWM_DC_EDGEFILT_EDGECNT_1);
   EPWM_enableValleyHWDelay(base);
EPWM_setValleySWDelayValue(base, 30);
```

Considering the dead time is relatively stable across operation conditions, it is safe even though the SWVDELVAL register does not operate in shadow mode. Since the active FET and sync FET roles are exchanged under a positive cycle and a negative cycle, the source (sync FET PWM) for the DCxEVT1 event is required to change at the same time. This is accomplished by selecting different GPIOs as the source of the input XBAR.

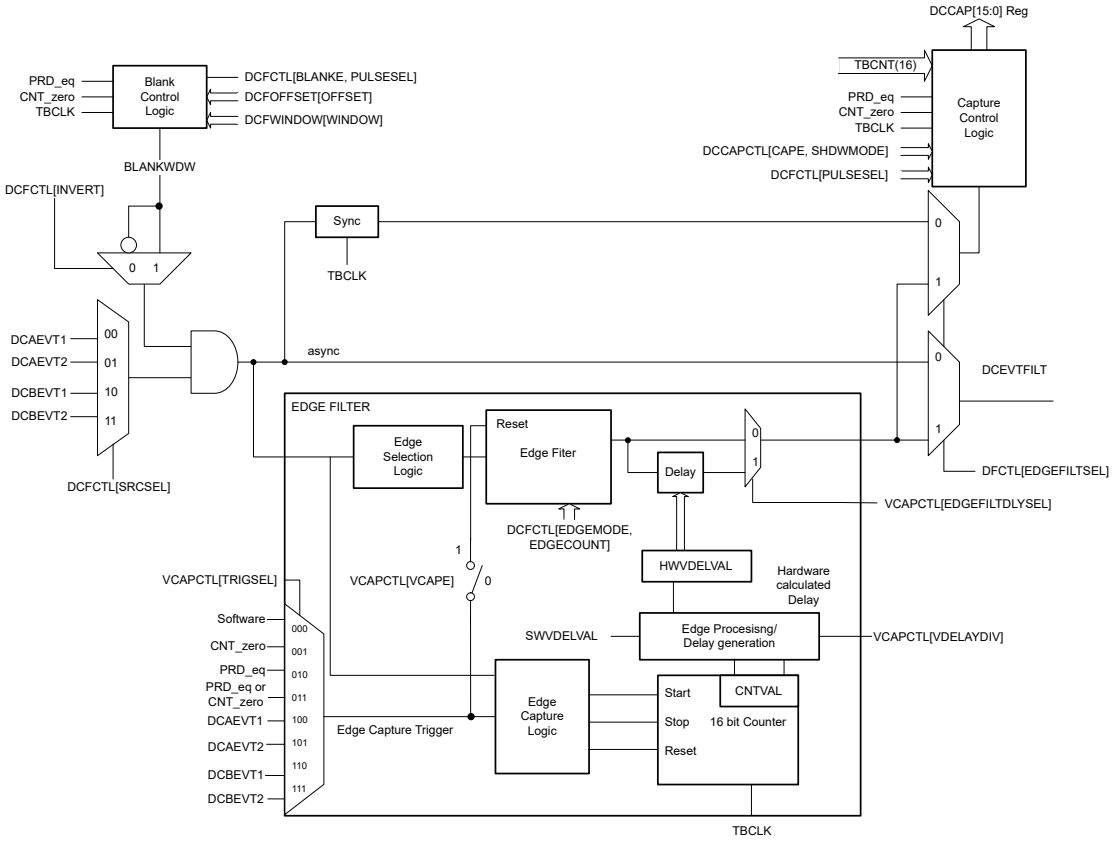

Figure 3-2. Edge Filter Function of the DC Module

3.2 Configure a ZCD Signal as a T1 Event

Figure 3-3 shows additional T1 and T2 events (sourced from comparator, external trip, or sync events) that are added to generate AQ actions in the latest Type 4 ePWM module. For more details regarding new T1 and T2 features, see the corresponding technical reference manual. In this case, the rising edge of the ZCD signal is defined as a DCxEVTy event (active high), through the input XBAR, EPWM XBAR and digital compare (DC) submodule. Next, the DCxEVTy event is selected as the source for a T1 event.

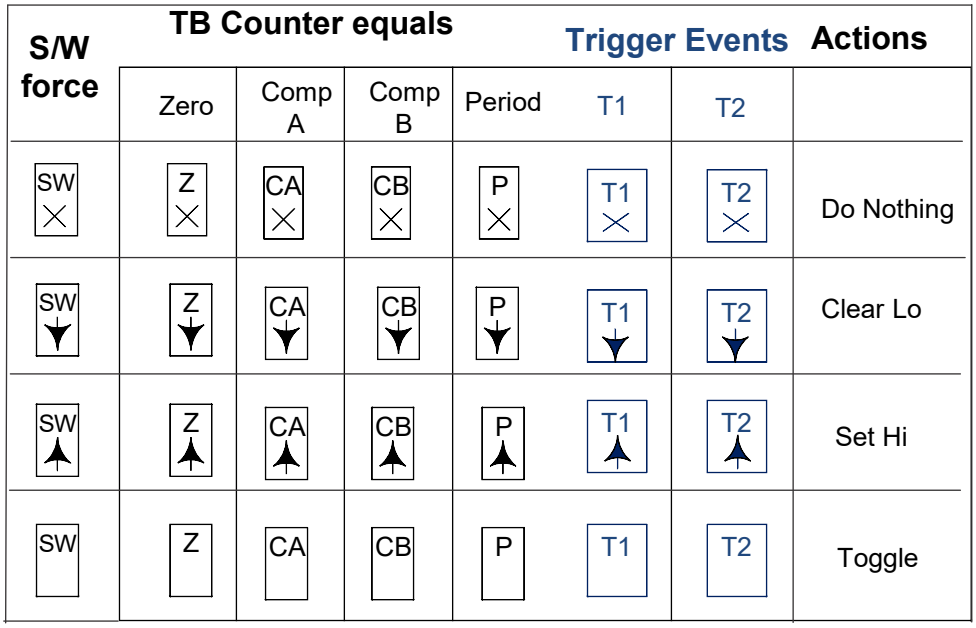

Figure 3-3. Action-Qualifier Actions for ePWMxA and ePWMxB Outputs

4 How to Capture the Phase Difference and Period of Multiphase Totem Pole PFCs

Due to the large current ripple with TCM control mode, a multiphase TCM totem pole PFC is required for high-power applications. Generally, interleaved control has two designs: open-loop control and close-loop control [1]. Since the open-loop control implements a specific ratio of the switching period of the master phase to the slave phase, the control cannot verify if the slave phase is operating in the ZVS condition all the time because of the parameter variations among different phases. For close-loop control, turn-on instances of different phases are decided by the ZCD signals separately to make sure ZVS is operating with better efficiency and stability.

To achieve the expected phase shift relationship, additional logic is required to capture the phase difference among different phases and the period of the master, so that the phase difference can be further adjusted to the expected phase by changing the on-time of the slave phases in order.

Generally, ECAP modules can be used, but two modules are required for two phases, and at least three modules are required for three phases. This is not an efficient method and the amount of ECAP modules is limited for some C2000 devices.

Figure 4-1 shows a simplified design to capture the phase difference and periods of multiphase PWM output simultaneously. An auxiliary PWM output is designed to reflect the two rising edges of the different phase PWM outputs. The auxiliary PWM output actions are controlled by the T1 and T2 events, where the T1 event refers to the rising edge of phase 1 PWM, and the T2 event refers to the rising edge of the phase 2 PWM. In this way, the single capture module is enough to obtain the phase differences (duty cycle of auxiliary PWM) and period, instead of using two modules. In this way, even for three phase interleaved totem pole PFCs, only two capture modules are required.

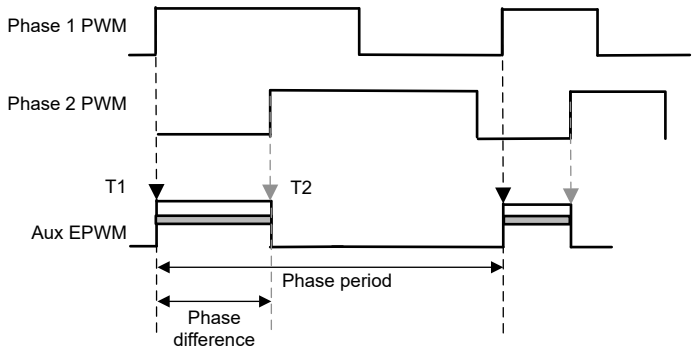

Figure 4-1. New Design to Capture the Phase Difference and Period

5 How to Eliminate the External ZCD Circuits with TI GaN

Figure 5-1 shows a common external ZCD circuits for a TCM totem pole PFC. Generally, this consists of a shunt resistor, a high-bandwidth operational amplifier, and a high speed comparator. When designing a high power system with high switching frequency, it is challenging to balance the detection speed and the noise immunity for the ZCD circuits. Additionally, the shunt resistor causes power loss and affects efficiency.

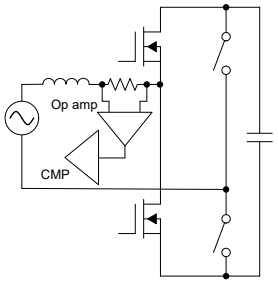

Figure 5-1. External ZCD Circuits

TI released an intelligent GaN (LMG3427R030), which integrates a ZCD signal to simplify the system design, as Figure 5-2 shows.

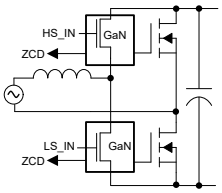

Figure 5-2. GaN with Integrated ZCD for Totem Pole PFC

The device integrates a ZCD circuit that provides a digital feedback signal when the drain-to-source current direction changes from negative to positive, which is different from traditional ZCD signals. To better illustrate how to leverage the ZCD signals from both high side and low side GaN, Figure 5-3 shows the ZCD signal behaviors during a positive cycle and a negative cycle and the corresponding PWM logic. Therefore, different from the usage of traditional single ZCD signals, it is required to switch the source for the ZCD signal in the PWM configurations, since the high side GaN provides the effective ZCD signal for the control during the positive cycle and the low side GaN provides the ZCD signal during the negative cycle. This can be done by changing the GPIO source in the settings of the input XBAR.

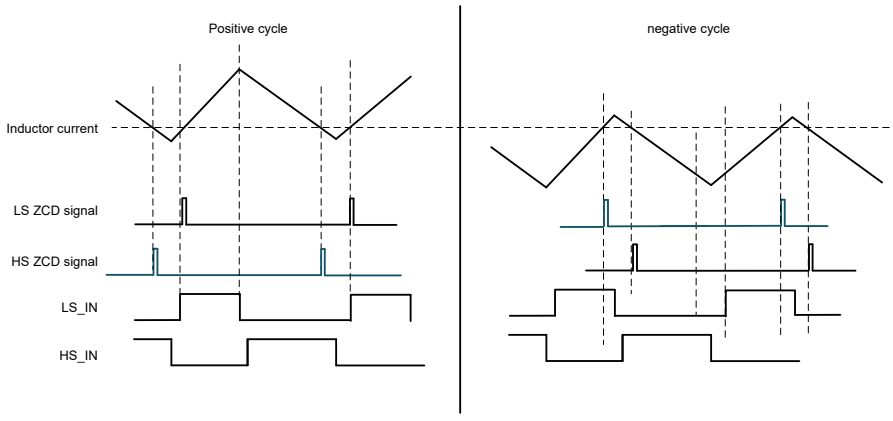

Figure 5-3. GaN ZCD Signal Behaviors During Positive and Negative Cycles

6 Summary

The application note provides new PWM configurations for totem pole PFCs with TCM control to avoid shoot through issues. The document also proposes a simplified scheme to capture the phase difference and period for multiphase topologies. The application note also demonstrates how to leverage GaN with an integrated ZCD signal and related software logic for TCM totem pole PFCs to simplify system design.

7 References

- Ma, Qingxuan, et al. *Digital interleaving control for two-phase tcm gan totem-pole pfc to reduce current distortion*. 2019 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2019.
- Texas Instruments, *TMS320F28003x Real-Time Microcontroller Technical Reference Manual*, technical reference manual.
- Texas Instruments, *Handling PWM Challenges in Resonant Converters*, application note.

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