Application Note

AM26x Custom PCB System Getting Started Guide

ABSTRACT

This document serves as a guide for engineers bringing up custom PCB systems featuring a microcontroller from the TI AM26x product family of high-performance MCUs. Once a custom PCB project utilizing an AM26x device has completed fabrication and assembly, there are a series of basic checks an engineer can perform to verify the proper operation of the PCB system and the AM26x device.

This application note is to be used in conjunction with the AM26x Hardware Design Guidelines application note. Engineers designing an AM26x-based PCB system must make sure the design guidelines are adhered to during the design phase of a custom PCB project. This document is to be used post-fabrication and assembly once PCBs are in hand and ready for bring-up.

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1 Introduction

Upon receiving a fabricated and assembled AM26x-based PCB system, an engineer must visually inspect the board. This inspection must include noting any components with poor solder joints or non-populated components that can cause issues or damage to the PCB at power on.

When bringing up any AM26x-based PCB system for the first time, perform the following steps in this order:

1. Power checks
2. Verify AM26x device boot status
3. Verify AM26x device is alive
4. Verify AM26x JTAG connection
5. Run example code to verify program loading and output

This document details the process to be followed to successfully bring-up an AM26x-based PCB system.

Note

AM26x refers to any of the MCU devices in the AM263x, AM263Px, and AM261x families of high-performance microcontrollers.

2 Power Net Checks

2.1 Verify Proper AM26x Power Rail Voltage Levels

Once the visual inspection is complete and no issues are identified, the PCB is ready for initial power-on. Once powered on, each critical voltage net for the AM26x device must be probed and verified to be within the recommended operating conditions. This is shown in Table 2-1.

Table 2-1. AM26x Power Nets - Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
VDD	SOC VDD Core Supply	R5F = 400MHz	1.140	1.200	1.260	V
		R5F = 500MHz[1]	1.188	1.250	1.320	V
VDDAR1[2], VDDAR2, VDDAR3	SRAM Array Supplies	R5F = 400MHz	1.140	1.200	1.260	V
		R5F = 500MHz[1]				
VDDS18	1.8V IO Bias Supply from Bias LDO routed through board		1.710	1.800	1.890	V
VDDS33	3.3V IO Supply		3.135	3.300	3.465	V
VDDA18_OSC_PLL	1.8V Analog supply for PLL. Routed from the Analog LDO out through board		1.710	1.800	1.890	V
VDDA33	Analog 3.3V Supply		3.135	3.300	3.465	V
VDDA18	1.8V Analog supply. Routed from 1.8V Analog LDO out through Board		1.710	1.800	1.890	V

(1) AM261x devices of 'O' speed grade require 1.25V nominal core voltage regardless of the core frequency settings
(2) AM263x and AM263Px only

2.2 Verify Maximum Current Loading

After probing the AM26x device power nets, this is essential to verify that the maximum current loading on the device core and IO power nets are not being exceeded while the device is in an idle state. If current loading is being exceeded, then there is high risk for damage to the AM26x MCU and system once an application is run on the system. Table 2-2 details the peak power consumption that is not to be exceeded.

Table 2-2. Estimated Peak Power Consumption at 150°C Junction Temperature

Device Supply Name	Nominal Voltage (V)	AM263x Peak Current (mA)	AM263Px Peak Current (mA)	AM261x, R5F = 400MHz Peak Current (mA)		AM261x, R5F = 500MHzPeak Current (mA)(1)		Supply Description
VDD, VDDAR	1.2	**2500**	**2800**	**1750**		**1500**		Digital core power
VDDS33	3.3	**200**	**200**	3.3V IOs Only	**200**	3.3V IOs Only	**200**	3.3V digital I/O power
				1.8V and 3.3V IOs	**120**	1.8V and 3.3V IOs	**120**	
VDDA33	3.3	**100**	**200**	**100**		**100**		3.3V analog I/O power

(1) Power consumption data for R5F = 500MHz is for 125°C junction temperature

2.3 AM26x Power Sequencing

Once the device power nets and current loading have been verified, the power sequencing of the AM26x must be checked using an oscilloscope or a similar electronic test instrument. TI recommends to connect test wires or probe hooks to test points or exposed copper on the PCB to have a secure connection between the oscilloscope and the PCB.

Some key points to consider when verifying the AM26x power sequencing are:

- There is no sequencing requirement with respect to the primary core digital VDD 1.2V and I/O power 3.3V rails
- A pair of on-die LDO are supplied through the VDDS33 power net. These on-die LDOs generate the required VDDS1V8 and VDDA1V8 1.8V digital and analog power
- The minimum ramp time for the 3.3V rail, *tRamp_3V3* must be respected
- Additional PORz and SOP boot mode latch timing must be respected by the PCB design

Note

For Industrial-grade AM261x devices ('O' speed grade), the core voltages VDD and VDDAR are 1.25V

Figure 2-1 shows the AM26x power-on sequencing. Table 2-3 describes the timing shown in Figure 2-1.

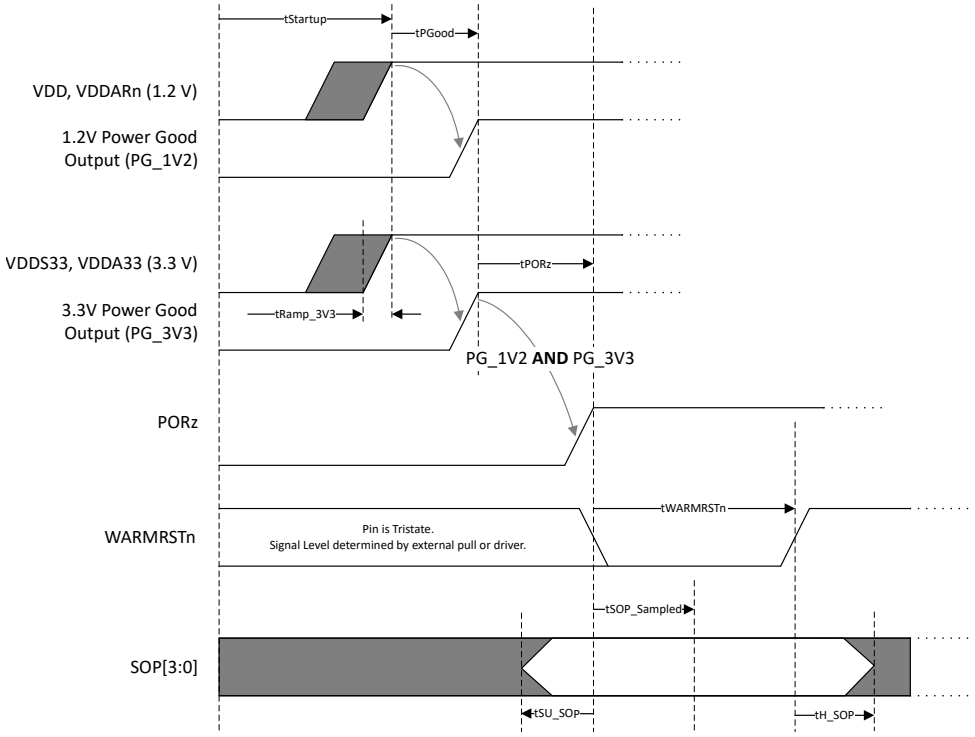

Figure 2-1. AM26x Power-On Sequencing

Table 2-3. AM26x Power-On Sequencing Timing

PARAMETER		MIN	MAX	UNIT
$t_{Startup}$	Time for 1.2V and 3.3V DC-DC converters to start up after being enabled. This is an arbitrary amount of time; no constraint imposed by the device.	–	–	ms
t_{PGood}	Time for Power Good signals to be generated from DC-DC converters after rails are stable. This is an arbitrary amount of time - no constraint imposed by the device.	–	–	ms
t_{Ramp_3V3}	Ramp time of the VDDS3V3 and VDDA3V3 supplies. This is a requirement imposed by the device.	0.1	–	ms
$t_{SOP\_Sampled}$	Time from PORz de-assertion until the SOP[3:0] pins are sampled. This is a device internal pentameter. Sampling happens when the internally generated supplies are stable. For information only. Refer to TSU_SOP and TH_SOP parameters for application usage.	0	–	ms
t_{SU_SOP}	Setup time for SOP relative to PORz assertion.	10	–	µs
t_{H_SOP}	Hold time for SOP relative to WARMRSTn deassertion.	0	–	µs
$t_{WARMRSTn}$	Time from PORz de-assertion until the device deasserts the WARMRESETn signal.	2.0	–	ms

Follow the steps below on the PCB and AM26x to boot the device from power-on reset (PORz):

1. PORz is held low by the external power supply monitor.
2. VDD core digital 1.2V and VDDS3V3/VDDA3V3 3.3V supplies ramp to the nominal voltages.
   a. This requires a logical AND be applied to the power good signal generated from each supply.
3. SOP[3:0] pins held in the boot latch state.
4. After PCB supplied power nets are stable, the external supply monitor deasserts PORz.
5. Device starts up 1.8V on-die LDO.
6. After internal supply monitors show externally and internally generated supplies are stable, the SOP[3:0] pin states are latched.
7. R5F cores are unhalted and SOP selected boot ROM execution begins.

Once the power-on sequencing has been verified, the probes need to remain connected to the PCB to verify the power-down sequencing. Like with the power-on process, the order of power-down on the 1.2V and 3.3V rails do not matter.

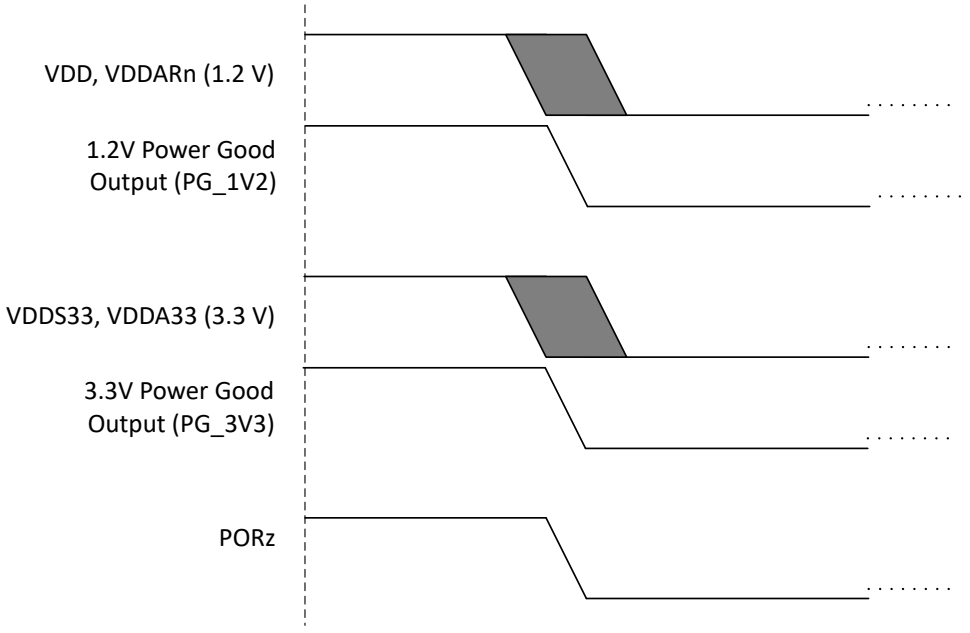

Figure 2-2. Power-Down Sequencing

2.4 AM26x Power Topology References

The AM26x Hardware Design Guidelines application note can be referenced for specific power topologies that are similar to a custom PCB design. The following sections detail AM26x PCB system power topology:

- *Discrete DC-DC Power Solution*
- *Integrated PMIC Power Solution*

3 Device Boot Status

3.1 AM26x SOP Pin Status

AM26x microcontrollers have four SOP (Start-On-Power) pins that configure the device boot mode. Each SOP pin must be held in a valid logic state; 3.3V (1) or GND (0) using external pull resistors. The pin assignments on each AM26x device are shown in Table 3-1.

Table 3-1. SOP and Functional Mode Signal Mapping

SOP Mode Signal	Primary Pinmux Signal	AM26x ZCZ Pin	AM261x ZFG Pin	AM261x ZNC Pin	AM261x ZEJ Pin
SOP[0]	OSPI0/QSPI0_D0	N1	R2	N2	M2
SOP[1]	OSPI0/QSPI_D1	N4	R1	N1	N1
SOP[2]	SPI0_CLK	A11	A13	A12	A12
SOP[3]	SPI0_D0	C10	B12	B12	A10

The boot mode options for each AM26x device are shown in the tables below.

Table 3-2. AM263x Boot Modes

Boot Mode	SOP[3]	SOP[2]	SOP[1]	SOP[0]
QSPI (4S) - Quad Read Mode	0	0	0	0
UART	0	0	0	1
QSPI (1S) - Single Read Mode	0	0	1	0
QSPI (4S) - Quad Read UART Fallback Mode	0	1	0	0
QSPI (1S) - Single Read UART Fallback Mode	0	1	0	1
DevBoot	1	0	1	1
Unsupported Boot Mode	All other combinations not defined above			

Table 3-3. AM263Px Boot Modes

Boot Mode	SOP[3]	SOP[2]	SOP[1]	SOP[0]
QSPI(4S), 50MHz - Quad Read UART Fallback Mode	0	0	0	0
UART	0	0	0	1
QSPI(1S), 50MHz - Single Read UART Fallback Mode	0	0	1	0
OSPI(8S), 50MHz - Octal Read UART Fallback Mode	0	0	1	1
xSPI (1S->8D) , 25MHz, SFDP	1	1	0	0
DevBoot	1	0	1	1
Unsupported Boot Mode	All other combinations not defined above.			

Table 3-4. AM261x Boot Modes

Boot Mode	SOP[3]	SOP[2]	SOP[1]	SOP[0]
OSPI-OSPI (4S), 50MHz - Quad Read UART Fallback Mode	0	0	0	0
UART, XMODEM, 115200bps	0	0	0	1
OSPI-OSPI (1S), 50MHz - Single Read UART Fallback Mode	0	0	1	0
OSPI (8S), SDR, 33MHz - Octal Read UART Fallback Mode	0	0	1	1
DevBoot	1	0	1	1
xSPI (1S->8D), 20MHz, SFDP	1	1	0	0
USB DFU - USB with UART Fallback Mode	1	1	1	0
Unsupported Boot Mode	All other combinations not defined above.			

3.2 SOP Boot Mode Latch Timing

The SOP boot mode latch timing is referenced in Table 2-3. The parameters to take note of are:

- $t_{SOP\_Sampled}$
- t_{SU_SOP}
- t_{H_SOP}
- $t_{WARMRSTn}$

While a requirement is to check as part of power sequencing, this is important to emphasize the criticality of the timing of the SOP boot mode pins latching.

There is an additional way to check the timing of these critical signals. The SOP pins are latched in the internal circuit on the AM26x when the device Power Management Unit (PMU) provides a VDD_OK signal. VDD_OK is generated once all device supplies have ramped up and are stable. The last supply to ramp, and thus trigger VDD_OK is VDDA18, the 1.8V Analog LDO supply. VDDA18 ramps once PORz is released. Therefore, the critical sequence for latching the boot mode pins is:

1. PORz releases, goes high
2. 1.8V Analog LDO (VDDA18) supply ramps
3. VDD_OK signal is triggered
4. SOP pin states are sampled

Although there is no explicit device pin signal available to probe and indicate when the SOP pin states are sampled to latch the AM26x boot mode, the VDDA18 ramp can be monitored to find this point. Once the VDD_OK signal is generated, the AM26x device boots for 2-6ms. The last point of boot is the WARMRSTn signal release, in which the boot mode is latched, SOP pins are not necessary to hold the states, and can now be changed.

3.3 AM26x SOP Pin Isolation

The AM26x SOP signals are on-device pins shared with other digital I/O. Due to the SOP and functional mode multiplexing, additional care needs to be taken in the design phase to make sure that the SOP mode selection resistors, jumpers or switch paths are routed in such a way that the SOP mode branches do not present inductive stubs to the functional mode signal paths. Issues regarding SOP latch timing, functional mode signal integrity or timing issues, especially non-functional OSPI, QSPI or SPI, can be attributed to this, and the PCB layout must be reviewed.

For TI's recommended SOP pin isolation method, reference the *SOP Signal Implementation* section in the AM26x Hardware Design Guidelines application note.

4 Verify UART Output

Once the device boot status is verified and functional, next the device UART output is checked to validate that the device successfully boots.

4.1 Configure AM26x for UART Boot

To check the AM26x UART output, the device must first be placed into UART boot mode.

If the PCB design accounts for a configurable boot mode (that is, through DIP switches), then set the SOP[3:0] switches to 0001. This SOP[3:0] setting for UART boot mode applies for all AM26x devices.

If the PCB design has a fixed boot mode configured by soldered pull resistors, then this is likely that the AM26x is set in a boot mode with UART Fallback. To confirm, see Section 3.1.

Once UART boot mode is set, connect the AM26x PCB system to a host PC using any USB to UART adapter. Make sure that the UART0 instance TX, RX pins are being used to connect to the host PC. TI recommends the XDS110 JTAG Debug Probe, which is supported for use by all AM26x microcontrollers, and is well integrated with the TI software and debug tools.

4.2 Configure Host PC for UART Boot Validation

After connecting the AM26x UART0 interface to the host PC, open the *Device Manager* or similar application to verify that the UART ports are being detected.

Note

If the COM ports are not populating, then the TI XDS Drivers needs to be installed. The XDS Drivers are typically downloaded by default when Code Composer Studio is installed. However, if a different IDE is being used, then the drivers need to be installed separately.

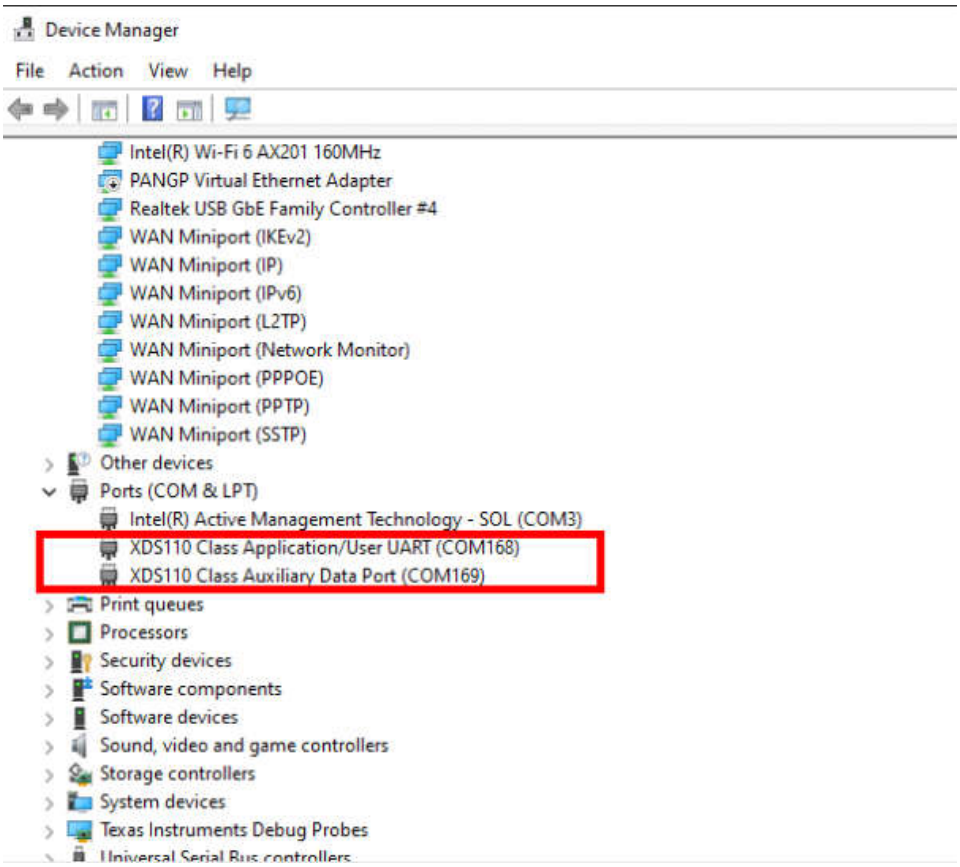

Figure 4-1. AM26x UART Port Detection

Once verified, open a UART terminal application, such as Tera Term.

In the Tera Term window, select *Setup* → *Serial Port*, and configure the following settings:

- Port: COM### (Class Application, User UART, from Figure 4-1)
- Speed: 115200
- Data: 8 bit
- Parity: none
- Stop bits: 1 bit

Click *New Open*. Assert the AM26x Power-On-Reset (PORz), which is accomplished by triggering a PORz reset circuit on the PCB, or by simply power cycling the PCB system.

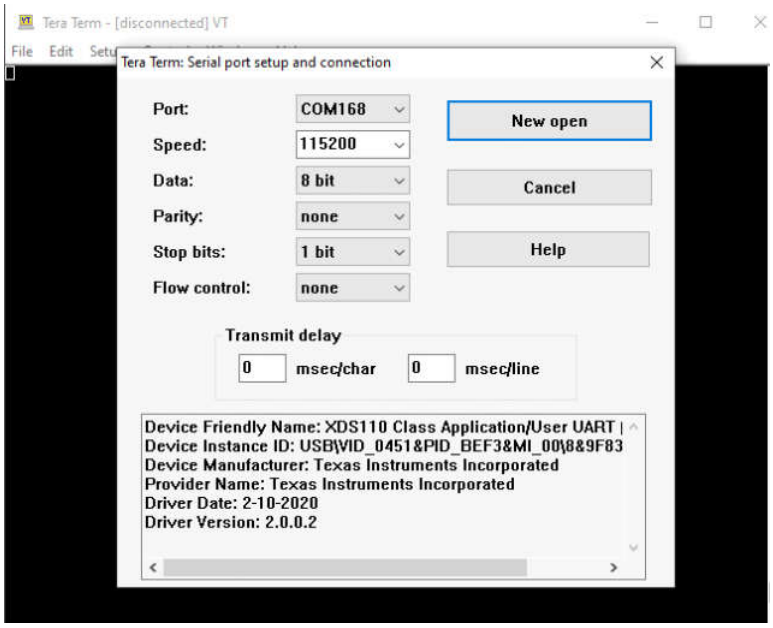

Figure 4-2. Tera Term Setup

After power cycling the AM26x, the ASCII character 'C' prints to the UART console. This confirms that the AM26x is alive and is booting via UART.

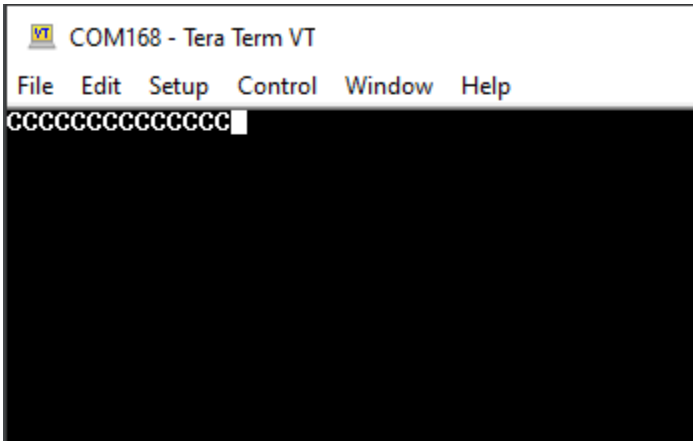

Figure 4-3. AM26x UART Boot Console Output

UART Boot Debug

If Cs are not printing to the UART console, then make sure the following are checked.

- Check that the UART terminal application baud rate is set to 115200.
- Confirm the AM26x boot mode is UART, or boot mode with UART fallback.
- Power-on-reset the AM26x.

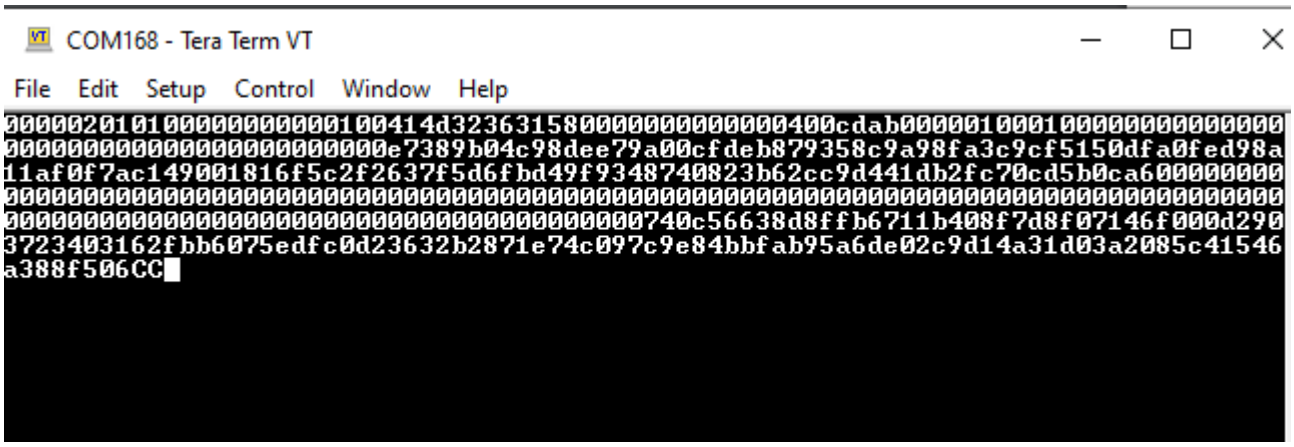

Figure 4-4. UART Console After Power-on-Reset, with Cs Printing At the End of the UART Output

5 Verify JTAG Connection

Establishing a UART connection and confirming that the device boots certifies that the AM26x device is alive on the PCB. Next, the JTAG connection is verified to check the debug interface with a host PC.

5.1 Configure AM26x for JTAG

To configure the AM26x device for JTAG debug, set the SOP[3:0] pins to **1011**. The boot mode setting for JTAG debug, referred to as DevBoot is the same for all AM26x devices.

Connect the AM26x JTAG pins (TDI, TDO, TMS, TCK) to a JTAG emulator such as the XDS110 JTAG Debug Probe or similar hardware debugger platform, and connect the debugger to a host PC.

5.2 Configure Host PC for JTAG Debug

Code Composer Studio Setup

On the host PC, make sure the latest version of TI Code Composer Studio (CCS) is installed.

Note

- If downloading for the first time, then select *Custom Installer* in the installation executable.
- Select *Sitara AM2x MCUs* when selecting components.

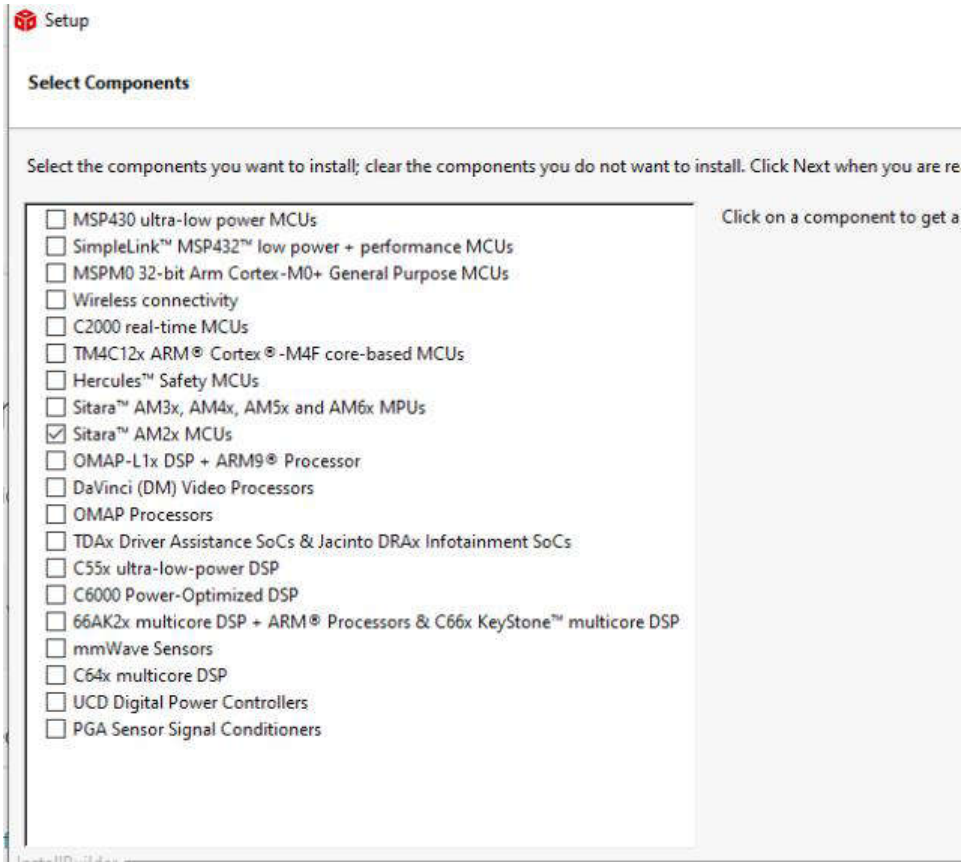

Figure 5-1. Code Composer Studio Installation - Component Selection

Create AM26x Target Configuration

Once Code Composer Studio has finished the installation process, create a new Target Connection for the AM26x device.

1. In CCS, *View* → *Target Configurations*.

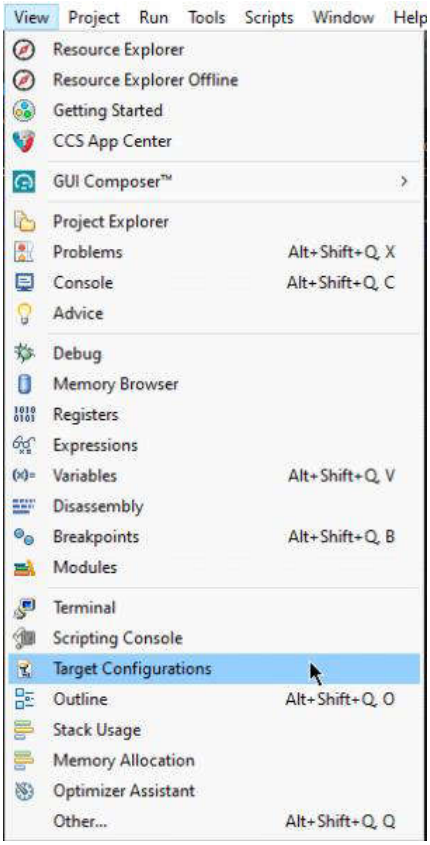

Figure 5-2. View → Target Configurations

2. In the Target Configurations window, right-click *User Defined* and select *New Target Configuration*.

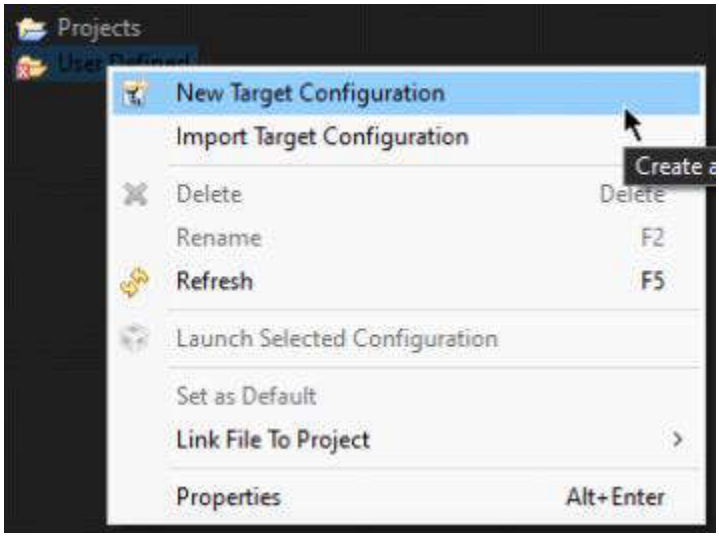

Figure 5-3. User Defined → New Target Configuration

3. Name the Target Configuration and click *Finish*.

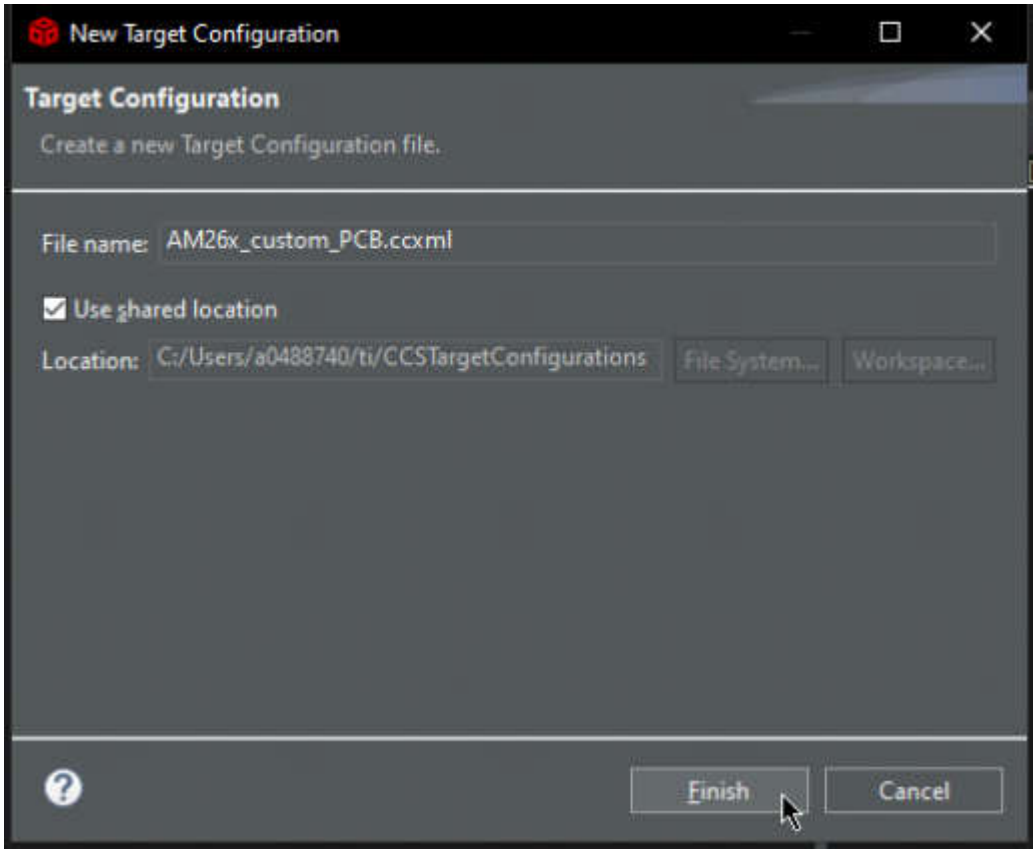

Figure 5-4. Name the Target Configuration

4. In General Setup, select the *Connection* (XDS110 USB Debug Probe, in this example) and the AM26x device on the PCB system (AM263Px used in this example).

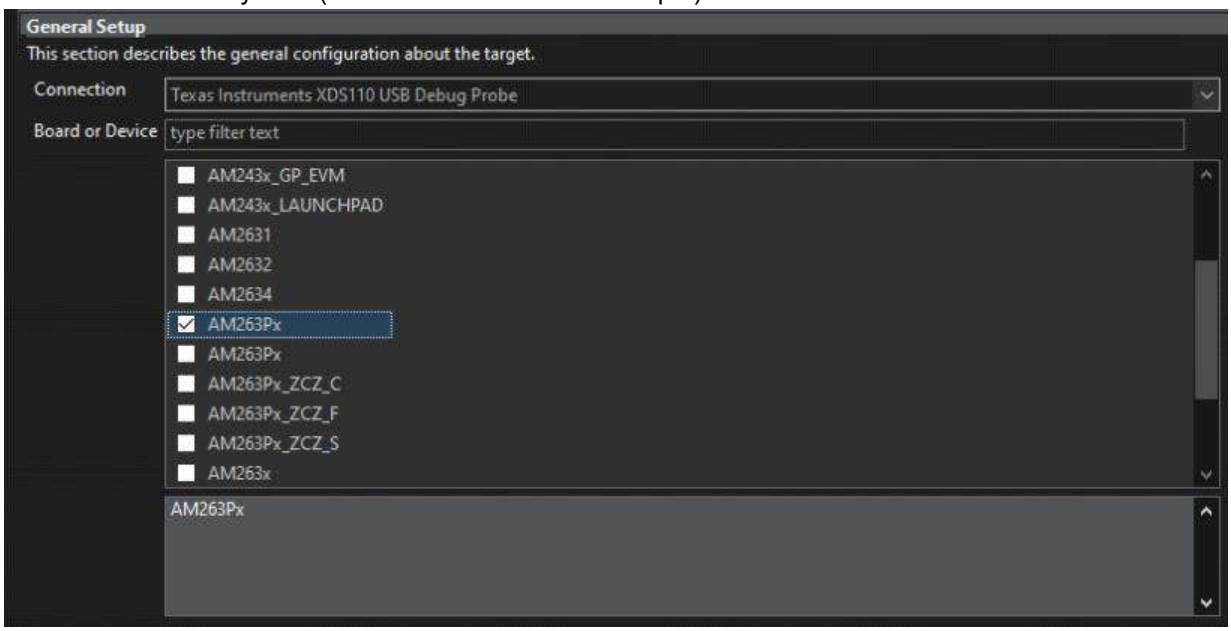

Figure 5-5. General Setup - Connection

5.3 Test the JTAG Connection

Once the General Setup of the Target Connection is complete, click *Save Configuration*, then *Test Connection*.

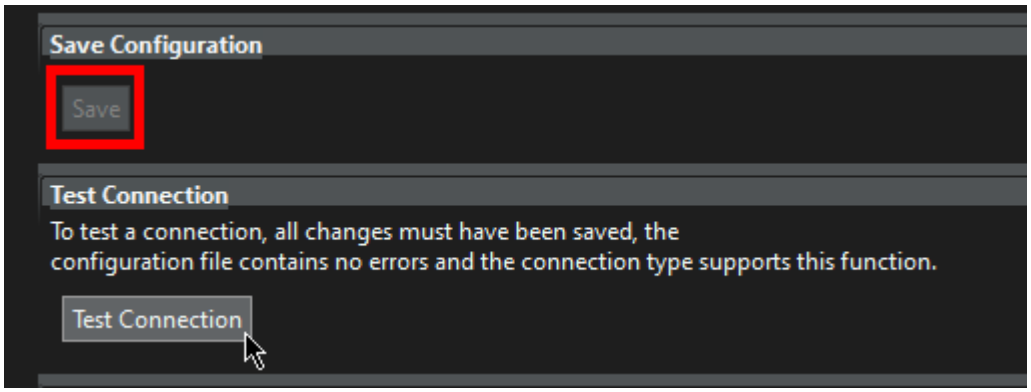

Figure 5-6. Save and Test JTAG Connection

The JTAG Connection window pops up. Confirm that the JTAG DR Integrity scan-test has succeeded by observing the console output.

```
The JTAG DR Integrity scan-test has succeeded
```

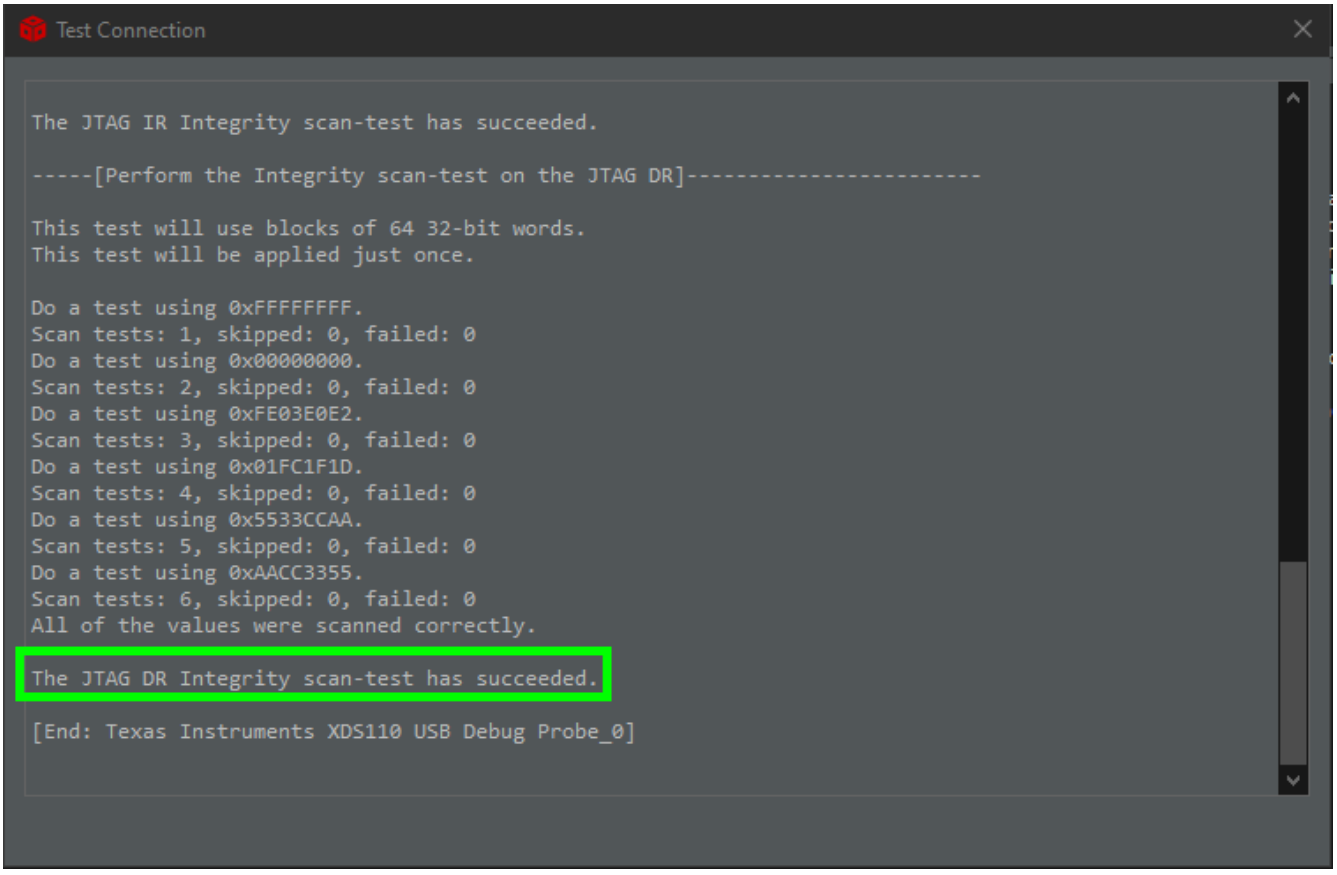

Figure 5-7. JTAG Connection Test Output

5.4 Connect to the AM26x R5F Core

Launch the Target Connection

If the JTAG scan-test is successful, then right-click the *Target Configuration ccxml file* → *Launch Selected Configuration*.

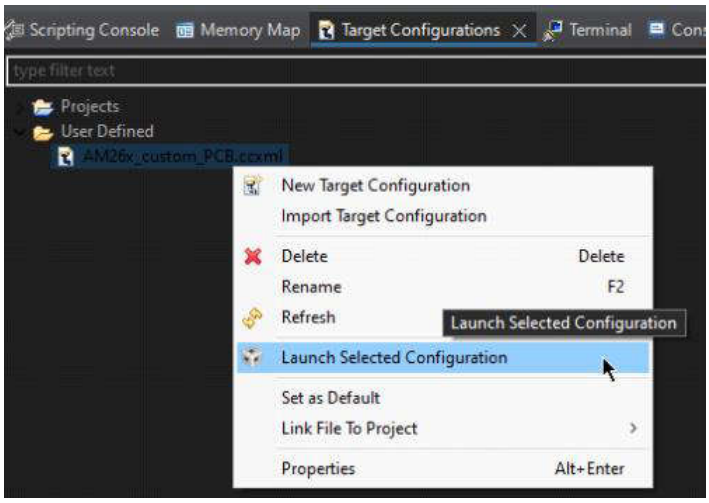

Figure 5-8. Launch the Target Configuration

Connect to the AM26x

Once loaded, right-click on the R5_0 core and click *Connect Target* in the *Debug* window.

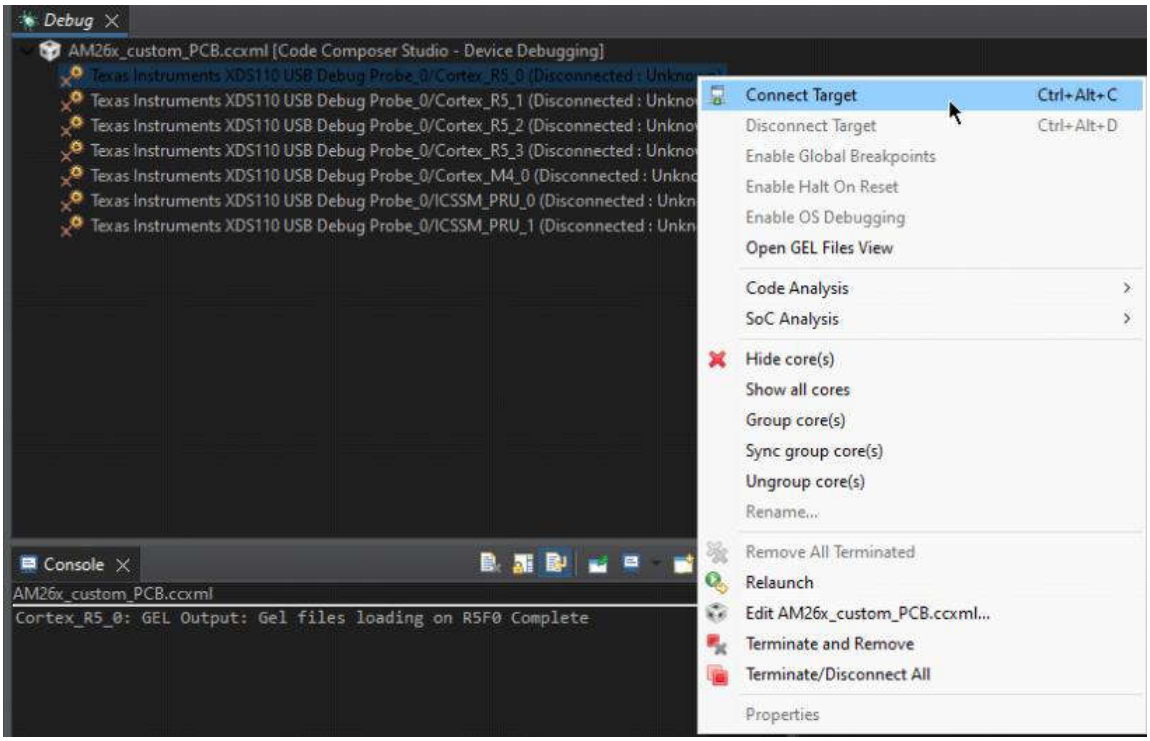

Figure 5-9. Connect Target

Observe the console output. If the output console is not visible, then select *View* → *Console* in Code Composer Studio.

Connecting to the AM26x target automatically loads GEL (General Extension Language) files to the AM26x R5F Core to initialize the AM26x device. This includes configuring device clocks, enabling peripheral clocks, and unlocking control registers.

Alternative GEL File Loading Method

GEL files can also be manually loaded to the AM26x device. While this is not recommended for initial bring-up, this allows for more customization and bring-up of specific device blocks, rather than the entire set of AM26x peripherals.

1. Right-click the R5_0 Core and click *Open GEL Files View*.

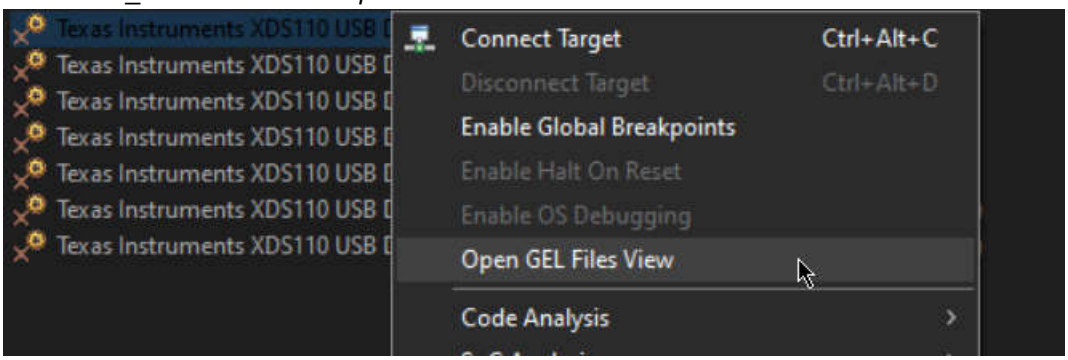

Figure 5-10. Open GEL Files View

2. A window displaying the GEL files opens. Device-specific GEL files can be found at *{CCS_install_path}/ccs[version]/ccs_base/emulation/gel/[device_name]*.

Note

GEL files are only compatible with the target device. AM263x GEL files are only compatible with AM263x, and so forth.

If no errors are observed in the output console, then JTAG connection to the device is verified.

6 Loading and Executing a Code Example

After connecting the AM26x device via JTAG, a software example can be loaded to the AM26x and executed on the device. This section details running the *Hello World* example binary from the *MCU+ SDK* on the AM26x to verify proper program loading and output.

Note

This section is a continuation of the previous section. This is assumed that the AM26x core is already connected by JTAG, and the system is in an idle state.

6.1 Importing, Building, and Loading the Project

Note

Make sure that the latest AM26x MCU+ Software Development Kit is installed on the host PC.

- AM263x: https://www.ti.com/tool/MCU-PLUS-SDK-AM263X
- AM263Px: https://www.ti.com/tool/MCU-PLUS-SDK-AM263PX
- AM261x: https://www.ti.com/tool/MCU-PLUS-SDK-AM261X

Import the Project

1. In Code Composer Studio, select *File* → *Import*.

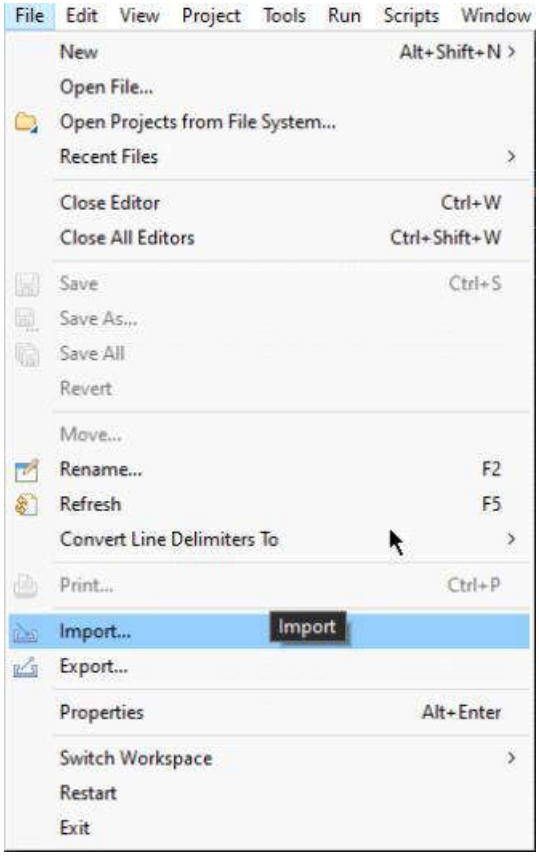

Figure 6-1. Import Project

2. Select *CCS Projects*.
3. In the *Import* window, select *Browse* and navigate to *mcu_plus_sdk_{AM26x_device_name}_{version}\examples\hello_world\am263px-cc\r5fss0-0_freertos\ti-arm-clang*.
4. Click *Finish*.

Build the Project

In the *Project Explorer* window, right-click the project name and select *Build Project*.

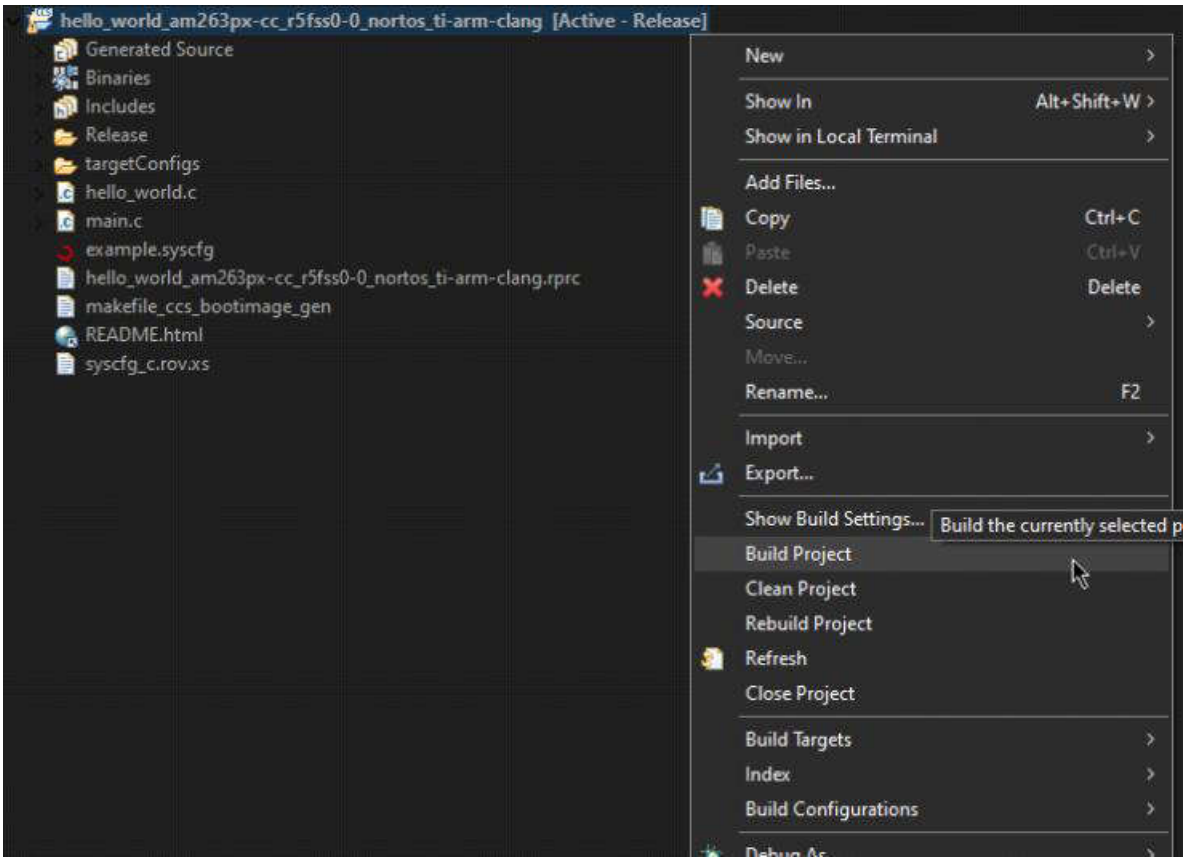

Figure 6-2. Build Project

After the project has completed building, connect to the R5_0 core of the target connection as outlined in Section 5.4 if this is not done already.

Load the Program

1. In the CCS toolbar, click *Run* → *Load* → *Load Program*.

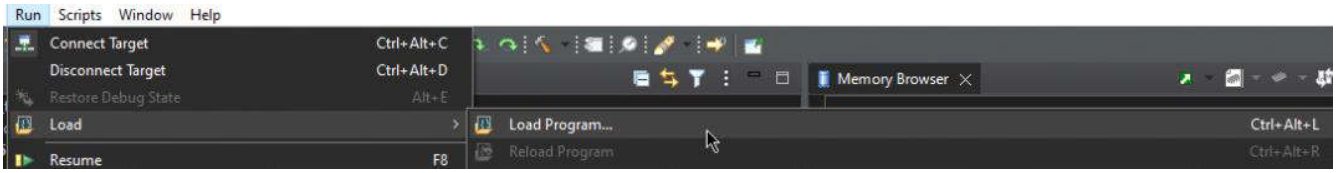

Figure 6-3. Load Program

2. In the *Load Program* window, select *Browse Project* and navigate to the *Release* folder of the CCS project.

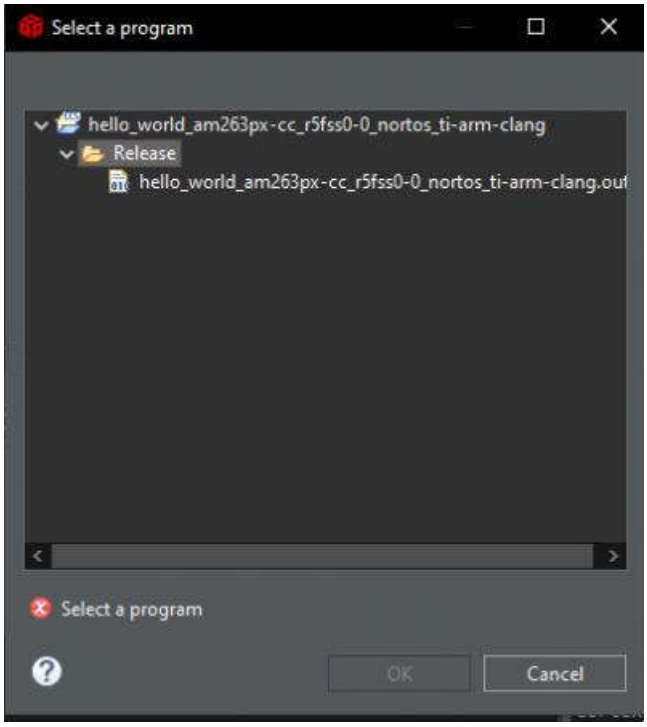

Figure 6-4. Release Folder

3. Click *OK* to load the project binary file to the AM26x device R5_0 Core.

Note

If the program load fails, then perform a CPU reset by selecting the *CPU Reset* icon in the CCS toolbar. Then re-load the program.

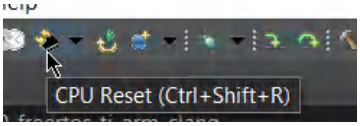

Figure 6-5. CPU Reset

4. Click the *Play (Resume)* button in the CCS toolbar to run the binary on the AM26x device.

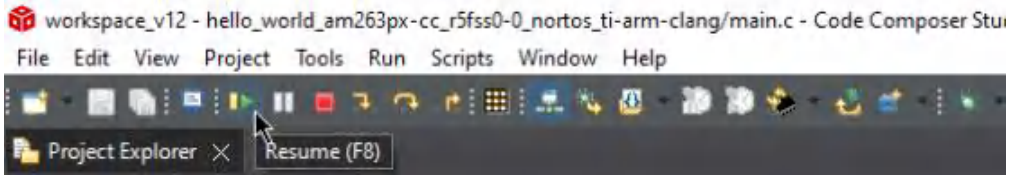

Figure 6-6. Resume Binary

5. Observe the console output. The proper output is in Figure 6-7.

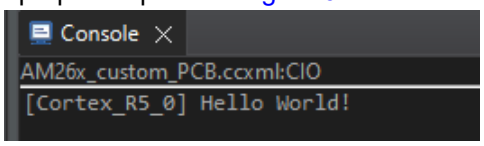

Figure 6-7. Hello World Console Output

The basic checks for bringing up a custom PCB with an AM26x device are now complete.

7 Summary

This application note describes the process of bringing up an AM26x-based PCB system, and how to diagnose and debug potential issues that can be encountered in the bring-up sequence. This concludes the process for initial bring-up on a custom AM26x PCB system. After completing each item in this guide, an engineer can have confidence that the AM26x system is behaving normally in terms of power, boot, and debug connectivity. Application development can go forward without concern for the health of these system attributes.

8 References

General AM26x Resources

- Texas Instruments, AM26x Hardware Design Guidelines, application note

AM263x

- Texas Instruments, AM263x Sitara™ Microcontrollers, data sheet
- Texas Instruments, AM263x Sitara™ Microcontrollers Texas Instruments Families of Products, technical reference manual
- Texas Instruments, AM263x Register Addendum, technical reference manual
- Texas Instruments, AM263x Software Development Kit (SDK), webpage

AM263Px

- Texas Instruments, AM261x Sitara™ Microcontrollers, data sheet
- Texas Instruments, AM263Px Technical Reference Manual, technical reference manual
- Texas Instruments, AM263Px Register Addendum, technical reference manual
- Texas Instruments, AM263Px Software Development Kit (SDK), webpage

AM261x

- Texas Instruments, AM261x Sitara™ Microcontrollers, data sheet
- Texas Instruments, AM261x Technical Reference Manual, technical reference manual
- Texas Instruments, AM261x Register Addendum, technical reference manual
- Texas Instruments, AM261x Software Development Kit (SDK), webpage

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2025) to Revision A (May 2025)	Page
• Added 'O' speed grade core voltage requirements for AM261x devices	3
• Added current information for 500MHz AM261x devices	3
• Added note for industrial-grade AM261x devices running at 500MHz. The core VDD requirement is 1.25V	4

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