Application Note

Handling PWM Challenges in Resonant Converters

Brian Wang

ABSTRACT

Nowadays, topologies that requiring PWM phasing-shifting and frequency-changing have been widely used in digital power applications. Complicated topologies like multi-phase interleaved LLC have been introduced as the result of demand for higher efficiency and higher power level. To handle the challenge, Type-4 PWM is introduced on TI generation 3 C2000 devices. Especially, new features like global load and one shot reload would significantly simplify implementation phase-shifting and frequency changing topology. This application note discusses the benefit of these new features, and how to deal with corner cases in real practice.

Table of Contents

List of Figures

Trademarks

1 Introduction

With higher requirement of power rating and efficiency in power applications like server and telecom PSU, resonant converters like LLC have become the prioritized option of DC/DC stage in more and more new designs. Comparing with traditional full-bridge topology, LLC is easier to achieve soft switching due to resonant operation, leading to better EMI performance, higher efficiency and less stress on power stage.

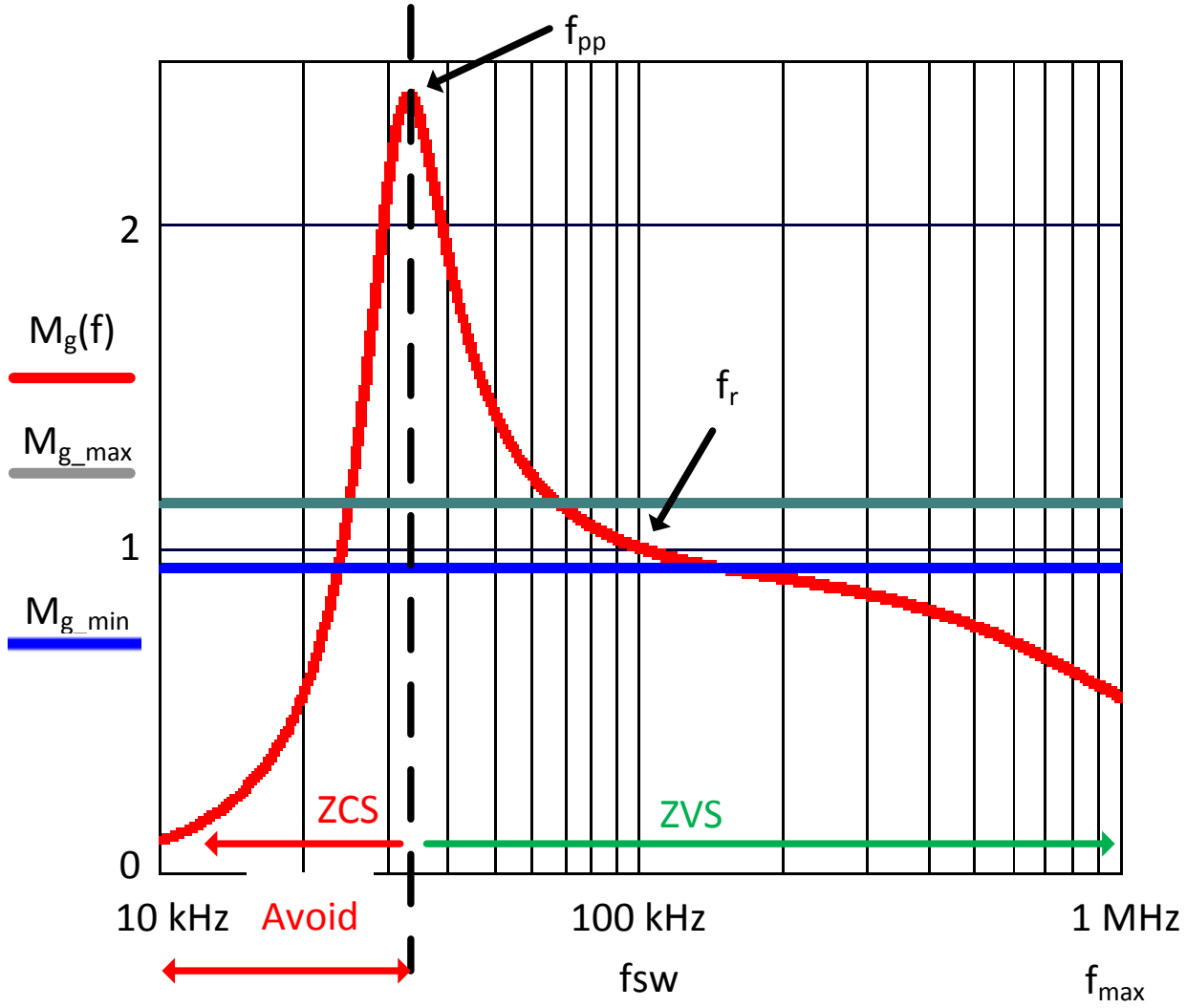

Figure 1-1. Plot of Gain vs. Frequency

Normally the LLC converter works under variable frequency but fixed duty cycle. The typical gain curve of a LLC converter is shown in the following picture. The converter works near f_r and adjust switching frequency through the control loop to stabilize the output voltage.

2 Challenge of Implementing LLC Control in MCU

Comparing to traditional power topologies that normally work under fixed switching and ISR frequency. LLC topology becomes more complicated to control by MCU due to the following two aspects.

2.1 Frequency Changing Requires Multiple PWM Configuration update

In LLC converter a switching frequency change would require multiple PWM registers to be updated accordingly, including TBPRD, CMPx or TBPHS in multi-phase interleaved topology. Thus, it is necessary to have a mechanism to shorten the CPU cycles needed for updating registers and to sync up the shadow to load active of multiple registers.

In type-4 ePWM, a new global load feature can be used for all the shadow registers if the corresponding GLDCFG[REGx] is set to 1, and all the load from shadow to active register happens simultaneously once the event configured by GLDMODE register happens. The available global load event source is presented in Figure 2-1.

Additionally, in LLC converter, since multiple power switches share the same switching frequency and duty cycle in the converter. The PWMLINK can be enabled by configuring the corresponding bits in EPWMXLINK register. For example, if EPWM2LINK[CMPALINK] is set to 0x0000(EPWM1), then all the writing to EPWM1 CMPA register result in a simultaneous writing to EPWM2 CMPA.

By doing all the procedures above, you could shorten the PWM upgrade time period as much as possible, and also forbidden unexpected shadow to active load before PWM upgrade finishes.

Overall, type-4 ePWM's new feature would significantly simplify the control of LLC conversion and help reduce the potential risk caused by unexpected PWM behavior.

2.2 No Fixed Timing Relationship Between Control and Switching Frequency

The typical way of achieving LLC control in MCU is to implement a control loop with fixed frequency, so that the interrupts and background loops can all be well organized and responded correctly. However, since the LLC switching frequency is changing from cycle to cycle, the timing relationship between switching and control ISR becomes unpredictable.

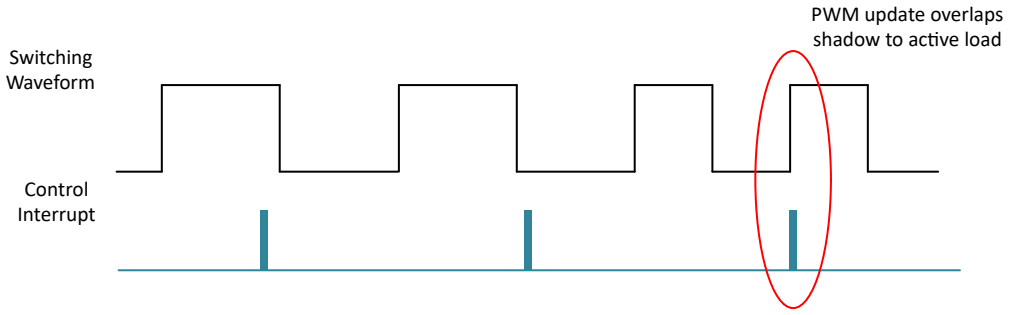

Figure 2-1. PWM Update Overlapping With Shadow to Active Load

Traditionally, shadow register is loaded as active whenever the event configured happens. And in type-4 PWM it can be CTR=PRD, CTR-Zero and, and so forth. Thus, in LLC converter it is important to ensure PWM configuration is carefully updated at the beginning or ending of a PWM switch cycle, to guarantee it does not cause any PWM disorder. Ideally the shadow to active load should be forbidden when PWM configuration update happens, so duty cycle, period and phase shift mismatch would not happen.

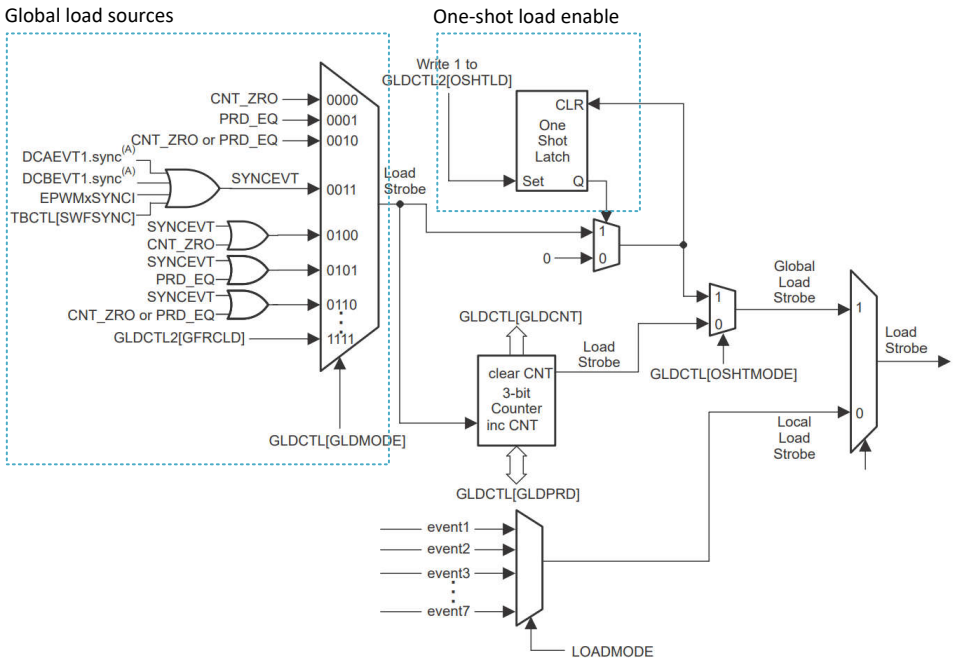

Figure 2-2. Type -4 ePWM Global Load Block Diagram

To solve this problem, one shot load is introduced in C2000 type-4 ePWM. The idea is to add an additional 'mask' to the shadow to active load event. The shadow to active load will only be trigger by the load event when GLDCTL2[OSHTLD] is set as 1, and this bit will be cleared automatically once a load happens, to get ready for the next update.

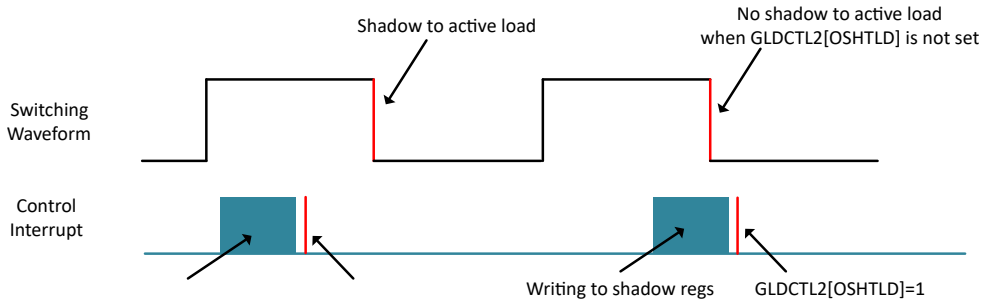

Figure 2-3. One-Shot Load Feature

3 Corner Cases and Real-Case Challenges

However, in real case practice, even with global load and one-shot load enabled, some unexpected PWM behaviors have been observed occasionally. Even the behaviors are caused by rare corner cases, and only have very low possibilities to happen, but may still cause sever damages, especially in important power supply applications.

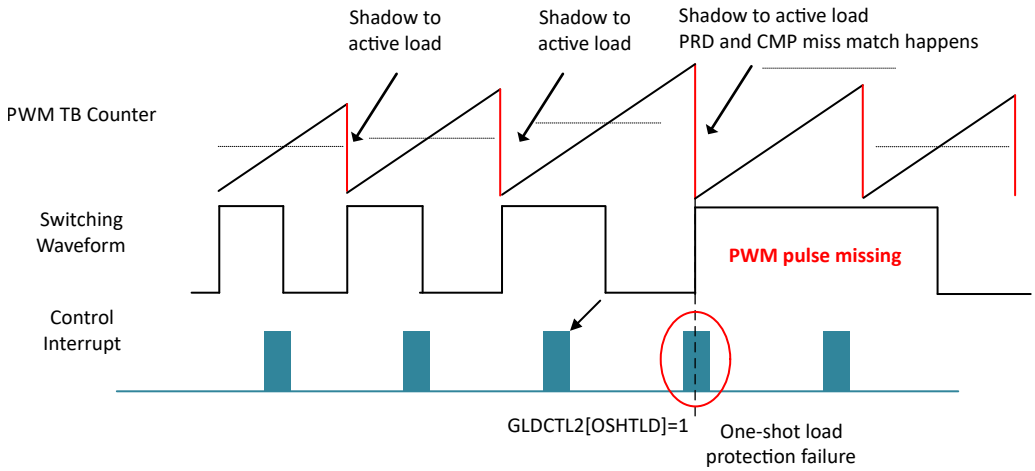

Figure 3-1. PWM Disorder in LLC converter

In real case LLC applications, in order to achieve better transient performance, the switching frequency range is selected to be a wide range. For example, 20kHz to 200kHz is the switching frequency normally used in server PSU industry, while 100kHz is the typical control loop ISR frequency. During the transient when LLC works in low switching frequency, there is a possibility that multiple control ISR may happen within the same switching period. Following the recommended one-shot load operation, GLDCTL2[OSHTLD] is set to 1 in the first control ISR. Global load will be responded and GLDCTL2[OSHTLD] will be cleared at next CTR=PRD. However, since the switching frequency is low, the second control ISR happens before switching period ends. Since GLDCTL2[OSHTLD] has already been set, the shadow to active would happen once CTR equals to PRD. Under this condition, one-shot load will not work and PWM disorder may happen as explained in Section 2.1.

3.1 Software Workaround

A simple workaround can be achieved with the following method:

```
while(EPwm1Regs.TBCTR>(EPwm1Regs.TBPRD - PwmUpdateTime))
{
} // Wait in while if there is no enough time for PWM register update.
PWMRegsUpdate(); //Function to update PWM shadow registers. Make sure to put all register updating
code here before seting global load one-shot bit
EPwm1Regs.GLDCTL2.all = 1;
```

Where PwmUpdateTime is a constant that represents the time cycles reserved for PWM shadow register writing.

By doing this, a time period before the PWM cycle end is reserved. If the PWM updating happens during the reserved period, the CPU will run in a while loop and not to write PWM shadow registers until the reserved time period has passed. In this way, even GLDCTL2[OSHTLD] is set by a previous ISR in the same switching cycle, no mismatched PWM register update will happen.

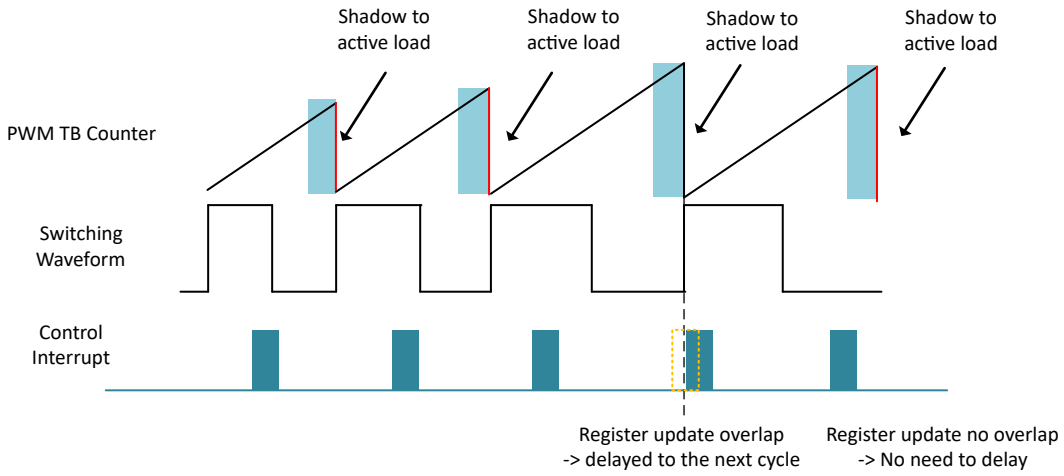

Figure 3-2. Software Workaround

3.2 CLB-Based Hardware Workaround

Though the software workaround is simple, but would require extra code and CPU bandwidth to monitor the PWM time base counter, and needs to spend CPU cycles waiting for the available timing for PWM register update. For a typical register update including TBPRD, CMPx and TBPHS register, it requires ~50 CPU cycles, which equals ~0.5μs for a 100Mhz CPU, which takes 5% for 100kHz interrupt.

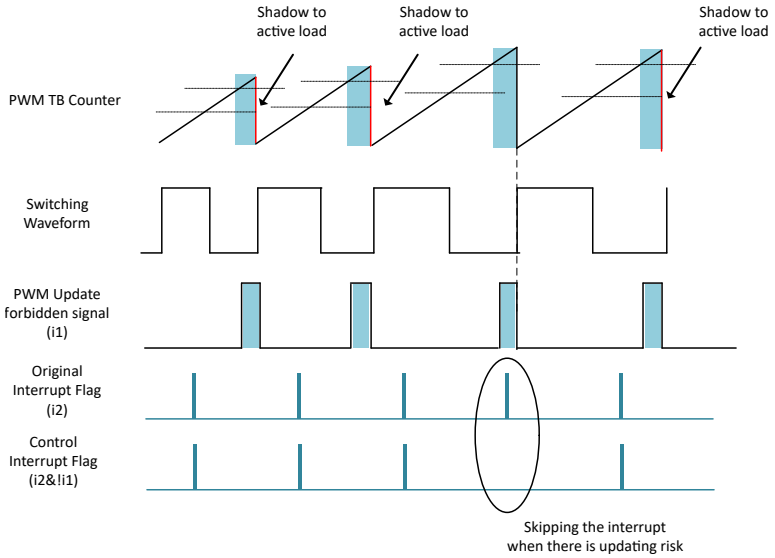

Figure 3-3. CLB Workaround Block Diagram

Another options is to implement the PWM updating nesting logic in the configurable logic block (CLB). The solution introduce original control interrupt signal and a PWM updating forbidden signal in to CLB, and generate another CLB interrupt to trigger the real control loop interrupt. With the logic inside CLB, all the original control interrupts happen during the PWM updating forbidden signal will be nested, so no control loop interrupt will be triggered, and all the risk of PWM disorder will the eliminated.

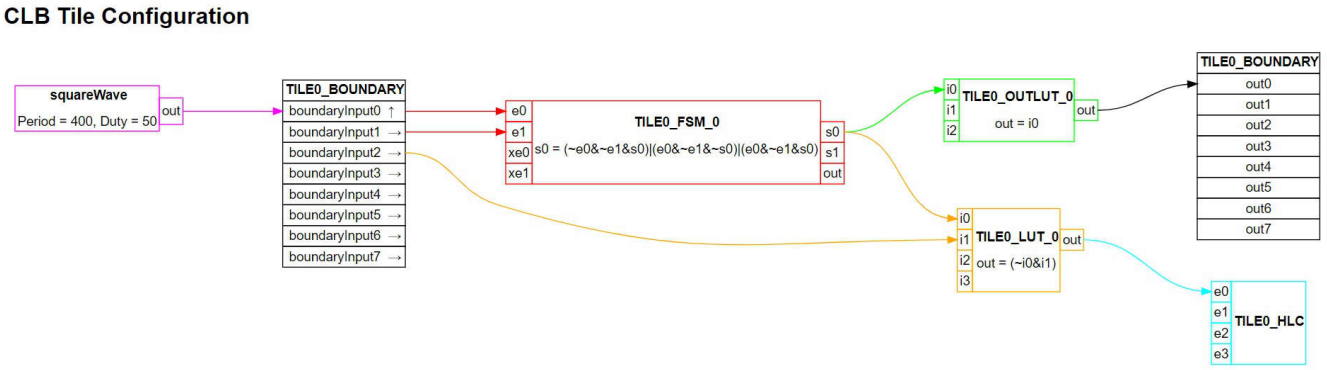

Figure 3-4. CLB Tile Configuration

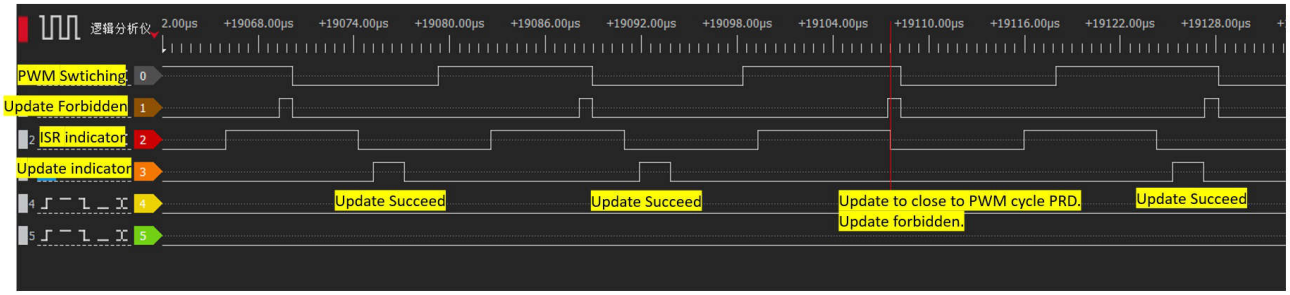

Figure 3-5. CLB Workaround Testing Result

4 Summary

This application note discusses the challenges of using Type-4 PWM in resonant converters. Even with advanced new features like PWM global and one-shot load, there are still some corners cases where unexpected PWM waveform would be generated due to incorrect PWM settings or PWM peripheral imperfections. Both software and hardware solution based on CLB have been proposed to handle the PWM abnormal challenges.

5 References

- Texas Instruments: *TMS320F28004x Real-Time Microcontroller Technical Reference Manual*
- Texas Instruments: *Leverage New Type ePWM Features for Multiple Phase Control*
- Texas Instruments: *Designing With the C2000™ Configurable Logic Block*
- Texas Instruments: *Implement Three-Phase Interleaved LLC on C2000TM Type-4 PWM*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265