Application Note

AM62x, AM62Ax, AM62Px, AM62Lx Spread-Spectrum Clocking

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ABSTRACT

Electrical interfaces that utilize high-frequency clocks to transmit and receive data radiate energy that can possibly interfere with nearby devices. This radiation is called Electromagnetic Interference (EMI). By making use of spread-spectrum clocking (SSC), EMI can be reduced to meet emission standards and regulations. SSC is a technique used to introduce controlled variation of the clock signal frequency to reduce EMI. When implementing SSC, EMI is distributed across a wider frequency range instead of concentrating solely at the nominal clock frequency. Care must be taken to modulate the clock within the tolerance of the overall system to avoid disrupting communication between the circuits and devices involved.

This document describes how EMI reduction is achieved when using the Display Parallel Interface (DPI) with a 24-bit RGB data output to modulate the pixel clock frequency using SSC. The method applies to AM62x, AM62Ax, AM62Px, and AM62Lx system-on-chip (SoC) designs.

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Trademarks

1 Spread-Spectrum Clocking

Due to the periodicity and square-shaped attributes of the digital clock signal, most of the energy of the clock concentrates at the center frequency and odd harmonics. SSC modulates the clock nominal frequency in a controlled manner to reduce the radiated emissions of the clock signal itself. In the frequency domain, SSC reduces the peak amplitude of the digital clock signal by spreading the localized peak energy across a wider frequency range. In the time domain, SSC injects jitter to the clock signal, but the voltage amplitude remains unchanged. The SSC of the SoC is fully described using the following parameters: modulation rate, modulation depth, spread type, and modulation profile.

Figure 1-1 shows the SSC characteristics using a common triangular-shape SSC modulation profile. SSC can be configured for the clock signal to either produce a symmetrical modulated output or configured to produce a down spread modulated output. The down spread type reduces the clock frequency from the center frequency.

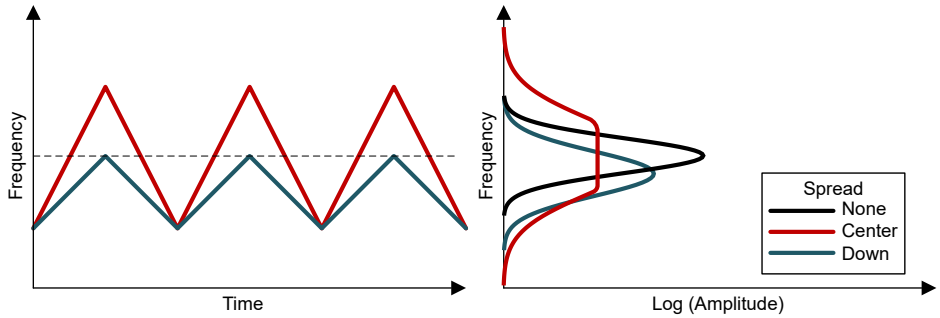

Figure 1-1. SSC Characteristics

1.1 SSC Modulation Rate

The modulation period is the time required to cycle the clock nominal frequency from an initial value through all the different values along the modulation profile and back to the initial value. The modulation rate is the inverse of the period.

1. The modulation rate is controlled by the CLKSSCG, the 128-point internal wave table, and the divide value MOD_DIV as $f_{mod} = f_{CLKSSCG} / (128 \times MOD\_DIV)$.
2. $f_{CLKSSCG} = f_{REF} / REFDIV$. With fractional-N mode set for AM62x, AM62Ax, AM62Px, and AM62Lx: REFDIV = 1. This means in this case $f_{CLKSSCG} = f_{REF}$, where f_{REF} is the PLL reference clock (for example, f_{REF} = 25MHz).
3. For modulation fidelity, which is determined by the PLL bandwidth, and to avoid interference with audio applications, the modulation frequency is typically set above 32kHz and below $f_{CLKSSCG} / 200$. For example, the maximum modulation frequency if a PLL reference clock frequency of 25MHz is used, is 125kHz.

1.2 SSC Modulation Depth

The modulation depth refers to the maximum variation in frequency as a percentage of the clock center frequency. For AM62x, AM62Ax, AM62Px, and AM62Lx, the minimum modulation depth is 0.1% and the maximum is 3.1%. Modulation depth can be adjusted in 0.1% increments.

1.3 SSC Spread Type

The clock frequency variation can be affected only on the negative side (lower frequency) or on both positive side (higher frequency) and negative side. When varied equally on both sides, the spread type is referred as centered. When varied on the negative side only, the spread type is referred to as down spread.

The AM62x, AM62Ax, AM62Px, and AM62Lx SoCs support both center and down spread.

CAUTION

Use center spread with caution because center spread increases the highest frequency of the interface above the nominal value. Care must be taken so that the interface is designed to handle this slightly higher frequency. Conversely, down spread results in an average frequency that is less than the nominal frequency.

1.4 SSC Modulation Profile

The modulation profile refers to the shape of the curve describing the variation of the modulated clock frequency. Conventional profiles include sinusoidal, triangular, sawtooth, and Hershey shape.

The AM62x, AM62Ax, AM62Px, and AM62Lx SoCs support triangular modulation by default. An external wave table can be used to modulate the clock frequency using a profile other than triangular.

2 PLL SSC Implementation Details

The PLL reference clock frequency, f_{REF}, undergoes an input predivider of REFDIV. This stage transforms high-speed signals into lower-frequency versions for processing. Next, a feedback multiplier (FB_DIV_INT) acts as a Voltage-Controlled Oscillator (VCO) and filter on the transformed signal. The filtered output feeds back to fine-tune performance. Finally, a post-divider, configured as HSDIV + 1, further decreases the signal frequency before being delivered by the PLL clock generator. The clock output frequency is calculated as $f_c = (f_{REF} / REFDIV) \times FB\_DIV\_INT / (HSDIV + 1)$. SSC is accomplished by varying FB_DIV_INT in small steps following a triangular pattern.

For the display parallel interface (DPI), the PLL used by the display subsystem (DSS) is commonly multiplexed to PLL17 by default for AM62x, AM62Ax, AM62Px, and AM62Lx. However, PLL16 or PLL18 can also be used for DPI. The pixel clock frequency for DPI coming from the DSS PLL (that is, PLL17) must not exceed 165MHz.

Table 2-1. SSC Supported Configurations

Parameter	MIN	MAX	Unit
Modulation depth	0.1	3.1	%
Spread type	Both center spread and down spread are supported		
Modulation rate	32	$f_{CLKSSCG}$ / 200	kHz

CAUTION

For DPI applications with SSC, only the DSS PLL allocated for DPI (PLL16, PLL17, or PLL18) is approved to be changed by customers. Use of other PLLs is neither approved nor recommended.

2.1 PLL SSC Configuration Registers

Table 2-2 describes the registers involved to configure SSC for PLL17, which is the DSS PLL commonly used for DPI.

Table 2-2. SSC Related Register Fields

Register Name	Physical Address Offset	Bit Field Information		
		Bit No.	Name	Description
PLL17_CTRL	0x11020	1	DSM_EN	Delta-sigma modulator enable
				1'b0: Delta-sigma modulator disabled (integer divide mode)
				1'b1: Delta-sigma modulator enabled (fractional divide mode)
		0	DAC_EN	Fractional noise canceling DAC enable
				1'b0: Fractional noise canceling DAC is disabled
				1'b1: Fractional noise canceling DAC is enabled
PLL17_SS_CTRL	0x11040	31	BYPASS_EN	Bypass the SS modulator
				1'b0: Spread-spectrum modulation (SSMOD) is enabled
				1'b1: SSMOD is bypassed
		4	DOWNSPREAD_EN	Center or down spread clock variance select
				1'b0: Center spread
				1'b1: Down spread

Table 2-2. SSC Related Register Fields (continued)

Register Name	Physical Address Offset	Bit Field Information		
		Bit No.	Name	Description
PLL17_SS_SPREAD	0x11044	19:16	MOD_DIV	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1–63. $f_{mod} = f_{CLKSSCG} / (128 \times MOD\_DIV)$.
				1'h6: 32.6kHz if $f_{CLKSSCG}$ = 25MHz
				1'h5: 39.1kHz if $f_{CLKSSCG}$ = 25MHz
				1'h4: 48.8kHz if $f_{CLKSSCG}$ = 25MHz
				1'h3: 65.1kHz if $f_{CLKSSCG}$ = 25MHz
				1'h2: 97.7kHz if $f_{CLKSSCG}$ = 25MHz
		4:0	SPREAD	Sets the spread modulation depth
				5'b00001: 0.1%
				5'b01010: 1%
				5'b10100: 2%
				5'b11001: 2.5%
				5'b11111: 3.1%

2.2 PLL SSC Implementation Sequence With DSS PLL17 on AM62Px

The SSC manual implementation sequence described below needs to be done after the full PLL sequence (as defined by the API firmware) occurs and the PLL is locked. The SSC registers described in this document no longer need to be reconfigured manually once a standard SSC software interface is put in place with the SDK11.2 release, which is anticipated to happen at the end of 2025.

1. To enable fractional divide mode since spectrum spreading is not allowed in integer mode, enable the delta-sigma modulator by setting PLL17_CTRL[1] DSM_EN to 1’b1 and enable the fractional noise canceling DAC (if not already enabled) by setting PLL17_CTRL[0] DAC_EN to 1’b1.
   - Set 0x691020 to 0x00018013
2. Enable spread-spectrum modulation by setting PLL17_SS_CTRL[31] BYPASS_EN to 1’b0
   - Set 0x691040 to 0x00000000
3. Set the spread type by setting PLL17_SS_CTRL[4] DOWNSPREAD_EN to 1’b0 for center spread or 1’b1 if down spread
   a. If down spread, set 0x691040 to 0x00000010
   b. If center spread, set 0x691040 to 0x00000000
4. Set the modulation rate by setting PLL17_SS_SPREAD[19:16] MOD_DIV. 1’h6 corresponds to a modulation rate of 32.6kHz and 1’h2 corresponds to a modulation rate of 97.7kHz.
5. Set the modulation depth by setting PLL17_SS_SPREAD[4:0] SPREAD. 1’h1F corresponds to a modulation depth of 3.1% and 1’h01 corresponds to a modulation depth of 0.1%.
   a. If mod rate of 32.6kHz and mod depth of 3.1%, set 0x691044 to 0x0006001F
   b. If mod rate of 97.7kHz and mod depth of 0.1%, set 0x691044 0x00020001

CAUTION

When using center spread, maintain these two things:

1. Target display is capable of communicating with the SoC at the higher and lower peak modulation frequencies.
2. The highest frequency of the clock after SSC must still be less than 165MHz. The overshoot of 20% on the modulated depth must also be factored in while computing the highest possible frequency.

3 SSC Conclusion and Considerations

Some display panels can have clocking limitations not specified in the data sheets, so the displays need to be validated to have sufficient functional margin with the jitter introduced by spread spectrum modulation. Any display-related issues due to the introduction of SSC need to be worked directly with the display panel manufacturer. To minimize the impact of introducing jitter to the overall system, the recommendation is to keep the modulation depth as low as possible while still meeting emission standards and regulations with sufficient margin.

CAUTION

The customer assumes all responsibility for the configuration and usage of spread-spectrum clocking. The customer must research the clock limitations associated with the selected display panel and configure SSMOD to be compatible with that specific display panel. There are no plans for TI to participate in the assessment of the appropriate SSMOD configuration because TI does not know the clocking limitations associated with the selected display panel. The customer also needs to verify that the SSMOD configuration does not cause any system-related issues for any operating condition. The customer must work with the display panel vendor to resolve any issue caused by enabling SSC with SSMOD.

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