Application Note

Optimized Control Schemes for Totem Pole PFC With Digital Controller

Aki Li

ABSTRACT

Among the different PFC topologies, totem-pole PFC is attracting more attention because it can offer the highest efficiency among the bridgeless PFC topologies. Due to more complicated schemes and special requirements to support boundary conditions, it is common to use digital controller for the totem pole PFC. This application note discusses several control schemes to optimize the totem pole PFC performance based on C2000 real-time MCU, in order to achieve more reliable and flexible system designs.

Table of Contents

List of Figures

Trademarks

1 Optimized ePWM Configurations

A basic totem-pole PFC structure is shown in Figure 1-1. Different from the boost converter, the control of a totem-pole PFC is much more complex. Based on the input voltage VAC polarity, high frequency FETs Q1 and Q2 alternately work as a PFC active switch or sync switch, while slow frequency FETs Q3 and Q3 switch at grid frequency. The basic control logic could refer to *Control challenges in a totem-pole PFC*. In the actual applications, it is required to consider how to better handle the transient conditions, when the power stage enters overload conditions, light load or fault conditions, which is discussed in the proposed PWM configurations.

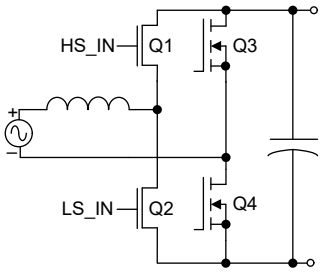

Figure 1-1. Totem-Pole PFC Structure

1.1 Cycle by Cycle (CBC) Protection

When PFC runs into overload conditions, for example, during AC voltage transient from high line to low line, or some fault events occur, it is required to implement overcurrent protection with CBC based PWM shut down control, in order to limit the PFC inductor current instead of shutting down the power stage. Normally, it is common to configure both PWM output for Q1 and Q2 to turn off together as soon as the inductor current reaches the overcurrent threshold. However, it might induce the risk for the power stage, especially during high temperature.

Because of the reverse recovery issue, a regular MOSFET cannot be used in a continuous-conduction mode (CCM) totem-pole PFC, so Q1 and Q2 need to be GaN or SiC FETs. As discussed in the third quadrant operation of GaN, located in *Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN*, the reverse conduction voltage Vsd is much higher under third quadrant operation, ranging from 3 V~5 V, or even more with larger reverse current, which also applies for SiC. The high reverse conduction voltage can cause excessive losses, and it brings concerns on device's thermal limitation and system reliability. Take positive cycle operation as example, showed in Figure 1-2, with the traditional PWM configurations, after both high side and low side FETs shut down at overcurrent event, large inductor current will continue to flow on the high side FET, so the conduction loss increases due to the third quadrant operation, which might cause the junction temperature rise up and lead to thermal damage for the GaN or SiC.

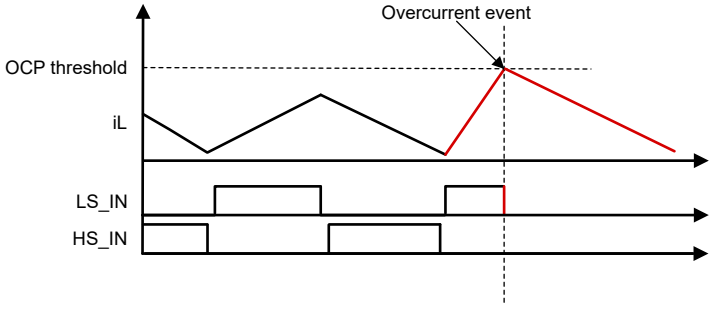

Figure 1-2. PWM Configurations for Traditional CBC Protection

Therefore, an ideal CBC protection scheme for the PWM configurations is shown in Figure 1-3. The PWM for the sync switch (high side FET Q1 for positive cycle in this case) should be turned on after the active switch turns off, with a customized dead time. However, the traditional trip-zone (TZ) submodule of ePWM could not be used to achieve the above logic. As shown in Figure 1-4, when a cycle-by-cycle trip event occurs, the action specified in the TZ submodule is carried out immediately on the ePWMxA and ePWMxB outputs, without any delay, since the TZ submodule is the last part before the ePWM outputs. In addition, for totem pole PFC, the ePWM output used for active FET and sync FET is different based on the VAC polarity, so the actions set inside the TZ submodule could not work for both positive and negative cycle automatically.

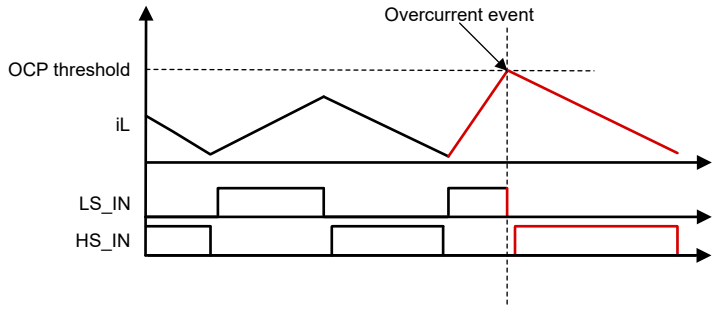

Figure 1-3. PWM Configurations for Ideal CBC Protection

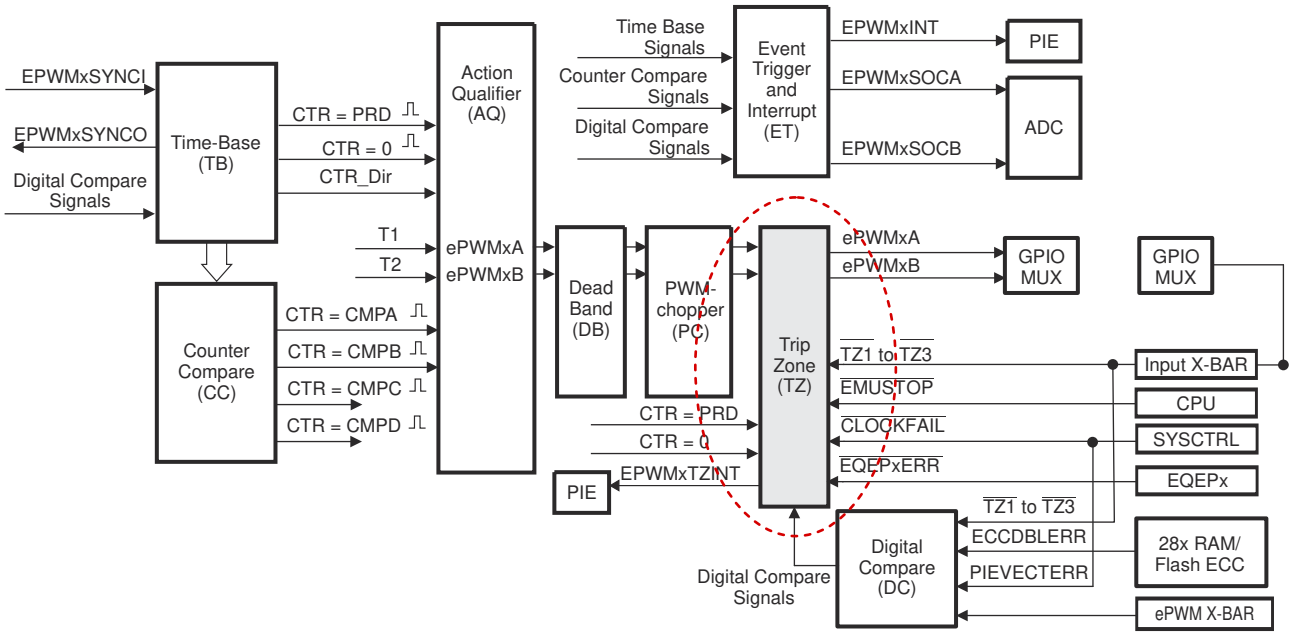

Figure 1-4. ePWM Submodules

1.2 Reverse Current Control

As discussed in *Control challenges in a totem-pole PFC*, large reverse current is generated when input AC voltage drops, and the power stored in the output capacitor is discharged and the hold-up time can no longer be assured. Another condition is the light load operation, when CCM operation changes to discontinuous conduction mode (DCM), in order to improve the light load efficiency. Thus, in either condition, it is required to fast detect the reverse current and then shut down the sync switches, or all the switches for simplicity, as shown in Figure 1-5.

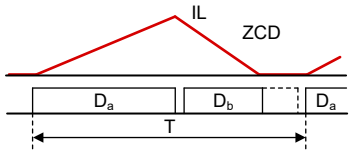

Figure 1-5. Reverse Current Control

1.3 ePWM Configurations Proposed

Combining the above requirements, the below ePWM configurations are proposed, shown in Figure 1-6. Take ePWM1 as example, ePWM1A is defined to set high at ZREO event, and clear low at CMPA or T1 event. T1 event, which is triggered by the comparator for the inductor current, is selected to clear low ePWM1A at the overcurrent condition, in replace of the traditional CBC scheme. As shown in Figure 1-7, with the latest Type 4 ePWM, T1 and T2 events, sourcing from comparator, trip or sync events, can also generate actions through action qualifier (AQ) submodule. More details regarding new T1/T2 features can refer to TRM. Since the AQ submodule is before the dead band (DB) submodule, it is natural to enable the rising edge delay and falling edge delay for ePWM1A and ePWM1B, respectively, with active high complementary (AHC) mode. As shown in the 1st and 2nd cycle in Figure 1-6, it covers the normal operation and the overcurrent conditions. For the reverse current control, it can be simplified to use the traditional CBC protection based on the zero current detection (ZCD) event, which takes effect for both ePWM1A and ePWM1B. As shown in the 3rd cycle, ePWM1A output is already low during the negative current event, so it can be set with the same action as ePWM1B, regardless of the VAC polarity.

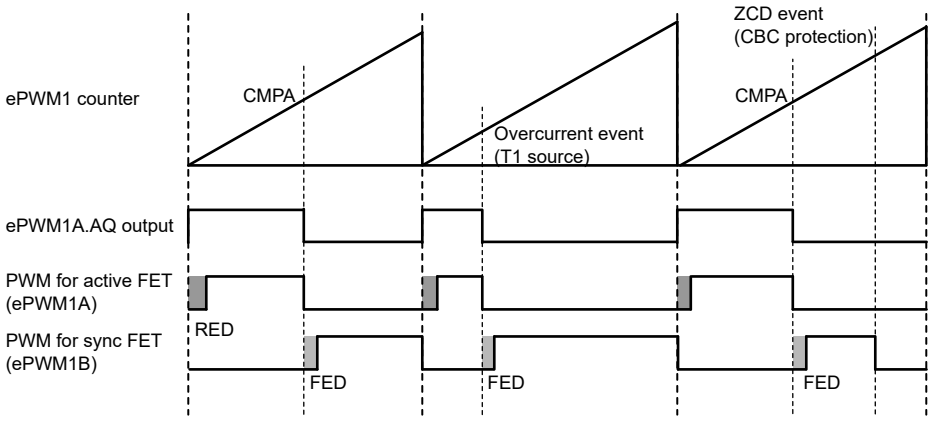

Figure 1-6. Basic ePWM Configurations Block Diagram

S/W force	TB Counter equals			Trigger Events			Actions
	Zero	Comp A	Comp B	Period	T1	T2	
SW	Z	CA	CB	P	T1	T2	Do Nothing
SW	Z	CA	CB	P	T1	T2	Clear Lo
SW	Z	CA	CB	P	T1	T2	Set Hi
SW	Z	CA	CB	P	T1	T2	Toggle

Figure 1-7. Action-Qualifier Actions for ePWMxA and ePWMxB Outputs

Since the active FET and sync FET role is exchanged under positive cycle and negative cycle, the related PWM control signals are required to exchange also, which can be support by the DB submodule of Type 4 ePWM directly. As shown in Figure 1-8, S6 and S7 are used to swap ePWMxA and ePWMxB output. And the added red arrows also indicate the detailed settings inside the DB submodule.

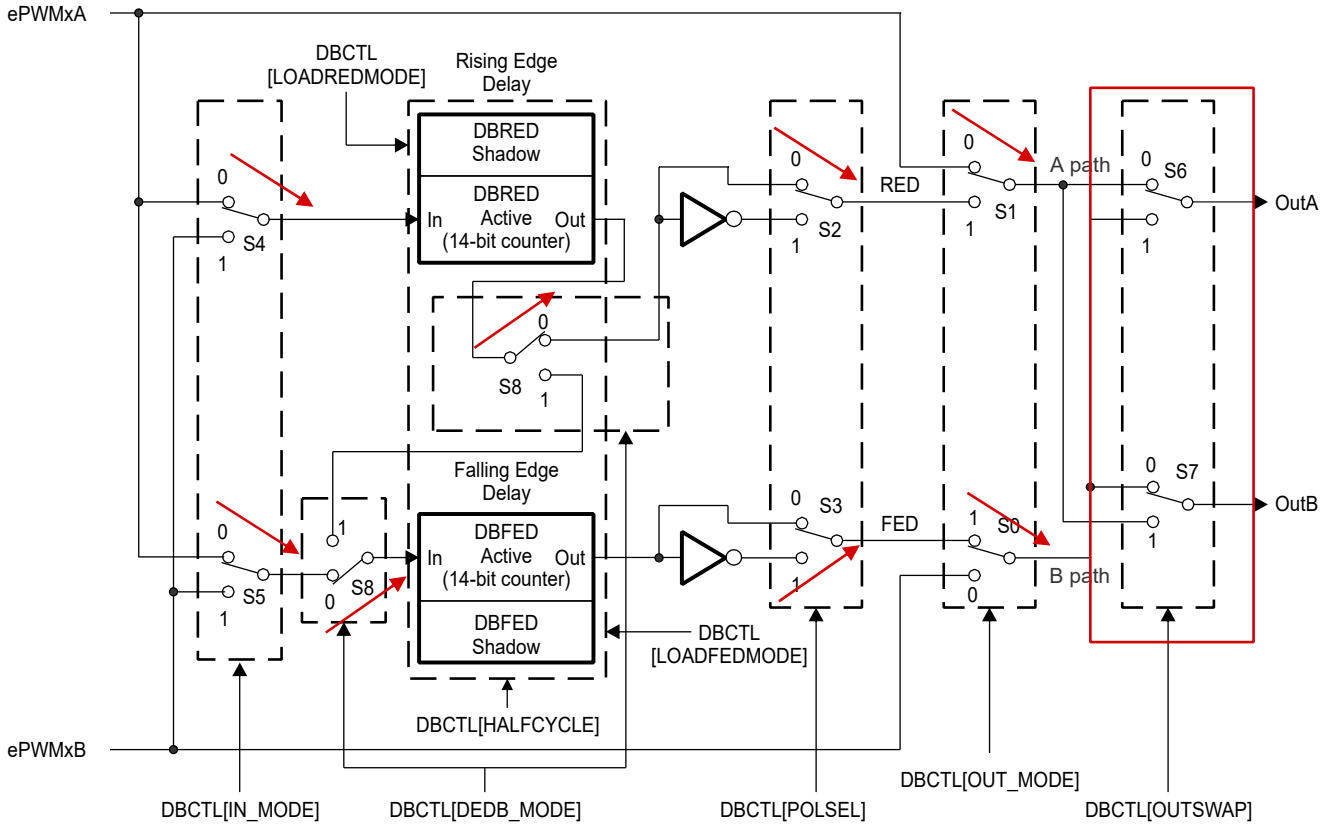

Figure 1-8. Dead Band Submodule Block Diagram

In order to better demonstrate how to leverage the T1 event together with CMPSS for the totem pole PFC configurations, the below example codes are provided. In this example, CMPSS1_H is selected as the source for TRIP4 input through ePWM X-Bar. Note that only the T1 event related configurations are shown, and other ePWM settings can refer to the example projects in C2000WARE.

```
    XBAR_setEPWMMuxConfig(XBAR_TRIP4, XBAR_EPWM_MUX00_CMPSS1_CTRIPH);
    XBAR_enableEPWMMux(XBAR_TRIP4, XBAR_MUX00);

    // assign DCAL for TRIP4
    EPWM_selectDigitalCompareTripInput(base,EPWM_DC_TRIP_TRIPIN4,EPWM_DC_TYPE_DCAL);

    EPWM_setTripZoneDigitalCompareEventCondition(base,EPWM_TZ_DC_OUTPUT_A2,EPWM_TZ_EVENT_DCXL_HIGH);

    // DCAEVT2 = DCAEVT2 (not filtered)

    EPWM_setDigitalCompareEventSource(base, EPWM_DC_MODULE_A,
                                      EPWM_DC_EVENT_2,
                                      EPWM_DC_EVENT_SOURCE_ORIG_SIGNAL);

    // Select DCAEVT2 event as AQ T1 source
    EPWM_setActionQualifierT1TriggerSource(base, EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_2);

    // This is to avoid impact of high impedance state
    EPWM_setTripZoneAction(base, EPWM_TZ_ACTION_EVENT_DCAEVT2, EPWM_TZ_ACTION_DISABLE);

    //During the normal condition
    EPWM_setActionQualifierAction(base,EPWM_AQ_OUTPUT_A,EPWM_AQ_OUTPUT_HIGH,
EPWM_AQ_OUTPUT_ON_TIMEBASE_ZERO);
    EPWM_setActionQualifierAction(base,EPWM_AQ_OUTPUT_A,EPWM_AQ_OUTPUT_LOW,
EPWM_AQ_OUTPUT_ON_TIMEBASE_UP_CMPA);
    //set T1 action for EPWM1A during CBC protection
   EPWM_setActionQualifierAction(base,EPWM_AQ_OUTPUT_A,EPWM_AQ_OUTPUT_LOW,
EPWM_AQ_OUTPUT_ON_T1_COUNT_UP);
```

2 How to Better Use the CMPSS for Totem Pole PFC

As discussed in Section 1, it is required to detect both the reverse current and the overcurrent events for totem pole PFC, so CMPSS can be used to save the external comparator circuits. In order to use the minimum CMPSS amount, the diagram in Figure 2-1 shows how to use one CMPSS for single phase totem pole PFC. The inductor current is routed to both high side comparator CMPSS1_H and low side comparator CMPSS1_L, while CMPSS1_H is for overcurrent detection, and CMPSS_L for reverse current detection.

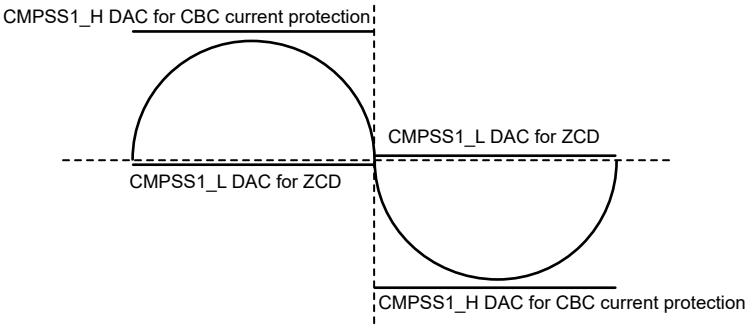

Figure 2-1. CMPSS Configurations

As for overcurrent protection for both positive cycle and negative cycle, it is required to change the DAC value with different thresholds at the zero-crossing point. In addition, to select one of DCxEVT1/2 events as the T1 source, specific high or low level effective should be defined for the CMPSS1_H output. During the positive cycle, when the overcurrent event occurs, the output of CMPSS1_H is high level effective, while in the negative cycle, the output of CMPSS1_H is low level effective. To address this, the CMPSS1_H output could be inverted with the COMPCTL[COMPHINV] register in the negative cycle so as to keep the same high level effective logic for the protection scheme regardless of the VAC polarity.

As for the reverse current detection, note that the reverse current is always in the opposite polarity of the VAC waveform, which is the negative current spike at the positive cycle, and the positive current spike at the negative cycle. Therefore, similar with the CMPSS1_H configurations, it is also required to change the DAC value and invert the output polarity in the negative cycle for CMPSS1_L.

For totem pole PFC, during the zero-crossing point, there exists a dead time when all the PWM signals shut down, so it is safe and also suggested to change the DAC value and output polarity of CMPSS during that time. According to the device-specific data sheet, the CMPSS DAC settling time is within 1 µs, which is fast enough to handle any change.

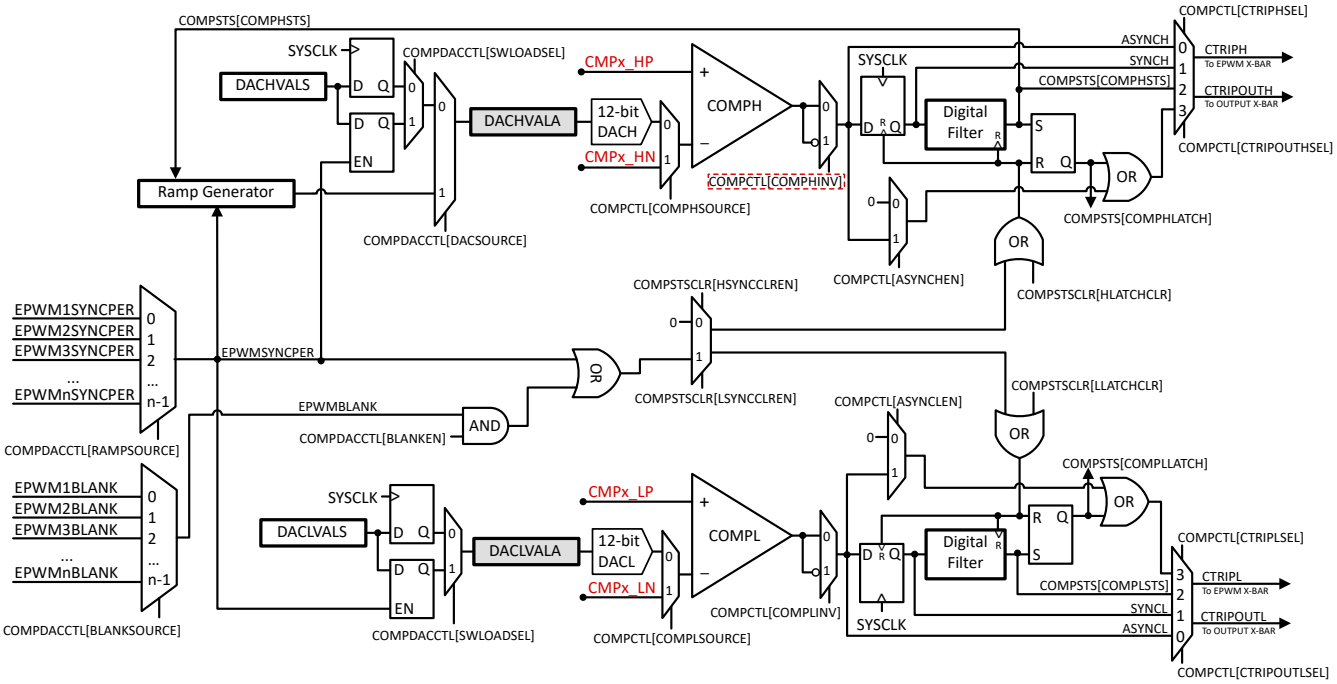

Figure 2-2. CMPSS Module Block Diagram

3 How to Control the Slow Frequency MOSFETs

Generally, to further improve efficiency, MOSFETs will be used as the slow frequency FETs (driven at grid frequency, normally 50Hz or 60Hz), due to lower conduction loss compared to diodes, as shown as Q3 and Q4. Since it is driven at grid frequency, with always high or low state, some users might select GPIO to control the slow frequency MOSFETs. However, for the reliability consideration, it is still suggested to use ePWM output as the control signals, so that the fast protection response could be ensured for the MOSFETs during the fault conditions. Otherwise, the delay caused by the ISR to set low status for the GPIO might pose risks to the system.

To simplify the configuration, the continuous software force action of the AQ submodule can be used. For example, if using ePWMxA for Q3 and ePWMxB for Q4, in the positive cycle, the below settings can be applied.

```
EPWM_setActionQualifierContSWForceAction(base, EPWM_AQ_OUTPUT_A, EPWM_AQ_SW_OUTPUT_LOW);
EPWM_setActionQualifierContSWForceAction(base, EPWM_AQ_OUTPUT_B, EPWM_AQ_SW_OUTPUT_HIGH);
```

Note that when enabling the actions with TZ submodule for the slow frequency MOSFETs during fault conditions, one-shot trip mode should be used instead of CBC mode, since generally the MOSFETs selected for the slow frequency FETs are not suitable for hard switching conditions. Besides, after trip low with one-shot mode, the TZ flags could be cleared at the next zero-crossing point so as to enable the slow frequency MOSFETs with the least effect for the system.

4 How to Implement Reliable Zero-Crossing Detection

As discussed in *How to reduce current spikes at AC zero-crossing for totem-pole PFC*, it is critical to implement the soft-start scheme for Q1~Q4 during the zero-crossing point to reduce the current spike and improve THD. Before that, accurate and reliable AC voltage zero-crossing detection is most important. In the reference designs, *Design Guide: TIDM-2008/TIDM-1007 - Bidirectional Interleaved CCM Totem Pole Bridgeless PFC Reference Design Using C2000™ MCU* or *Design Guide: TIDA-010203 - 4-kW, Single-Phase Totem Pole PFC Reference DesignWith C2000 and GaN*, software phase-locked loop (SPLL) is leveraged to detect the zero-crossing point with the voltage phase information. As a low-pass filter, SPLL is a good method to avoid the error caused by the sensing voltage noise or spike. However, if the actual applications need to support the step change of the AC frequency, SPLL could not provide the expected performance due to the calculation delay. Thus, it is still necessary to understand how to achieve accurate zero-crossing detection with the pure voltage sensing circuits using ADC.

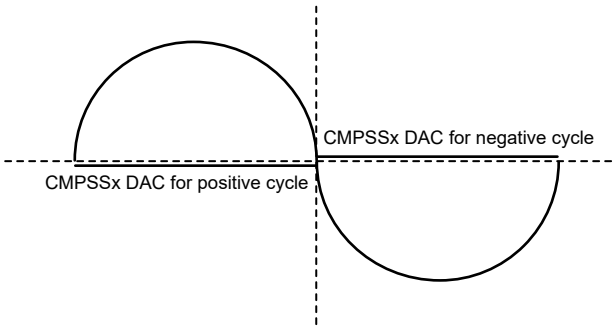

Figure 4-1. CMPSS Used for Vac Sensing

As shown in Figure 4-1, CMPSSx is suggested to enable for the Vac sensing signal, with the DAC threshold set closed to 0. With the help of the CMPSS, it is possible to shut down all the switches controlled by ePWM modules as soon as the AC polarity changes without any software delay. During the normal operation, it can naturally provide the dead time before the zero-crossing point when the soft-start scheme starts to implement, as discussed in *How to reduce current spikes at AC zero-crossing for totem-pole PFC*.

In the actual applications, the rectifier diodes are also added to bypass surge current. The most critical issue during the surge test is that, for example during the positive cycle, when the reverse surge energy forces the AC voltage polarity from positive to negative for a short time, the AC source will be in short circuits since Q4 keeps the on state as in the positive cycle, as shown in Figure 4-2. Thus, with the CMPSSx enabled for Vac sensing, it will turn off Q4 so as to avoid the short circuit condition within 55ns, which minimizes the risk of the damage to the power stage. During the normal conditions, turning off the switches when the AC voltage goes through the threshold voltage during the zero-crossing point is also unexpected. In addition, it is also helpful when testing with non-sinusoidal AC voltage input, even with square wave type AC input.

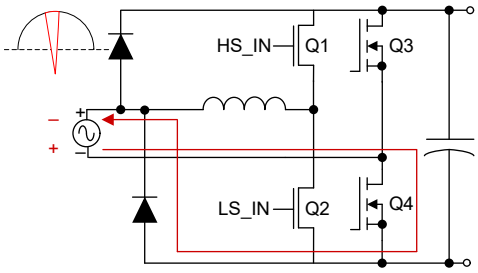

Figure 4-2. Short Circuit Issue During the Surge Test

5 How to Implement 2 Phase Interleaved Control

When the power rating increased, interleaved topologies are common to selected, for better thermal design and ripple current performance. Therefore, 2 phase interleaved totem pole PFC is also popular in high power applications. In *Leverage New Type ePWM Features for Multiple Phase Control*, it showed flexibility of the phase register TBPHS when configuring the phase shift relationship among different ePWM modules, but since TBPHS does not provide the shadow mode, cares should be taken when the switching frequency changes with a large step. For CCM mode totem pole PFC, it uses fixed frequency normally, it is fine to enable the phase register for 2 phase interleaved configurations. In this document, another more simplified scheme is discussed, which is helpful to implement the frequency dithering feature for the EMI optimization.

As shown in Figure 5-1, ePWM1 and ePWM2 are used as the example, representing the control modules for the master phase and the slave phase, respectively. Instead of using the phase shift register, both ePWM modules share the same time base. Different from the PWM configurations in Section 1, up-down count mode is used, and the duty cycle for the active FET is centralized with the Period event for the master phase (Phase 1), while it is centralized with the ZERO event for the slave phase (Phase 2). With such design, the 180° phase shift is achieved naturally. Another benefit is that, if the switching frequency is required to change, for example, for the frequency dithering function, the register linking scheme with the EPWMXLINK register can ensure the period registers of different ePWM modules are written simultaneously.

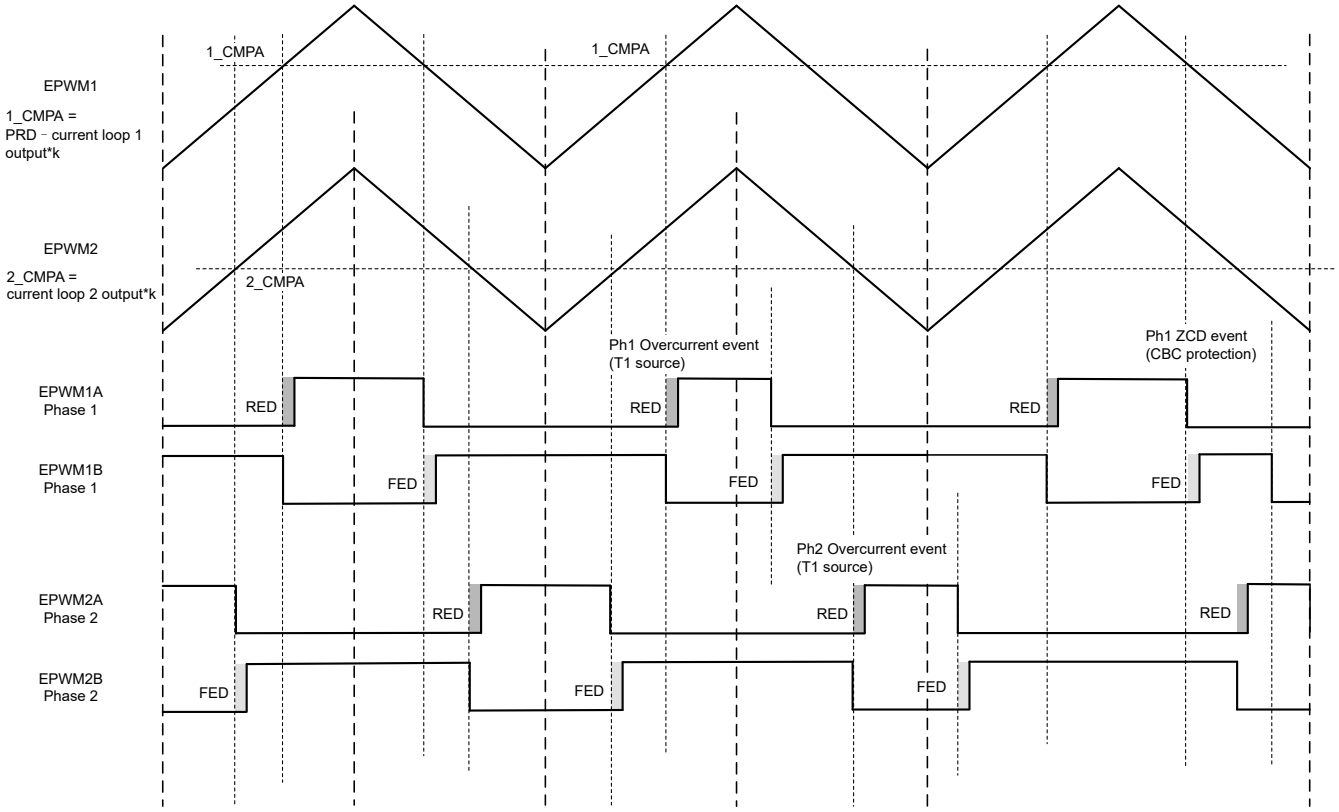

Figure 5-1. Phase Interleaved Totem Pole PFC ePWM Configurations

6 References

- Texas Instruments: *Control challenges in a totem-pole PFC*
- Texas Instruments: *How to reduce current spikes at AC zero-crossing for totem-pole PFC*
- Texas Instruments: *Leverage New Type ePWM Features for Multiple Phase Control*
- Texas Instruments: *TMS320F28003x Real-Time Microcontrollers Technical Reference Manual*
- Texas Instruments: *Design Guide: TIDM-2008/TIDM-1007 - Bidirectional Interleaved CCM Totem Pole Bridgeless PFC Reference Design Using C2000™ MCU*
- Texas Instruments: *Design Guide: TIDA-010203 - 4-kW, Single-Phase Totem Pole PFC Reference DesignWith C2000 and GaN*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265