Application Note

AM62x SiP Escape Routing for PCB Design

ABSTRACT

This document is intended to provide a reference for escape routing on the AM62xSiP device.

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Trademarks

1 Introduction

The AM62xSiP is an extension of the low-power, low-cost Sitara Industrial/Auto grade family of process. The AM62xSiP is based on the Cortex-A53 microprocessor, M4F microcontroller with dedicated peripherals, 3D graphics acceleration, dual display interfaces, and extensive peripheral and networking options for a variety of embedded applications.The AM62xSiP is available in a 13-mm × 13-mm FBGA package with a 0.5-mm ball pitch. The package BGA design is built leveraging TI Via Channel Array Technology (VCA) technology, which enables package miniaturization while still utilizing low cost PCB routing rules. Via Channel Array (VCA) is built with careful considerations on escape routing to avoid costly High-Density Interconnect (HDI) and expensive Via technologies. This document is intended to provide a reference for escape routing on the AM62xSiP device. Care must be taken to route signals with special requirements such as DDR, high speed interfaces. Refer to the High-Speed Interface Layout Guidelines for more details. Details on Power Delivery Network are provided in AM62x PDN Application note and any routing and layout requirements specified in those documents supersede the generic requirements provided here.

2 Via Channel Arrays

Via Channel Array Technology has been successfully used in a variety of TI products that helps in minimizing package dimensions by using smaller ball pitch and utilizing low cost PCB routing. Via Channel technology is a way of enabling routing channels to escape innermost BGA positions. This allows several advantages. First, the via outside diameter (also known as the annular ring) can be larger than it normally would be if it had to be placed in between the BGAs in a tighter pitch, because all the vias are placed in special areas called *via channels*. This makes PCB manufacturing less expensive because larger vias are possible. Second, the vias are grouped in a radial pattern instead of a series of concentric rings around the middle of the chip, which is the case with normal BGA array PCB routing. The traces are more easily routed out of the inner parts of the chip because they are not restricted to the narrow paths in between many rows of vias. The unique outer row routing and the via channel inner routing are two important parts of this technology on the AM62xSiP. The AM62xSiP BGA Via Channel Array is shown in Figure 2-1.

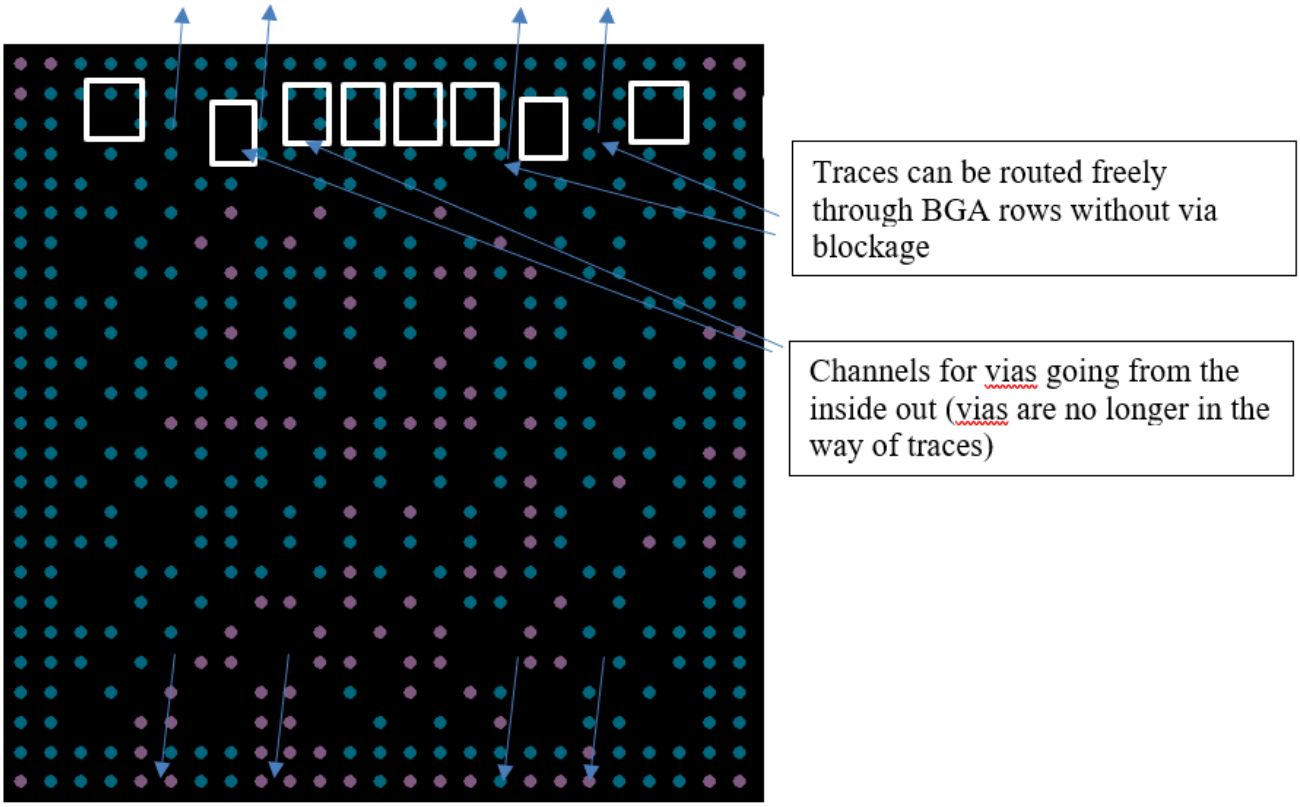

Figure 2-1. AM62xSiP BGA array with Via Channels

For the first two rows (from the outside in) of the BGA array, the balls have been arranged to allow wider traces than would otherwise be possible. The first row (the outside row) supports any size trace desired, because the trace comes from the PCB ball land and goes out on the PCB. Normally, the second row traces must be routed in between the first row of the PCB ball lands. On this package, the second row traces are routed through an open channel where the BGA ball has been removed to allow wider traces. The AM62xSiP parts allow a 3.2 mil trace/space in all areas, if routed correctly.

Figure 2-2 shows the first two rows of the AM62xSiP package and how it is possible to route large 3.2 mil (mm) traces and spaces in the areas of removed balls.

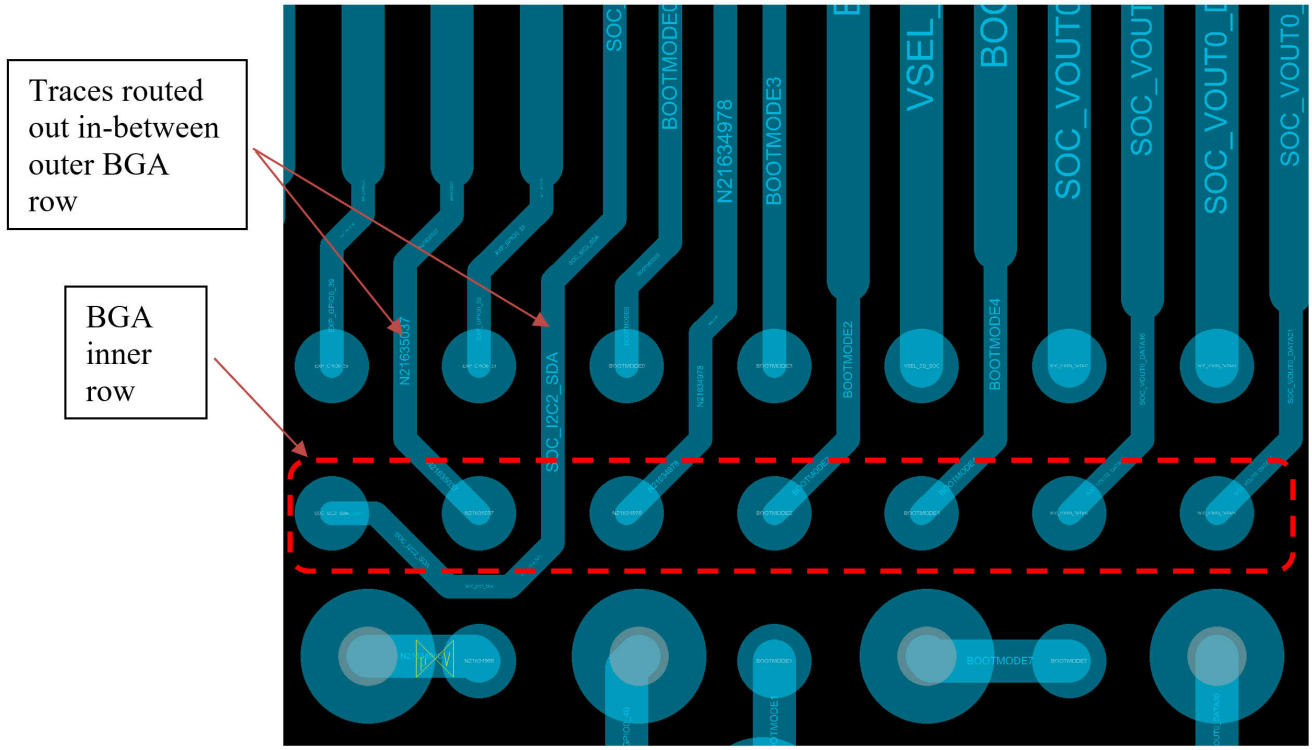

Figure 2-2. Outer Rows of Traces

Starting at the third row, as with any BGA package, vias are necessary. As stated before, the vias are gathered in the via channels, so the only vias that need to be placed in between balls are some of the power vias in areas of ground or power copper pour. In this case, they have no regular via ring since they are located in an area of copper pour where all the surrounding balls share the same net. This is elaborated more in the later section with details on via sharing. Because the via ring is larger than one that would normally fit in between these balls with the required clearance, the layout tool may flag a design rule check (DRC) error, however, this is a false warning since there is no risk of shorting to a nearby pad because they are all on the same net. The rest of the vias need to be placed into the via channels as shown below. Figure 2-3 shows how the vias are grouped in the via channels.

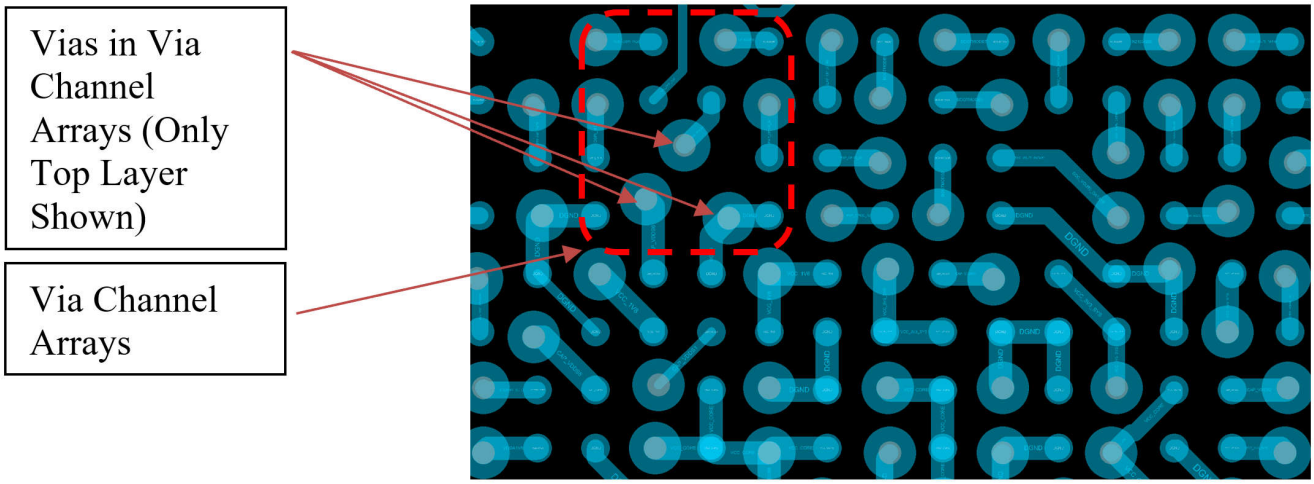

Figure 2-3. Vias in Via Channels

3 Width/Spacing Proposal for Escapes

The AM62xSiP Via channel array solution has been designed to support the following. The AM62xSiP package supports similar feature set as several other competition solutions with approximately 15% smaller package area and ~10% wider line width. This solution therefore, reduces PCB foot print and utilizes lower cost PCB rules enabling compact and low-cost systems.

Table 3-1. Width/Spacing Proposal for Escapes

PCB Feature	PCB Routing Requirements	Comments
Minimum via diameter	18 mils	Via pads dia - 18 Mils
Via hole size	8 mils	Via hole dia - 8 Mils
Minimum trace width/spacing required in the BGA breakout (Inner Layer)	Trace Width - 3.2 Mils	
	Spacing - 3.2 Mils	
Minimum trace width/spacing required in the BGA breakout (External Layer)	Trace Width - 3.2 Mils	
	Spacing - 3.2 Mils	
Number of layers used for escape	4 Layers	Top
		Ground
		Power
		Bottom
BGA land pad size	12 Mils	
Package Size	13 mm x 13 mm	
PCB layers (signal routing, total) recommended	(2, 4) Layers	Top
		Ground
		Power
		Bottom

4 Stackup

PCB stack-up is one of the first and important considerations in realizing a successful PCB. The AM62xSiP device supports a BGA array of 25 × 25 with a 0.5-mm pitch and a body size of 13 mm. Due to the number of rows of signal balls around the periphery, TI recommends two routing layers. PDN compliance and robustness is critical to meet all the performance objectives of the device and associated peripherals. To enable this, TI recommends allocating two layers for power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High speed interfaces such as CSI, USB require ground planes for impedance matching. The escapes on the AM62xSiP board was achieved with 4 layers, as shown below.

Table 4-1. Example PCB Layer Stack-up

PCB Layer	Layer Routing, Planes or Pours
Layer 1	Component pads and signal routing
Layer 2	Ground
Layer 3	Power
Layer 4	Signal Routing

The AM62xSiP board is implemented without HDI (High Density Interconnect) and does not use micro vias, which are both intended to save board cost. All vias on the AM62xSiP board are Plated Through Hole (PTH) and pass completely through the board. Proper analysis shall be performed to validate both signal and power integrity, if further optimizations are required to reduce PCB stack-up and/or routing rules illustrated in this document.

5 Via Sharing

The Via Channel Array BGA pattern implemented on the AM62xSiP design offers several opportunities for via sharing. Vias are shared across BGA pins. Figure 5-1 and Figure 5-2 show the via sharing opportunities for VDD_CORE and VSS power supplies, respectively. Via sharing across BGA pins provides for easier escape routing and robust electrical connection by connecting multiple pins.

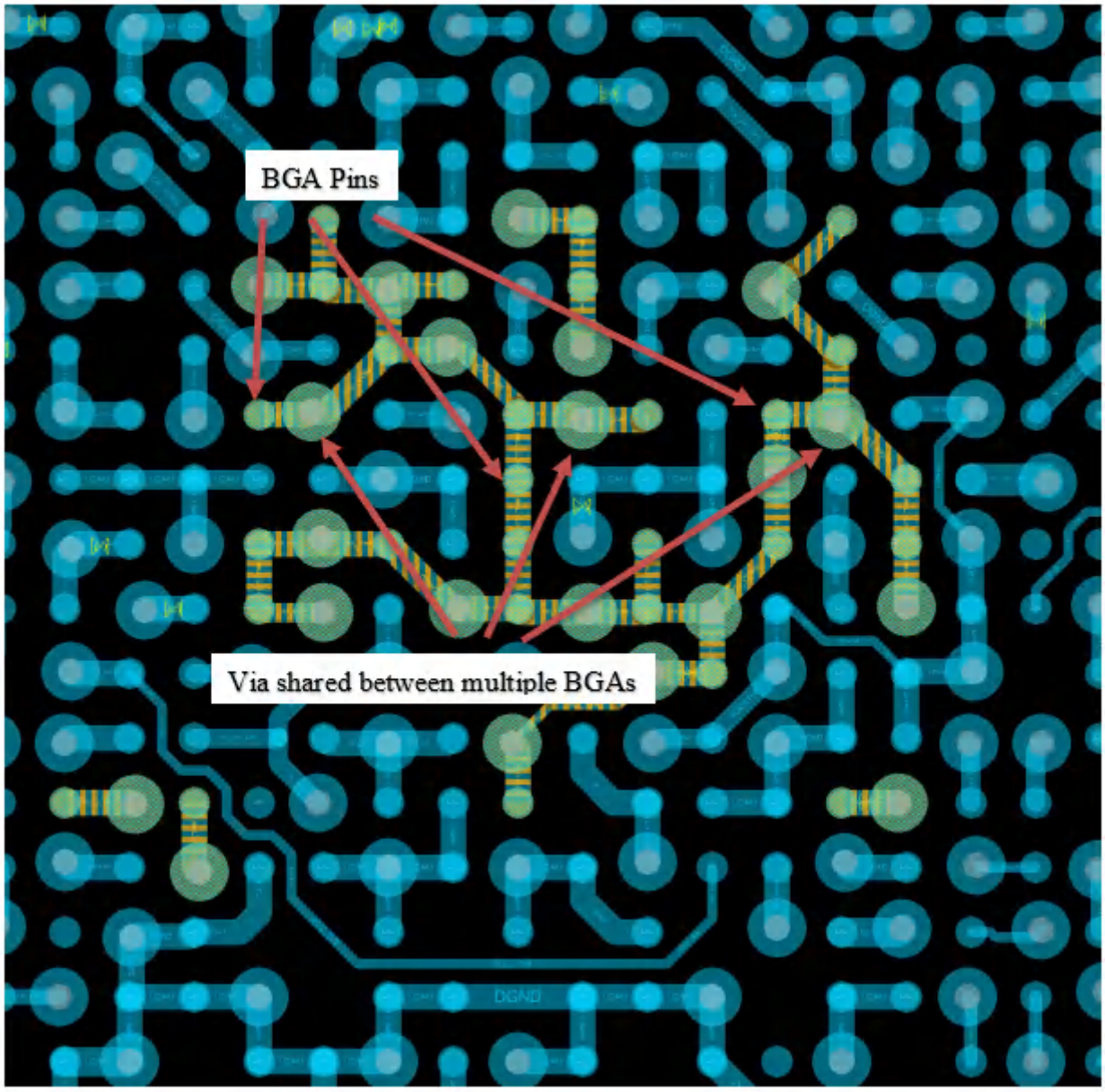

Figure 5-1. Via Sharing for VDD_CORE Domain

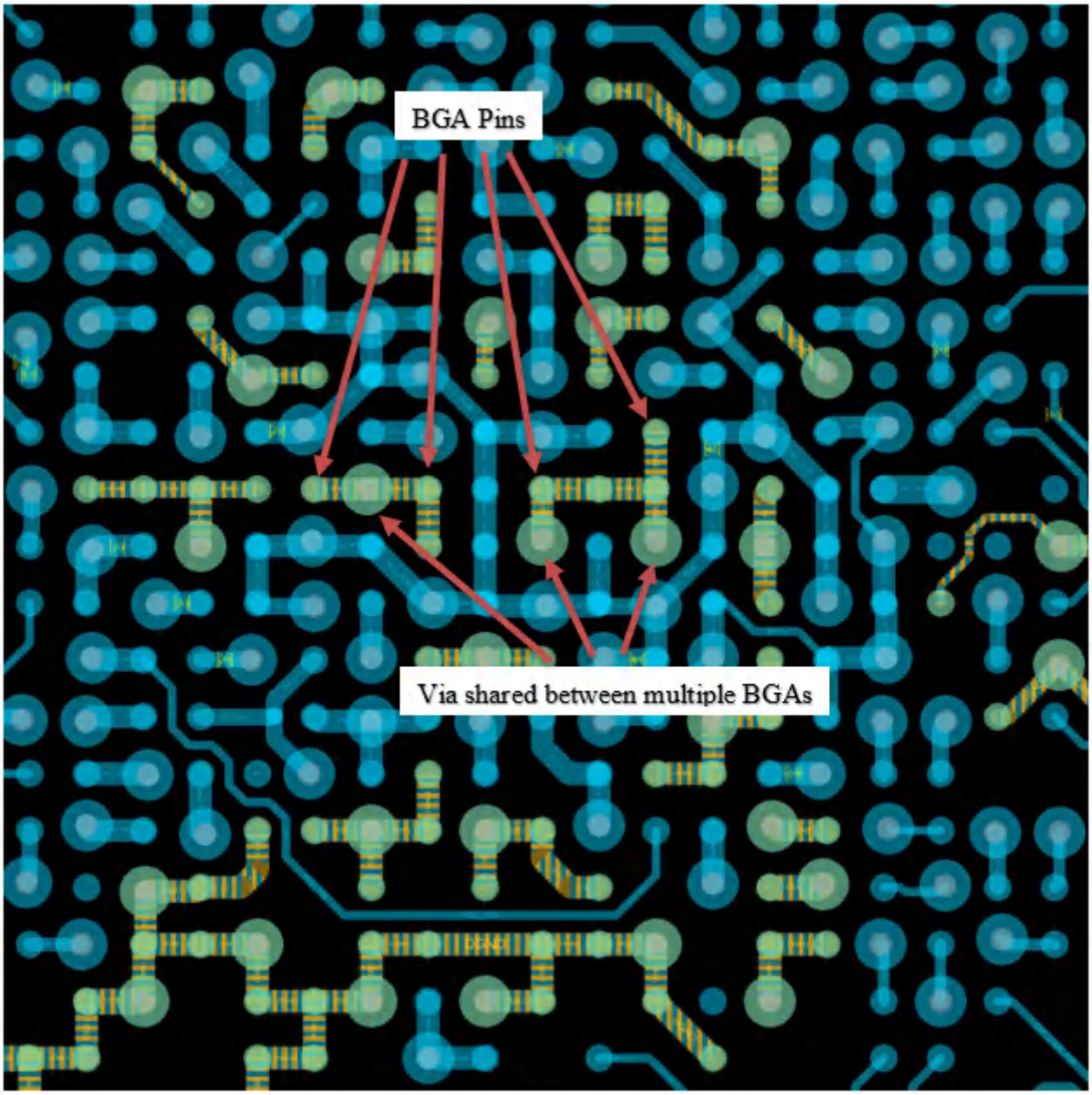

Figure 5-2. Via Sharing for VSS

6 Floorplan Component Placement

Careful analysis is required to analyze the locations of the interfaces used on the device and the associated components and connectors. Optimum trace routing will have routes as short as possible with a minimum cross-over. The AM62xSiP offers interface selection flexibility through pin-mux choices. Pin-muxing enables a same interface function made available on multiple pins and is selectable through a pin mux option. Favorable pin-mux options that ease PCB routing and component placement can be fully utilized to further optimize the PCB design. The figure below shows the default arrangement of the signal balls and the power and ground balls. Priority is given to component placements without pin-mux options such as CSI, USB, OLDI/LVDS, and so forth.

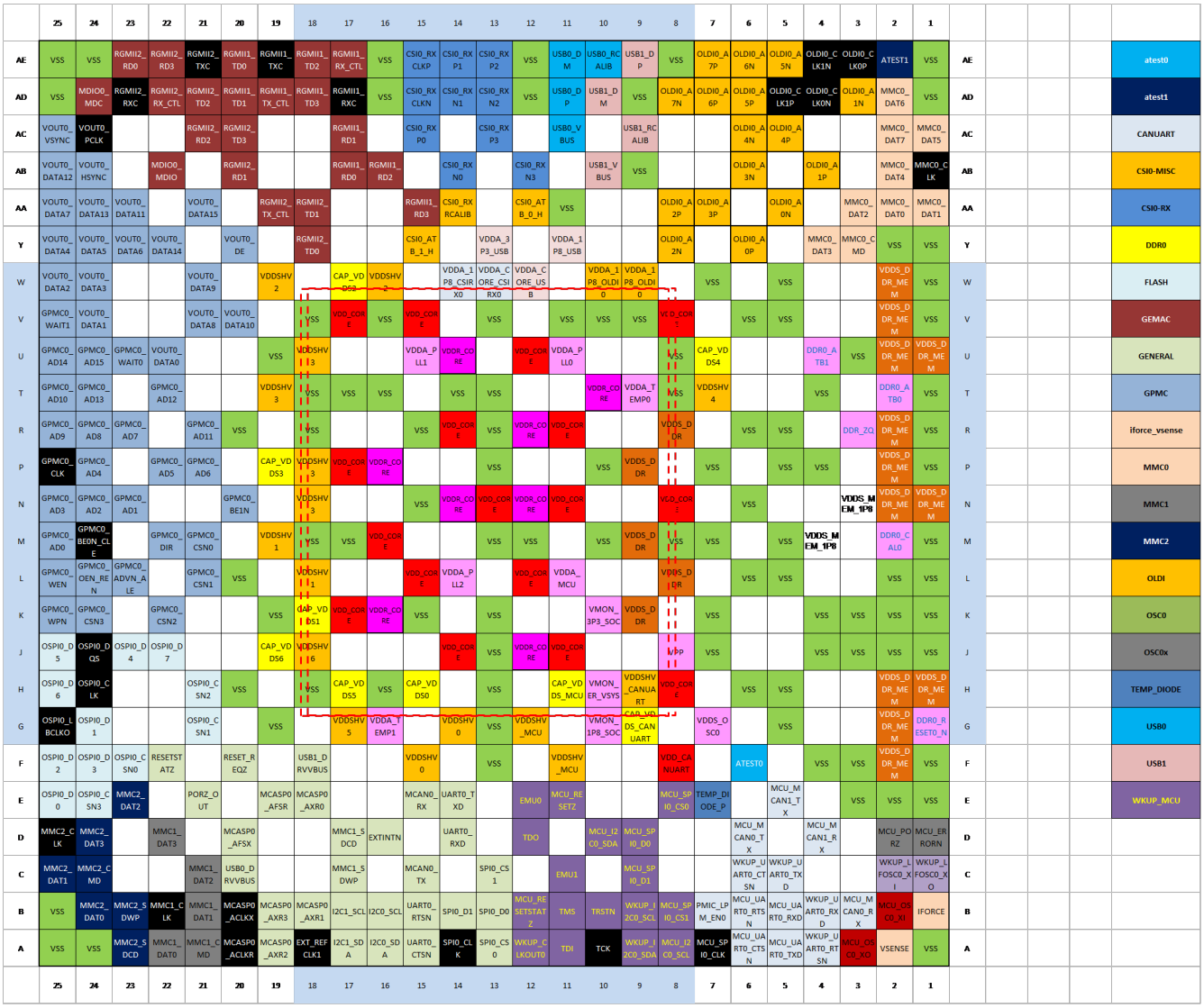

Figure 6-1. AM62xSiP Floorplan

7 Critical Interfaces Impact Placement

Placement of the AM62XSIP device and some of the components or connectors is also dictated by some of the highest performance interfaces such as CSI, USB, and so forth. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

8 Routing Priority

As indicated earlier, critical interfaces affect component placement options. The next step in PCB design is to prioritize routing to these critical interfaces. Those with higher priority must be completed before implementing those of lower priority. It is imperative to route interface with the higher priority first. PCB layout teams often end up in a time intense, iterative process with sub optimal results when routing priorities are not established.

The table below lists a recommended priority order for interfaces contained on the AM62XSiP family of devices. Individual design requirements may drive a need for adjustment of the priorities but this serves as a good baseline and has been used for the board example illustrated in this document.

Table 8-1. Routing Priority

Interface	Routing Priority
CSI	10 (Highest Priority)
OLDI	9
OSC	8
USB2, OSPI	8
Power distribution	7
RGMII	6
eMMC	5
Clocks	5
MII / RMII	4
SPI	4
Motor control	4
Analog	3
GPMC	2
GPIO	1
UART / CANUART	1
I2C / Temp Diode	1 (Lowest Priority)

The multi-gigabit Camera Serial Interfaces (CSI) are the most critical due to their data rate and loss concerns. CSI is at the top of the priority list because it is very sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the CSI connector and the AM62XSiP device. CSI signals are found on the outer layers of the BGA footprint allowing some of the CSI traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. The one surprise may be power distribution. It is often left to last. This then results in poor decoupling performance or current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.**

9 SerDes Interfaces

The package BGA ball map is also arranged to support routing the highest priority interfaces first. Therefore, the SerDes CSI interfaces are located on the outer two rings. The differential receive pair should be routed away from the SoC on the top layer leaving a gap without blocking vias. The lanes located on inner BGA rows require vias to escape as a differential pair on the bottom or on an interior layer. The VCA facilitates this for inner rows. See Figure 9-1 for an example of the escape of the SerDes signals on the AM62XSiP board on the top layer and on an inner layer. Wide traces can limit the signal loss but could violate the impedance requirements. For more detailed information on routing Serdes signals, refer to High-Speed Interface Layout Guidelines.

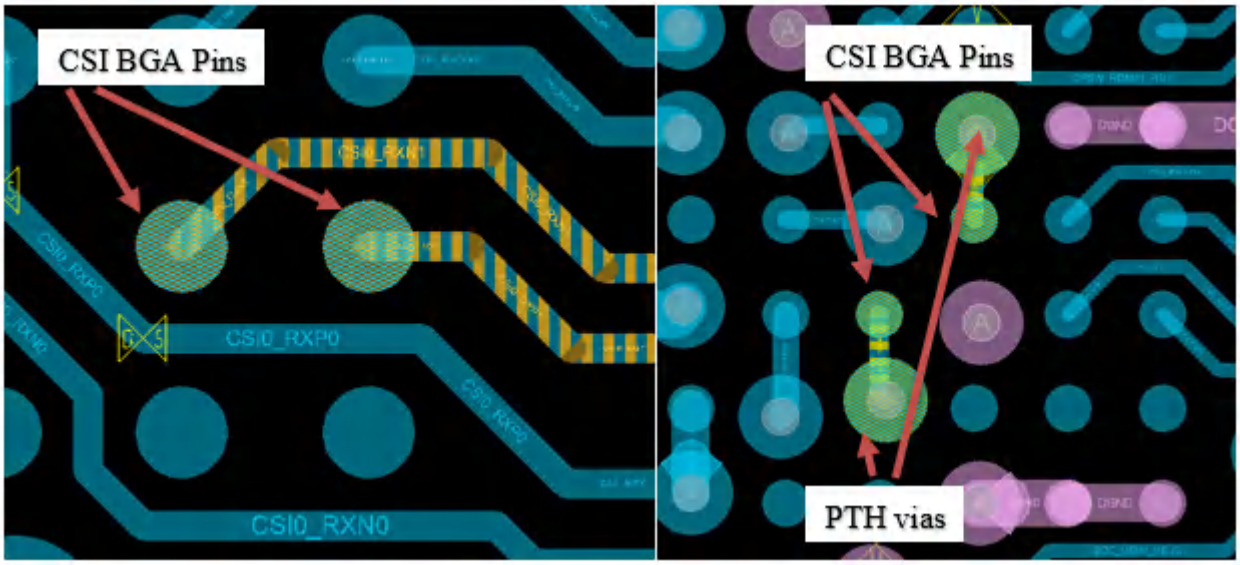

Figure 9-1. Serdes CSI Escapes for TOP Layer (Left) and Inner Layer (Right)

10 Power Decoupling

The middle priority interfaces and the power distribution planes and pours would be routed next after the SerDes interfaces. It is strongly encouraged to complete all SerDes routing before continuing with other interfaces. The power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SerDes routes, as these can influence the return currents for the high-speed interfaces. The highest speed source-synchronous interfaces, such as RGMII and QSPI, may also require simulation, so these may need to be completed at this time as well.

Special care is needed for the 1-uF output capacitors connected to the CAP_VDDS* BGA pins on the AM62XSiP device. These capacitors should be placed as close to the pin as possible, and a low inductance path should be present between the CAP_VDDS BGA pin and the supply pad on the capacitor. The layout used on the CAP_VDDS0 net on the AM62XSiP SK EVM is shown in Figure 10-1. Note the sharing of the GND pad of the capacitor with other capacitors in the vicinity, which allows saving routing resources. Also, it is important to keep the PTH vias for the capacitor power and GND pad connections as close to each other as possible to minimize the loop inductance.

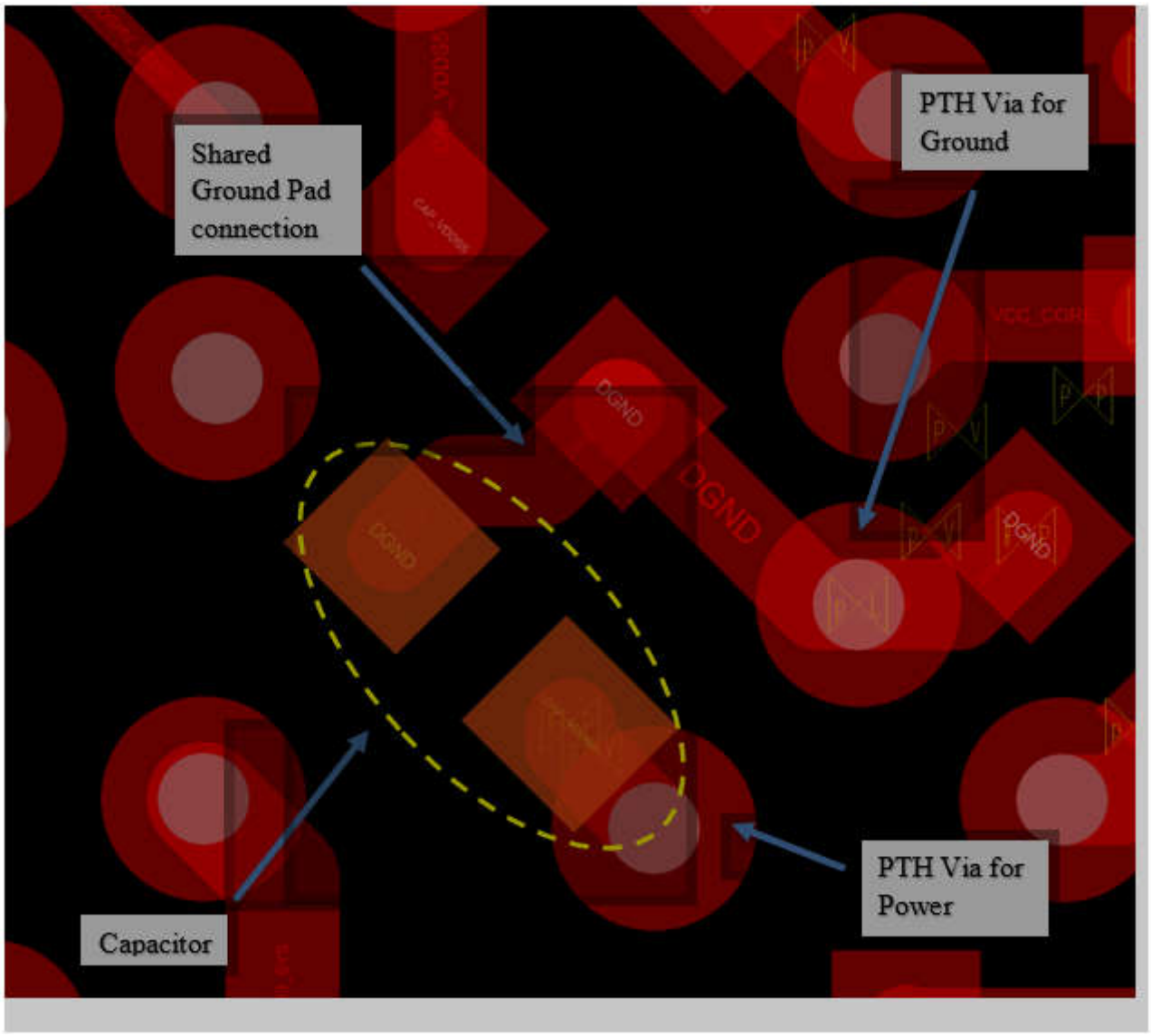

Figure 10-1. AM62XSiP SK EVM Output Capacitor Placement for CAP_VDDS0

This placement can be improved if the capacitors can be placed directly under the SoC. The decoupling capacitors for the VDD_CORE supplies should also receive the same priority as those on the CAP_VDDS* pins

and should be placed under the socket, with minimum inductance connections to the respective BGA pins on the AM62XSiP device.

11 Route Lowest Priority Interfaces Last

When the length matching and simulations have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and then the lower priority interfaces.

12 Summary

The via channels have been carefully co-designed to ensure escapes for all signals and power while meeting the respective signal and power integrity goals for each interface. A summary of all via channel arrays and vias for the different power supply nets is shown in Table 12-1.

Table 12-1. Via Channel Summary

Net	#Pins	#Vias for BGA Escape
VDD_CORE	17	21
VDDR_CORE	8	
VDD_CANUART	1	
VDDA_CORE_USB	1	
VDDA_CORE_CSIRX0	1	
VDDS_DDR	5	2
VDDS_DDR_MEM	12	5
VDDSHV0	2	8
VDDSHV2	2	
VDDSHV3	4	
VDDSHV_MCU	2	
VDDSHV_CANUART	1	
VDDA_3P3_USB	1	
VMON_3P3_SOC	1	
VDDSHV1	2	3
VDDSHV4	1	
VDDSHV6	1	
VMON_1P8_SOC	1	
VDDSHV5	1	1
VDDS_OSC0	1	11
VDDA_TEMP[0:1]	2	
VDDA_PLL[0:2]	3	
VDDA_MCU	1	
VDDA_1P8_OLDI0	2	
VDDA_1P8_CSIRX0	1	
VDDA_1P8_USB	1	
VDDS_MEM_1P8	2	

A picture with AM62xSiP with all signals and power escaped is shown in Figure 12-1.

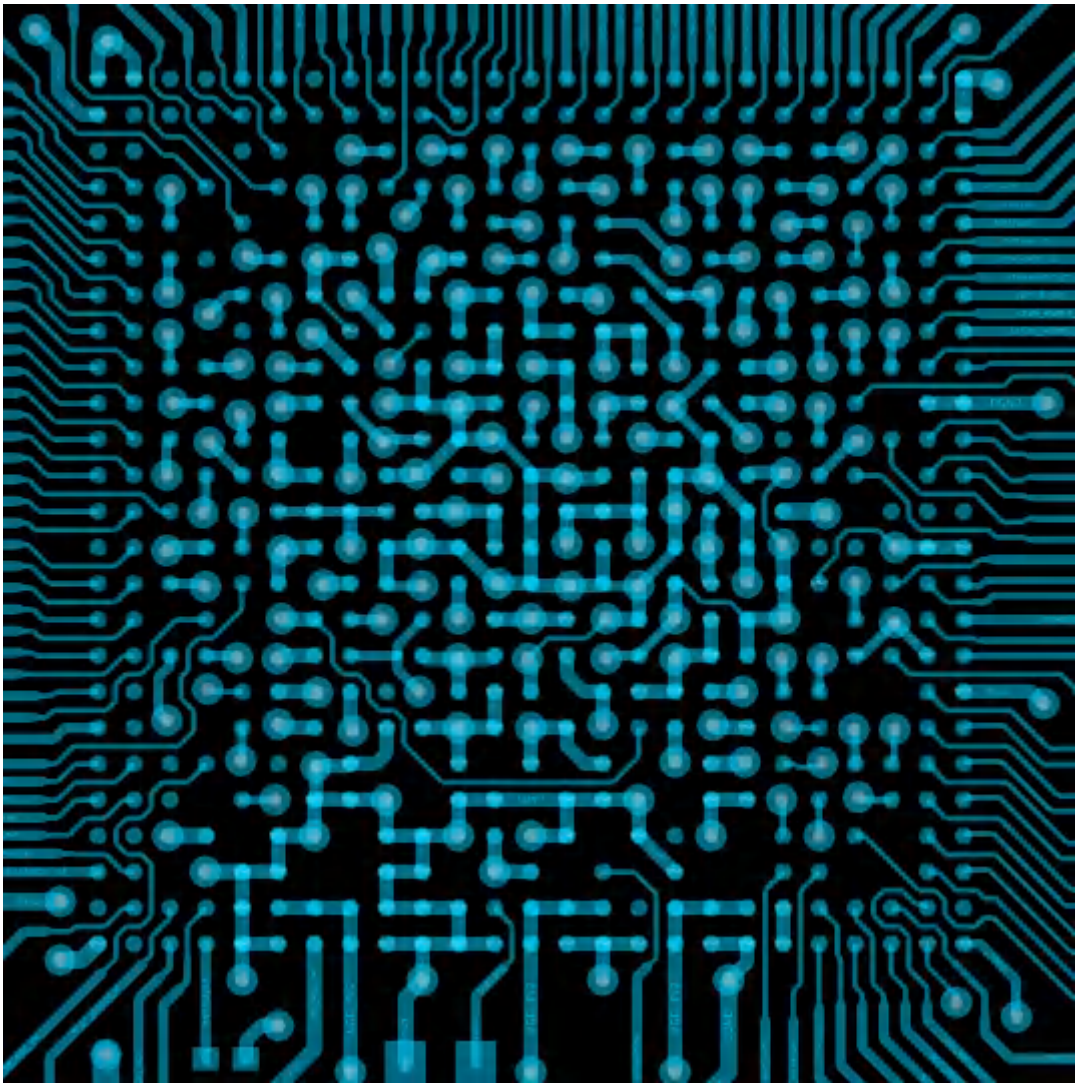

Figure 12-1. AM62xSiP with Complete Signal and Power Escapes

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