Application Note

AM26x Family Migration Overview

ABSTRACT

This application note describes the differences between the Texas Instruments' AM263, AM263P and AM261 microcontrollers to outline differences between devices, new features, and what needs to be considered when migrating from one AM26x device to another. Both hardware and software changes are covered for the purpose of application migration. This document provides a comprehensive list of feature differences for all AM26x microcontrollers. However, these details are kept at a feature level and specific information about the performance or usage of each feature can be found in the device-specific data sheets, technical reference manuals, or software user guides. Features that are identical between the devices are not included outside of the *Device Comparison* table.

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Trademarks

1 Feature Differences Between AM26x Devices

Device Comparison provides a feature-level comparison between the AM26x superset devices: AM2634, AM263P4 and AM2612.

Table 1-1. Device Comparison

Features	Reference Name	AM2634	AM263P4	AM2612
Processors and Accelerators				
Arm Cortex-R5F	R5FSS	4	4	2
Trigonometric Math Unit	TMU	No	Yes	Yes
Hardware Security Module	HSM	Yes	Yes	Yes
Crypto Accelerators	Security	Yes	Yes	Yes
Program and Data Storage				
On-Chip Shared Memory (RAM)	OCSRAM	Grade N: 1 MB Grade O/P: 2 MB	Grade N: 2 MB Grade O/P: 3 MB	Grade M, N: 1MB Grade L/O/P: 1.5MB
R5F Tightly Coupled Memory (TCM)	TCM	Up to 256KB(13)	Up to 512kB(14)	Up to 512kB
General-Purpose Memory Controller	GPMC	4MB	None	None(7) or 4MB
Peripherals				
Modular Controller Area Network Interface	MCAN	4	8	2
Full CAN-FD Support	MCAN	4	8	2
General-Purpose I/O	GPIO	Up to 139	Up to 140	Up to 141
Serial Peripheral Interface	SPI	5	8	2(7) or 4
Universal Asynchronous Receiver and Transmitter	UART	6	6	6
Local Interconnect Network	LIN	5	5	3
Inter-Integrated Circuit Interface	I2C	4	4	3
Analog-to-Digital Converter	ADC	3(1) or 5(2)	3(3) or 5(4)	2(7) or 3(10)
Resolver (ADC12B3M)	RDC	None	0(11) or 2(12)	None
	ADC	None	0(11) or 2(12)	None
Comparator Modules	CMPSS	12(1) or 20(2)	12(3) or 20(4)	9
Digital-to-Analog Converter	DAC	1	1	1
Programmable Real-Time Unit Subsystem(5)	PRU-ICSS	0 or 1	0 or 1	2(9)
Industrial Communication Subsystem Support(6)	PRU-ICSS	Optional	Optional	Optional
Gigabit Ethernet Interface	CPSW	2	1(12) or 2(11)	1
Multi-Media Card/Secure Digital Interface	MMCSD	1	1	0(8) or 1
Enhanced High-Resolution Pulse-Width Modulator Module	EHRPWM	16(1) or 32(2)	16(3) or 32(4)	10
Enhanced Capture Module	ECAP	5(1) or 10(2)	8(3) or 16(4)	2
Enhanced Quadrature Encoder Pulse Module	EQEP	2(1) or 3(2)	2(3) or 3(4)	2
Sigma Delta Filter Module	SDFM	1(1) or 2(2)	1(3) or 2(4)	0(7) or 2
Fast Serial Interface	FSI	4x FSI_RX + 4x FSI_TX	4x FSI_RX + 4x FSI_TX	1x FSI_RX + 1x FSI_TX
Quad / Octal SPI Flash Interface	QSPI / OSPI	QSPI	OSPI(15)	OSPI(15)
Real Time Interrupt	RTI	4	8	4
Windowed Watchdog Timer	WWDT	4	4	4

(1) Standard Analog configuration for AM263 contains 3x ADC, 16x EHRPWM, 5x eCAP, 2x EQEP, 1x SDFM, 12x CMPSS
(2) Enhanced Analog configuration for AM263 contains 5x ADC, 32x EHRPWM, 10x eCAP, 3x EQEP, 2x SDFM, 20x CMPSS
(3) Standard Analog configuration for AM263P contains 3x ADC, 16x EHRPWM, 8x eCAP, 2x EQEP, 1x SDFM, 12x CMPSS
(4) Enhanced Analog configuration for AM263P contains 5x ADC, 32x EHRPWM, 16x eCAP, 3x EQEP, 2x SDFM, 20x CMPSS
(5) AM263/AM263P: Programmable Real-Time Unit Subsystem is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, M, or N. Refer to the Device Data sheet for a Nomenclature Description table for definition of all feature codes.
(6) AM263/AM263P: Industrial Communication Subsystem Support is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, M, or N. Refer to the Device Data sheet for a Nomenclature Description table for definition of all feature codes.
(7) AM261 ZNC Package does not provide the General-Purpose Memory Controller (GPMC) and only provides 2 SPI, 2 ADC, and 0 SDFM peripheral instances. The SPI instances available are SPI0 and SPI2. The ADC instances available are ADC0 and ADC2.
(8) AM261 ZNC and ZEJ Packages do not provide the MMCSD peripheral.
(9) AM261 ZNC and ZEJ Packages have limitation in PRU-ICSS pin out which limits certain features. Refer to the Device Data sheet for a PRU-ICSS GPIO Signal Descriptions table for a list of pins available and not available per package.
(10) AM261 ZCZ Package only offers six ADC channels per instance of the ADC peripheral for a total of 18 channels. All other package variants offer seven ADC channels per instance for a total of 14 or 21 channels.

(11) AM263P: Applies to devices in the ZCZ-C Package only and have a Special Features code of C. Refer to the Device Data sheet for a Nomenclature Description table for definition of all feature codes.
(12) AM263P: Applies to devices in the ZCZ-S Package only and have a Special Features code of F or S. Refer to the Device Data sheet for a Nomenclature Description table for definition of all feature codes.
(13) Each R5FSS cluster supports 128-KB of Tightly-Coupled Memory (TCM). When configured as Single-Core or Lockstep operating mode, individual cores can utilize the entire 128-KB of TCM memory, while in Dual-Core mode, each core can only utilize the designated half (64-KB TCM).
(14) Each R5FSS cluster supports 256-KB of Tightly-Coupled Memory (TCM). When configured as Single-Core or Lockstep operating mode, individual cores can utilize the entire 256-KB of TCM memory, while in Dual-Core mode, each core can only utilize the designated half (128-KB TCM).
(15) AM263P/AM261: The Octal SPI (OSPI) Flash Interface can support Quad SPI (QSPI) Flash devices. The differences between QSPI and OSPI are covered in Section 3.1.4.

2 Package Options

This section provides an overview of all package options available for AM261, AM263, and AM263P microcontrollers. All offered device packages are NFBGA. The ZCZ package is the pin-to-pin compatible package across all three devices. Additionally, AM263P has a ZCZ-F package variant that includes an internally connected Silicon In Package (SIP) OSPI Flash device with 64Mb memory space.

Table 2-1. Package Options

Package Name	Pin Count	Dimensions	Pitch	AM263	AM263P	AM261	Notes
ZCZ (AM263, AM261) ZCZ-C (AM263P)	324	15mmx15mm	0.8mm	X	X	X	Pin-to-pin Compatible package across devices
ZCZ-F	324	15mmx15mm	0.8mm		X		Flash-on-Package
ZCZ-S	324	15mmx15mm	0.8mm		X		
ZFG	204	13.25mmx13.25mm	0.65mm			X	
ZNC	293	10mmx10mm	0.5mm			X	
ZEJ	256	13mmx13mm	0.8mm			X	

3 Feature Differences Between AM263 and AM263P

3.1 Feature Differences for System Consideration

This section outlines the differences and additions to modules when moving from AM263 to AM263P.

3.1.1 New Features in AM263P

3.1.1.1 Resolver Peripheral

Certain variants of the AM263P comes with a Resolver peripheral that provide two Resolver to Digital Converters (RDC) with dedicated ADCs. This feature is included in AM263P devices available in the ZCZ-S package and has a special feature code of F or S. For details about feature codes, see the *Device Naming Convention table* in the device-specific data sheet.

The Resolver to Digital Converter can process incoming digital data from ADCs to estimate the angle of the rotor and the angular velocity. The RDC is able to generate excitation sine PWM at frequencies of 5, 10, and 20kHz (with configurable amplitude and phase) and synchronizes sampling across sine or cosine channels. Offset, gain, and phase corrections, demodulation, and angle outputs or velocity outputs (or both) are done at the same rate as the excitation frequency. The RDC also provides safety diagnostics and observational data for the application that can be used for safety improvements.

If the resolvers are not used, it is possible to configure the associated dedicated SAR ADCs into general purpose ADCs that have four channels each with 12-bit resolution and 3MSPS sample rate. These ADC modules also do not have an associated comparator subsystem.

3.1.1.1.1 Migration From Software to Hardware Resolver

For AM263 devices, the five ADC modules (12-bit, 4MSPS) with comparator subsystems can be leveraged to implement a software-based Resolver system.

With the integrated Resolver peripheral in AM263P devices, two additional ADC modules (12-bit, 3MSPS, no comparator subsystem) were added for direct interface. This is in addition to the same five ADC modules with comparator subsystems that remain available. These added ADC modules can be used to interface to two parallel hardware resolver channels. The Resolver subsystem then hardware synchronizes precisely to the motor control PWM signal to enable the optimization of the motor control loop delay.

3.1.1.2 Trigonometric Math Unit

Each R5F core for all AM263P devices comes with a Trigonometric Math Unit (TMU). This hardware accelerator extends the capabilities of the R5F by speeding up the execution of common trigonometric and arithmetic operations. Table 3-1 provides a list of the available instructions in the TMU.

Table 3-1. List of Implemented Instructions in the TMU

Instruction Name	Description
SINPUF32	Returns the SINE of Input value
COSPUF32	Returns the COSINE of Input value
ATANPUF32	Returns the ATAN of Input value
QUADF32	Returns the quadrant value and the ratio of X and Y inputs which are provided as per unit values.
IEXP2F32	Returns inverse exponent of input value
LOG2F32	Returns base-2 logarithm of input value

3.1.1.3 Remote L2 Cache

Each R5F core for all AM263P devices now has an integrated Remote L2 (RL2) Cache controller that can be used to reserve system memory to cache data. The memory used is from system L2 SRAM and comes with ECC protection. The memory is structured to support 4096 lines of cache support at a line size of 32 bytes. The cache lines are software programmable and can support sizes of 8, 16, 32, 64, or 128kB.

The primary use case for this feature is to cache system data that is typically stored in flash memory into the SoC memory system to improve the processing performance. As the RL2 uses system memory, there are access protections that must be configured to guard the contents so no system data is altered by mistake. For more information, see the *AM263P Technical Reference Manual*.

3.1.2 Memory Subsystem Differences

AM263P comes with three changes to the memory module. The first is an increase in available Tightly-Coupled Memory (TCM) from 64kB to 128kB per CPU core. The second is an increase in the maximum total on-chip RAM (SRAM) from 2MB to 3MB depending on device variants. Details on the specific memory sizes per device variants can be found within the respective device datasheets under the *Operating Performance Points* section.

The final change is the addition of a Remote L2 (RL2) cache for external memory, programmable up to 128kB per CPU core. This RL2 cache allows users to cache the system flash into the SoC memory system. For full details on this feature, see the *Remote L2 Cache* subchapter of the *AM263P Technical Reference Manual*.

3.1.3 CONTROLSS Module Differences

3.1.3.1 ADC Feature Differences and Additions

AM263Px uses the Type-4 ADC Post-Processing Block (PPB). This enables the following additional features compared to the AM263x Type-3 ADC PPB:

- External Channel Selection – Two ADCxEXTMUX signals are provided for each ADC module. These can be used with an external analog MUX to control the channel select to route multiple analog signals to a single ADC channel.
- Repeater Block – Enables fixed amounts of repeated conversions that can be used for oversampling, undersampling, phase delay, and sample spreads.
- Oversampling - The hardware additions in the PPB that support averaging and min/max sample detection are available when oversampling. These can be used for applications like peak detection and outlier removal.
- Synchronization – Sync inputs from either hardware or software allow for the PPBs on different ADC modules to be synchronized.
- Global Software Trigger – This can be used to trigger multiple ADC SOC conversions with a single bit write from the *CONTROLSS_GLOBAL_CTRL* register.

3.1.3.2 ADC Safety Tile Additions

AM263Px adds 12 × ADC Safety Tiles (Simultaneous Compare Blocks) and 1 × ADC Safety Event Aggregator to support redundant sampling which enables safety checker functionality. The safety tiles allow for ADC conversion results from multiple ADC modules to be compared against each other for consistency. The event aggregator tracks the results of each check and can generate trip events for overflow events and measurements that exceed the programmed tolerance.

3.1.3.3 ADC_R Module Addition

To support the Resolver peripheral in AM263P devices, two additional SAR ADC modules, ADC_R0 and ADC_R1, have been added. In applications where the Resolver is not utilized, these ADCs can be configured and used as general purpose ADCs. Each has four channels with 12-bit resolution. The most notable differences between ADC_R0-1 versus ADC0-4 is that the maximum sample for ADCR0-1 is 3 MSPS compared to 4 MSPS for ADC0-4 and that ADCR0-1 does not contain the comparator subsystem that is part of each ADC0-4 module. These additional ADCs benefit from all the Type-4 ADC Post Processing Block improvements that are a part of the AM263P ADC0-4 modules.

3.1.4 QSPI/OSPI Module Differences

AM263P devices come with an Octal SPI (OSPI) that replaces the Quad SPI (QSPI) from AM263 devices. With this new interface, it is possible to connect to both Octal and Quad-SPI flash memories. To connect to OSPI flash memory cells, the interface supports four additional data lines, an additional chip select, and the DQS pin that can be used as a data strobe or loopback clock input. AM263P devices also include two reset outputs for external SPI devices and an input for external ECC failure indication.

There is also a significant change in operation regarding data access. The AM263 QSPI uses a Serial Flash Interface (SFI) memory-mapped block to handle addressing and data access and this interface was limited to a maximum size of 8MB for external flash support. In comparison, the new AM263P OSPI peripheral does not use a memory-mapped interface block and instead handles direct and indirect data accesses through a data target interface. With this change, the upper limit on memory addresses has been increased to 128MB.

These interfaces are not software compatible due to the differences in data accesses. Any AM263-to-AM263P migration requires software updates for the QSPI/OSPI even if the AM263P OSPI bus is only used as a QSPI bus.

Table 3-2 details the high-level feature differences between these interfaces. For further details, see the device-specific Technical Reference Manuals.

Table 3-2. Interface Feature Differences

Feature	AM263 Quad SPI	AM263P Octal SPI
# of Data Lines	4	8
# of Chip Select Lines	1	2
External Device Reset	N/A	Yes, 2 outputs
Data Strobe	N/A	Yes
ECC Fail Indicator	N/A	Yes, 1 input
Data Access	Data access through the SFI memory-mapped interface only	Direct and indirect access supported
Maximum External Flash Supported Per Chip Select	8 MB	128 MB
opTI Flash Support		
XIP	No	Yes
Boot Acceleration	No	Yes
FOTA Acceleration	No	Yes

3.1.5 Hardware Security Module Differences

AM263P devices come with two changes to the Hardware Security Module (HSM). The first is that the dedicated RAM for the HSM is increased from 192kB on AM263 devices to 256kB on AM263P devices.

Second, the HSM Watchdog Timer (WDT) is enabled by default in AM263P devices. With this change, the default clock source for the HSM WDT has been changed to RCCLK10M and the default timeout is set to 25 milliseconds.

3.1.6 Hardware Differences

3.1.6.1 Sourcing VPP With ANALDO

With AM263P, it is possible to use the ANALDO output to connect to the VPP rail to source VPP without the need for an external LDO. By taking advantage of this added functionality, BOM costs can be reduced by removing the VPP LDO from the hardware design.

Figure 3-1 illustrates how the connection can be made. For boards that need to support AM263 devices, a path can be added to support the LDO as necessary.

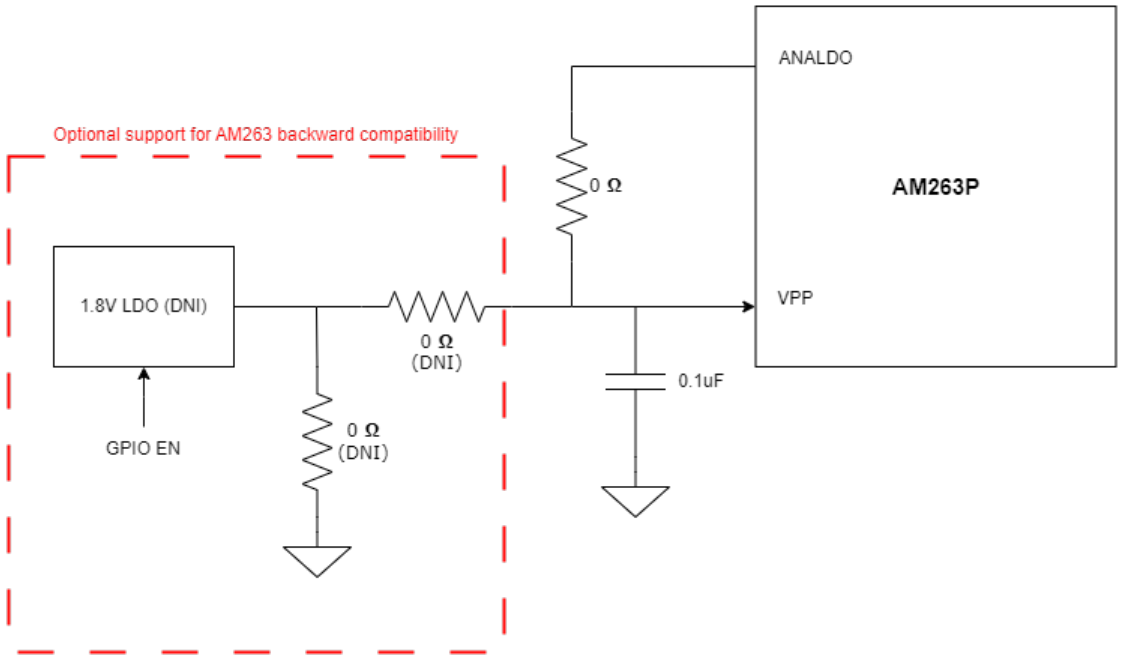

Figure 3-1. Example Schematic

3.1.7 Feature Omissions in AM263P

Beyond the features outlined which have dedicated sections to them, the following features from AM263 are not present in AM263P

- GPMC
- ELM

4 Software Changes Between AM263 and AM263P SDK

Component	AM263	AM263P
ADC	IP Type 3 Driver v1	New hardware feature now supports IP Type 4. SDK includes drivers (v2), documentation, SysConfig, and examples in SDK for the new additions with Type 4. Type 4 additions include the following: • DMA trigger (added feature) • SOC Trigger (added feature) • Trigger Repeater block (new feature set) • PPB Aggregator (new feature set) • External Channel Selection • Open Short Detection (new feature)
ADC Safety, ADC Safety Aggr	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • Comparison against any 2 selected results across most ADC modules with the exception of the 3MSPS or ADC-R modules. • Usage of interrupts when one or more threshold reaches occur across all the ADC Safety Tiles

Component	AM263	AM263P
Resolver	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • Sequencer modes to support single motor single core, single motor lockstep core, and dual motor dual core configurations. • Demonstration of a safety diagnostics feature. Software implementation of Track2 loop is included with the provided examples.
Sigma Delta Filter Module (SDFM)	IP Type 2.1 Driver v0	No hardware changes. Additional SDK examples provided: • Workaround for SDFM Digital Filter interrupt reassertion issue • SDFM-ECAP loopback example
SoC driver - ControlSS CTRL	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • Dynamic clock gating • How to configure the EPWM to use WLINK
Trip and Sync XBAR	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • New XBARs - EXTCHSEL, EQEP SOCAB XBAR, new groups to XBARs • XBAR clock gating
Opti-Flash • FLC • RL2 • RAT	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • RL2 example for how to configure the new feature • FLC example for early CAN response
OSPI	QPSI	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • Flash Diagnostics Example • Flash DMA Example • Flash IO Example • Use of two chip select pins QSPI is also supported with FLASH API which internally uses OSPI, however this requires software updates when transitioning from AM263 to AM263P.
SBL OSPI	SBL QSPI	SBL-OSPI is provided for AM263P
eXecute In Place (XIP) support	N/A	New hardware feature. Enabling XIP functionality does not require dedicated drivers. With XIP functionality offered in AM263P, it is possible to change the boot flow on a per application basis to leverage XIP.
Firmware Over the Air Update (FOTA)	N/A	New hardware feature.SDK includes driver and documentation.
On The Fly Encryption and Authentication (OTFA)	N/A	New hardware feature. SDK includes driver and documentation.
Smart Placement	N/A	New compiler support. This has been developed because Sitara Microcontrollers have different levels of memory with varying latency between the core and peripherals. Smart placement distributes functions and other linker-placed objects across different memories by assigning critically based on the frequency of use to minimize perform degradation. This new feature is available for other Sitara Microcontroller SoCs in addition to AM263P once released.

Component	AM263	AM263P
Function-call Based Layout	N/A	New compiler support. This feature is part of Smart Placement and is geared towards improving the performance of key usage for boot acceleration. However, this can be applied to any start-up code. This feature operates by grouping start-up code functions and data in execution order into address regions that can be programmed using a Fast Local Copy (FLC) hardware accelerator. This new feature becomes available for other Sitara Microcontroller SOCs in addition to AM263P, once released.

5 Feature Differences Between AM263 and AM261 Devices

5.1 Feature Differences for System Consideration

This section outlines the differences and additions to modules when moving from AM263 to AM261.

5.1.1 New Features in AM261

5.1.1.1 Universal Serial Bus (USB)

AM261 devices introduce a USB module that supports USB 2.0 in host, device, and dual role device configurations. In USB host mode, high-speed (HS, 480Mbps), full-speed (FS, 12Mbps), and low-speed (LS, 1.5Mbps) data rates are supported. In USB device mode, only high-speed (HS, 480Mbps) and full-speed (FS, 12Mbps) data rates are supported. The USB module supports all USB transfer types - control, bulk, interrupt, and isochronous.

Features include 15 IN (receive) and 15 OUT (transmit) endpoints (EPs) along with an EP0 endpoint that is bidirectional. USB descriptor caching and data pre-fetch is offered to streamline device enumeration.

For applications that require the USB host provides the 5V output on VBUS, an external charge pump to be controlled by the USB module is required.

5.1.1.2 Trigonometric Math Unit

Each R5F core for all AM261 devices comes with a Trigonometric Math Unit (TMU). This hardware accelerator extends the capabilities of the R5F by speeding up the execution of common trigonometric and arithmetic operations. Table 3-1 provides a list of the available instructions in the TMU.

Table 5-1. List of Implemented Instructions in the TMU

Instruction Name	Description
SINPUF32	Returns the SINE of Input value
COSPUF32	Returns the COSINE of Input value
ATANPUF32	Returns the ATAN of Input value
QUADF32	Returns the quadrant value and the ratio of X and Y inputs which are provided as per unit values.
IEXP2F32	Returns inverse exponent of input value
LOG2F32	Returns base-2 logarithm of input value

5.1.1.3 Remote L2 Cache

Each R5F core for all AM261 devices now has an integrated Remote L2 (RL2) Cache controller that can be used to reserve system memory to cache data. The memory used is from system L2 SRAM and comes with ECC protection. The memory is structured to support 4096 lines of cache support at a line size of 32 bytes. The cache lines are software programmable and can support sizes of 8, 16, 32, 64, or 128kB.

The primary use case for this feature is to cache system data that is typically stored in flash memory into the SoC memory system to improve the processing performance. As the RL2 uses system memory, there are access protections that must be configured to guard the contents so no system data is altered by mistake. For more information, see the AM261 Technical Reference Manual.

5.1.2 Memory Subsystem Differences

AM261 comes with three changes to the memory module. The first is an increase in available Tightly-Coupled Memory (TCM) from 64kB to 256kB per CPU core. The second is a decrease in the maximum total on-chip RAM (SRAM) from 2MB down to 1.5MB depending on device variants. Details on the specific memory sizes per device variants can be found within the respective device datasheets under the *Operating Performance Points* section.

The final change is the addition of a Remote L2 (RL2) cache for external memory, programmable up to 128kB per CPU core. This RL2 cache allows users to cache the system flash into the SoC memory system. For full details on this feature, see the *Remote L2 Cache* subchapter of the *AM261 Technical Reference Manual*.

5.1.3 CONTROLSS Module Differences

5.1.3.1 ADC Feature Differences and Additions

AM261 uses the Type-4 ADC Post-Processing Block (PPB). This enables the following additional features compared to the AM263 Type-3 ADC PPB:

- External Channel Selection – Two ADCxEXTMUX signals are provided for each ADC module. These can be used with an external analog MUX to control the channel select to route multiple analog signals to a single ADC channel.
- Repeater Block – Enables fixed amounts of repeated conversions that can be used for oversampling, undersampling, phase delay, and sample spreads.
- Oversampling - The hardware additions in the PPB that support averaging and min/max sample detection are available when oversampling. These can be used for applications like peak detection and outlier removal.
- Synchronization – Sync inputs from either hardware or software allow for the PPBs on different ADC modules to be synchronized.
- Global Software Trigger – This can be used to trigger multiple ADC SOC conversions with a single bit write from the *CONTROLSS_GLOBAL_CTRL* register.

5.1.3.2 ADC Safety Tile Additions

AM261 adds 12 × ADC Safety Tiles and 1 × ADC Safety Event Aggregator to support redundant sampling which enables safety checker functionality. The safety tiles allow for ADC conversion results from multiple ADC modules to be compared against each other for consistency. The event aggregator tracks the results of each check and can generate trip events for overflow events and measurements that exceed the programmed tolerance.

5.1.4 CPSW Feature Additions

AM261 devices add two new features to the CPSW peripheral.

Interspersed Express Traffic (IET)

This feature allows for the servicing of time-critical 'express' frames that suspend the transmission of non-time-critical 'premptable' frames. IET also allows for one or more time-critical frames to be transmitted. These express frames are transmitted with minimum delay at the cost of delaying the completion of premptable frame transfers.

This feature adheres to the Interspersing Express Traffic 802.3br standard.

Cut-through Switching

This feature is a specific switching method where the switch forwards packets or frames to the end destination immediately after the destination address has been processed without waiting for entire data packet to be received. Utilizing this feature allows for a reduction of latency compared to typical store and forward methods.

5.1.5 Hardware Differences

5.1.5.1 Sourcing VPP With ANALDO

With AM261, it is possible to use the ANALDO output to connect to the VPP rail to source VPP without the need for an external LDO. By taking advantage of this added functionality, BOM costs can be reduced by removing the VPP LDO from the hardware design.

Figure 3-1 illustrates how the connection can be made. For boards that need to support AM263 devices, a path can be added to support the LDO as necessary.

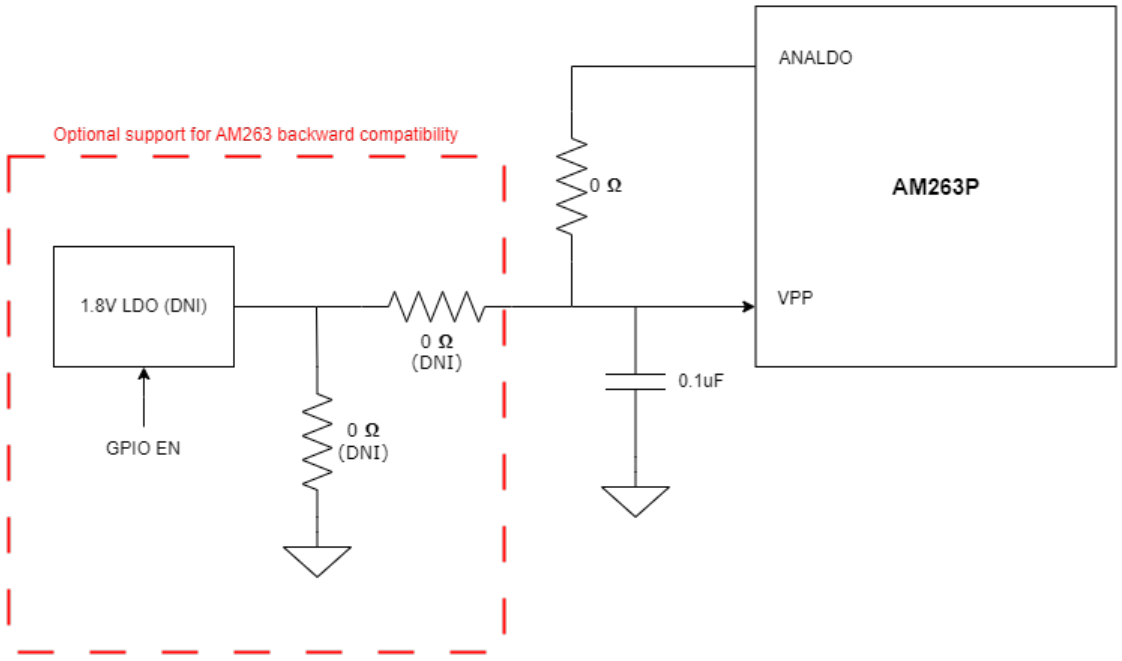

Figure 5-1. Example Schematic

5.1.6 Feature Reductions in AM261

Beyond the features outlined which have dedicated sections to them, the following features from AM263 are not present in AM261 due to the reduction of peripheral counts as outlined Table 1-1:

- ADC3 / ADC4
- ADC Voltage Reference Group 2
- ADC Calibration 1
- DAC Voltage Reference 1
- EPWM10 through EPWM31
- EQEP2
- FSI TX1 / RX1 through TX3 / RX3
- I2C3
- LIN3 and LIN4
- MCAN2 and MCAN3
- SPI4

6 Software Changes Between AM263 and AM261 SDK

Component	AM263	AM261
ADC	IP Type 3 Driver v1	New hardware feature now supports IP Type 4. SDK includes driver, documentation, SysConfig, and examples in SDK for the new additions with Type 4. Type 4 additions include the following: • DMA trigger (added feature) • SOC Trigger (added feature) • Trigger Repeater block (new feature set) • PPB Aggregator (new feature set) • External Channel Selection • Open Short Detection (new feature) Additionally supports hardware changes for: • 3MSPS • 7 Single Ended Channels • 4 External Channel Select Signals
ADC Safety, ADC Safety Aggr	N/A	New hardware feature. SDK includes driver, documentation, SysConfig, and examples for the following features: • Comparison against any 2 selected results across most ADC modules • Usage of interrupts when one or more threshold reaches occur across all the ADC Safety Tiles
CPSW	CPSW	Hardware feature enhanced. SDK includes driver, documentation, and SysConfig to support the following features: • Support for cut-through switching • Support for 802.3br Interspersing Express Traffic (IET) • Enable 25MHz and 50MHz clock output signals for driving Ethernet PHYs
SoC driver - ControlSS CTRL	N/A	New hardware feature. SDK includes driver, documentation, SysConfig, and examples for the following features: • Dynamic clock gating • How to configure the EPWM to use WLINK
HSM - PKE	PKE v3 IP	Hardware feature enhanced. SDK includes driver, documentation, unit test, and SysConfig to support the following features: • PKE v4 IP with 4kB memory
ICSSM	ICSSM at max clock 200MHz	Hardware feature enhanced. SDK includes driver, documentation, and SysConfig to support the following features: • Second instance of ICSSM • Max clock of 225MHz • Additional PRU GPIO pins: PR1_PRU0_GPIO17, PR1_PRU0_GPIO18, PR1_PRU0_GPIO19 • Parallel and serial host interface capability using ICSSM • Support for half-duplex MII signals • Encoder Protocol support for: Endat, HDSL, Tamagawa, Nikkon, and Biss-C
Trip and Sync XBAR	N/A	New hardware feature. SDK includes driver, documentation, SysConfig, and examples for the following features: • New XBARs - EXTCHSEL, EQEP SOCAB XBAR, new groups to XBARs • XBAR clock gating

Component	AM263	AM261
Opti-Flash • FLC • RL2 • RAT	N/A	New hardware feature. SDK includes driver, documentation, SysConfig, and examples for the following features: • RL2 example for how to configure the new feature • FLC example for early CAN response
OSPI	QPSI	New hardware feature. SDK includes driver, documentation, SysConfig, and examples for the following features: • Flash Diagnostics Example • Flash DMA Example • Flash IO Example • Use of two chip select pins • Serial NAND boot mode support • Second OSPI instance can optionally support SRAM, PSRAM, and flash devices QSPI is also supported with FLASH API which internally uses OSPI, however this requires software updates when transitioning from AM263 to AM263P.
SBL OSPI	SBL QSPI	SBL-OSPI is provided for AM261
XBAR	XBAR	Driver updates to reflect changes in integration between devices such as number of instances / signals.
eXecute In Place (XIP) support	N/A	New hardware feature. Enabling XIP functionality does not require dedicated drivers. With XIP functionality offered in AM261, it is possible to change the boot flow on a per application basis to leverage XIP.
Firmware Over the Air Update (FOTA)	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig.
On The Fly Encryption and Authentication (OTFA)	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig.
USB	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • USB 2.0 support • TinyUSB Middleware support with: – Device Firmware Update (DFU), run time only – Booting via DFU - SBL DFU – Network with RNDIS, CDC-ACM, CDC-NCM – Mass Storage Class (MSC) with multiple Logical Units (LUNs)

7 Feature Differences Between AM263P and AM261 Devices

7.1 Feature Differences for System Consideration

This section outlines the differences and additions to modules when moving from AM263P to AM261.

7.1.1 New Features in AM261

7.1.1.1 General-Purpose Memory Controller (GPMC)

Some AM261 devices offer a General-Purpose Memory Controller (GPMC) peripheral which is a unified memory controller dedicated for interfacing with external memory devices.

Devices that can be interfaced via the GPMC include:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash
- devices
- NAND flash
- Pseudo-SRAM devices

The GPMC can support memories up to 4MB in size, and supports 8, 16, or 32-bit wide data paths to external devices.

7.1.1.2 Universal Serial Bus (USB)

AM261 devices introduce a USB module that supports USB 2.0 in host, device, and dual role device configurations. In USB host mode, high-speed (HS, 480Mbps), full-speed (FS, 12Mbps), and low-speed (LS, 1.5Mbps) data rates are supported. In USB device mode, only high-speed (HS, 480Mbps) and full-speed (FS, 12Mbps) data rates are supported. The USB module supports all USB transfer types - control, bulk, interrupt, and isochronous.

Features include 15 IN (receive) and 15 OUT (transmit) endpoints (EPs) along with an EP0 endpoint that is bidirectional. USB descriptor caching and data pre-fetch is offered to streamline device enumeration.

For applications that require the USB host provides the 5V output on VBUS, an external charge pump to be controlled by the USB module is required.

7.1.2 Memory Subsystem Differences

AM261 comes with two changes to the memory module. The first is an increase in available Tightly-Coupled Memory (TCM) from 128kB to 256kB per CPU core. The second is a reduction in the total on-chip RAM (SRAM) where AM263P offers 2MB to 3MB of SRAM while AM261 offers 1MB to 1.5MB of SRAM. The amount of SRAM present depends on device variants. Details on the specific memory sizes per device variants can be found within the respective device datasheets under the *Operating Performance Points* section.

7.1.3 CPSW Feature Additions

AM261 devices add two new features to the CPSW peripheral.

Interspersed Express Traffic (IET)

This feature allows for the servicing of time-critical 'express' frames that suspend the transmission of non-time-critical 'premptable' frames. IET also allows for one or more time-critical frames to be transmitted. These express frames are transmitted with minimum delay at the cost of delaying the completion of premptable frame transfers.

This feature adheres to the Interspersing Express Traffic 802.3br standard.

Cut-through Switching

This feature is a specific switching method where the switch forwards packets or frames to the end destination immediately after the destination address has been processed without waiting for entire data packet to be received. Utilizing this feature allows for a reduction of latency compared to typical store and forward methods.

7.1.4 ADC Module Differences

There are a few differences between the ADC modules used in AM263P and AM261. See Table 7-1 for the full list of differences.

Table 7-1. ADC Differences

Feature	AM263P	AM261
Sampling Rate	Up to 4MSPS	Up to 3MSPS▼
Single Ended Channels per Module	6	7▲
Differential Channels per Module	3	3
Calibration Inputs	2	1▼

7.1.5 Feature Omissions and Reductions in AM261

Beyond the features outlined which have dedicated sections to them, the following features from AM263P are not present in AM261 due to the reduction of peripheral counts as outlined Table 1-1:

- ADC3 / ADC4
- ADC Voltage Reference Group 2
- ADC Calibration 1
- DAC Voltage Reference 1
- EPWM10 through EPWM31
- EQEP2
- FSI TX1 / RX1 through TX3 / RX3
- I2C3
- LIN3 and LIN4
- MCAN2 through MCAN7
- SPI4 through SPI7
- RTI4 through RTI7

The number of ADC Safety Tiles (Simultaneous Compare Blocks) per ADC instance are reduced from 12 to 6.

Additionally, the following features from AM263P are not present in AM261:

- Resolver-to-Digital Converter

8 Software Changes Between AM263P and AM261 SDK

Component	AM263P	AM261
ADC	IP Type 4	SDK includes driver changes, documentation, and SysConfig changes to support the following features: • 3MSPS • 7 Single Ended Channels • 4 External Channel Select Signals
CPSW	CPSW	Hardware feature enhanced. SDK includes driver, documentation, and SysConfig to support the following features: • Support for cut-through switching • Support for 802.3br Interspersing Express Traffic (IET) • Enable 25MHz and 50MHz clock output signals for driving Ethernet PHYs
GPMC	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • 16-bit parallel data bus and 22-bit address bus applications with GPMC • Memory expansion with External SRAM, PSRAM, NOR, and NAND memory options
HSM - PKE	PKE v3 IP	Hardware feature enhanced. SDK includes driver, documentation, and SysConfig to support the following features: • PKE v4 IP with 4kB memory

Component	AM263P	AM261
ICSSM	ICSSM at max clock 200MHz	Hardware feature enhanced. SDK includes driver, documentation, and SysConfig to support the following features: • Second instance of ICSSM • Max clock of 225MHz • Additional PRU GPIO pins: PR1_PRU0_GPIO17, PR1_PRU0_GPIO18, PR1_PRU0_GPIO19 • Parallel and serial host interface capability using ICSSM • Support for half-duplex MII signals • Encoder Protocol support for: Endat, HDSL, Tamagawa, Nikkon, and Biss-C
OSPI	OSPI	Hardware feature enhanced. SDK includes driver, documentation, and SysConfig to support the following features: • Second OSPI instance for optional SRAM, PSRAM, and flash device support • 1x OSPI instance with XIP at 166MHz • Serial NAND boot mode support
USB	N/A	New hardware feature. SDK includes driver, documentation, and SysConfig to support the following features: • USB 2.0 support • TinyUSB Middleware support with: – Device Firmware Update (DFU), run time only – Booting via DFU - SBL DFU – Network with RNDIS, CDC-ACM, CDC-NCM – Mass Storage Class (MSC) with multiple Logical Units (LUNs)
XBAR	XBAR	Driver updates to reflect changes in integration between devices such as number of instances / signals.

9 List of Errata Fixes in AM26x Devices

Table 9-1 contains a comprehensive list of Errata items from AM263 and outlines in which issues are fixed in either Rev 1.1 of AM263, Rev 1.0 of AM263P, or Rev 1.0 of AM261. Full details for the errata items are provided in the following documents:

- AM263x Sitara™ Microcontroller Silicon Revision 1.0A, 1.1
- AM263Px Sitara™ Microcontroller Silicon Revision 1.0
- AM261x Sitara™ Microcontroller Silicon Revision 1.0

Table 9-1. AM263 and AM263P Errata Fixes

Module	Description	Silicon Revisions Affected			
		AM263x		AM263P	AM261
		1.0A	1.1	1.0	1.0
ADC	i2346 — ADC result has error when switching between odd and even channels	Present	Fixed	Fixed	Fixed
ADC	i2347 — VREF current consumption of ADC is random at power up	Present	Fixed	Fixed	Fixed
ADC	i2349 — ADC VREFHI loading increased in power down	Present	Fixed	Fixed	Fixed
AES	i2428 — AES in DTHE generates extra DMA request for data_in at the end of GCM encrypt	Present	Present	Present	Fixed
BOOT	i2426 — ROM does not support OSPI extended OP Code in RDSFDP Sequence switching to 8S & 8D mode	Not Applicable	Not Applicable	Present	Fixed
BUS SAFETY	i2393 — Granular error status not logged in BUS_SAFETY_ERR registers for the detected faults	Present	Present	Present	Fixed
CLOCKS	i2324 — No synchronizer present between GCM and GCD status signals	Present	Present	Present	Present
CONTROLSS	i2352 — CONTROLSS-SDFM: Dynamically changing threshold settings (LLT, HLT), filter type, or COSR settings trigger spurious Comparator Events	Present	Present	Present	Present
CONTROLSS	i2353 — CONTROLSS-SDFM: Dynamically changing data filter settings (Such as Filter Type or DOSR) trigger spurious data acknowledge events	Present	Present	Present	Present
CONTROLSS	i2354 — CONTROLSS-SDFM: Two back-to-back writes to SDCPARMx Register Bit Fields CEVT1SEL, CEVT2SEL, and HZEN within three SD-Modulator Clock Cycles can corrupt SDFM State Machine, resulting in spurious Comparator Events	Present	Present	Present	Present
CONTROLSS	i2355 — CONTROLSS-ADC: DMA Read of stale result	Present	Present	Fixed	Fixed
CONTROLSS	i2356 — CONTROLSS-ADC: Interrupts stop if INTxCONT (Continue-to-Interrupt Mode) is not set	Present	Present	Present	Present
CONTROLSS	i2357 — CONTROLSS-ePWM: An ePWM Glitch can Occur if a Trip Remains Active at the End of the Blanking Window	Present	Present	Present	Present
CONTROLSS	i2358 — CONTROLSS-ePWM: Trip Events are not filtered by the Blanking Window for the first 3 Cycles after the start of a Blanking	Present	Present	Present	Present
CONTROLSS	i2359 — CONTROLSS-CMPSS:Prescaler counter behavior different from specification when DACSOURCE is made 0 or reconfigured as 1	Present	Present	Present	Present
CONTROLSS	i2405 — Race condition OUTPUT_XBAR and PWM_XBAR resulting in event miss	Present	Present	Present	Fixed
CPSW	i2345 — :Ethernet Packet corruption occurs if CPDMA fetches a packet which spans across memory banks	Present	Present	Present	Present
CPSW	i2401 — Host Timestamps cause CPSW port to lock up	Present	Present	Present	Fixed
CPSW	i2402 — Ethernet to Host Checksum Offload does not work	Present	Present	Fixed	Fixed
CPSW	i2329 — MDIO interface corruption (CPSW and PRU-ICSS)	Present	Fixed	Fixed	Fixed
CPSW	i2438 — Host to Ethernet Checksum generation with VLAN ADD/ Remove	Present	Present	Present	Fixed
CPSW	i2439 — Host to Ethernet Timestamp accuracy issue	Present	Present	Present	Present
CPSW	i2440 — Host to Ethernet Timestamp Sequence ID issue	Not Applicable	Not Applicable	Not Applicable	Present
CRC	i2386 — CRC 8-bit data width and CRC8-SAE-J1850 and CRC8-H2F possible use in CAN module is not supported	Present	Present	Fixed	Fixed
DCC	i2395 — DCC Module Frequency Comparison can Report Erroneous Results	Present	Present	Not Applicable	Not Applicable
GPMC	i2313 — Sub-32-bit read issue with NAND and FPGA/FIFO	Present	Present	Not Applicable	Fixed

Table 9-1. AM263 and AM263P Errata Fixes (continued)

Module	Description	Silicon Revisions Affected			
		AM263x		AM263P	AM261
		1.0A	1.1	1.0	1.0
ICSS	i2433 — Reading the 64-bit IEP timer does not have a lock MSW logic when LSW is read	Present	Present	Present	Present
M4 ROM	i2403 — SBL redundant boot image feature not supported on HSSE devices	Not Applicable	Present	Present	Fixed
MBOX	i2404 — Race condition in mailbox registers resulting in events miss	Present	Present	Present	Fixed
McSPI	i2350 — McSPI data transfer using EDMA in 'ABSYNC' mode stops after 32 bits transfer	Present	Present	Fixed	Fixed
OSPI	i2189 — Controller PHY Tuning Algorithm	Not Applicable	Not Applicable	Present	Present
OSPI	i2351 — Direct Access Controller (DAC) does not support Continuous Read mode with NAND Flash	Not Applicable	Not Applicable	Present	Present
OSPI	i2383 — 2-byte address is not supported in PHY DDR mode	Not Applicable	Not Applicable	Present	Present
QSPI	i2364 — Access to address beyond 8MB is not supported in mem map mode	Present	Present	New OSPI module can support addresses beyond 8MB	New OSPI module can support addresses beyond 8MB
R5FSS	i2374 — PBIST fails if clock frequency of R5SS_CORE_CLK is not same as R5FSS_CLK_SELECTED frequency	Present	Present	Present	Present
ROM	i2426 — ROM does not support OSPI 8D boot mode for the flashes supporting extended opcode	Not Applicable	Not Applicable	Present	Fixed
RAM SEC	i2427 — RAM SEC can cause Spurious RAM writes resulting in L2 & MBOX memory corruption				
SDFM	i2375 — SDFM module event flags (SDIFLG.FLTx_FLG_CEVTx) do not get set again if the comparator event is still active and digital filter path (using SDCOMPxCTL.CEVTxDIGFILTSEL) is being selected	Present	Present	Fixed	Fixed
SOC CONTROL	i2392 — Race condition in mem-init capture registers resulting in events miss	Present	Present	Present	Fixed
SOC CONTROL	i2394 — Race condition in interrupt and error aggregator capture registers resulting in events miss	Present	Present	Present	Fixed
TCM	i2411 — 128 Bytes burst access is not supported for TCM	Not Applicable	Not Applicable	Not Applicable	Present
UART	i2310 — Erroneous triggering of timeout interrupt	Present	Present	Present	Present
UART	i2311 — Spurious DMA Interrupts	Present	Present	Present	Present
USB	i2412 — USB can not generate interrupt upon DMA read/Write Access error	Not Applicable	Not Applicable	Not Applicable	Present
VDDA	i2348 — VDDA1V8 Static Power leakage	Present	Fixed	Fixed	Fixed

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (November 2024)	Page
• Migration Guide has been updated to add AM261 and now covers migration between AM263 / AM263P / AM261	1

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265