Technical White Paper

Enabling Low Power Embedded Systems With AM62x Processors

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Trademarks

1 Introduction

The increasing popularity of embedded systems in a wide range of applications pushes for a higher level of integration onto a single SoC. This high level of integration leads to higher power dissipation, increased thermal system cost, degraded performance, and reduced battery life. To overcome these challenges, SoCs should be defined, architected, and designed in the context of their usage in the targeted embedded systems. Since every application is different, picking the correct operating settings for the SoC will achieve optimal performance and power. This paper presents novel features and techniques developed on the AM62x processors - a next-generation Sitara MPU device from Texas Instruments.

AM62x processors feature a high-performance Quad-core Cortex A53 with 64-bit architecture, a powerful 3D Graphics Engine, an integrated M4F MCU Channel for general purpose usage or safety with full freedom-from interface (FFI) from the application domain, a Dual-core M4F for Foundational and Automotive/Industrial Security, a dedicated R5F core for device resources and low power management. The modular architecture of this device delivers performance with support for several low power modes without sacrificing critical system resources, such as connectivity, power, security, safety, and cost. Figure 1 shows a high-level AM62x processor block diagram.

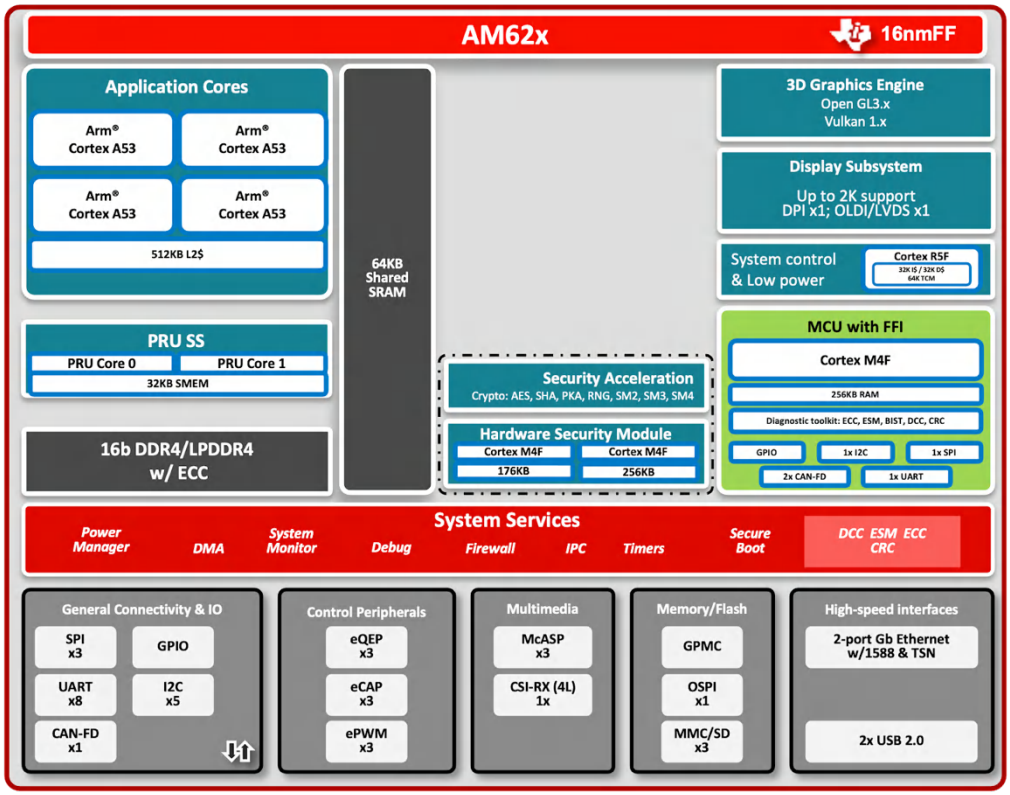


Figure 1-1. Block Diagram of the Sitara™ AM62x Processors

2 AM62x Power Management Features

The AM62 processor uses several essential techniques to reduce active and static power consumption. Table 2-1 shows the AM62x power management features and the benefits.

Table 2-1. AM62x Power Management Features

Key Features	AM62x Power Management	Benefits
Low Power Modes	DeepSleep, MCU Only, Standby, Partial I/O	Longer battery operation lifetime
Active Power Management	Low bus clock frequency operation at 125 MHz (OPP low)	Low active power consumption for low activity use cases
	Dynamic frequency scaling (DFS)	Thermal management
Power Supply Simplification	Up to 1.25 GHz A53 at 0.75 V Up to 1.4 GHz A53 at 0.85 V	Differentiated low power capability with 0.75-V core power supply Higher performance with 0.75-V core power supply
	Single core power supply Simpler power domains	Lower cost power solution and less complicated software control for power management
	Simple power sequencing with integrated LDO enabling a low-cost discrete power solution	Easier to optimize a power solution for the overall system Low-cost power solution
Companion PMIC	New low cost PMIC	Low cost PMIC optimized for AM62x

2.1 Low Power Modes

The AM62x processor supports optimized low power modes with varying levels of power dissipation: Partial I/O mode to Deepsleep mode to Standby mode (sub mW to a few mW). Table 2-2 shows a high-level description of various low-power modes supported on AM62x processors.

Table 2-2. AM62x Low Power Modes

Low Power Modes	Wakeup Sources	Application State and Use Case
Partial I/O	CANUART I/O Bank pins	The entire SoC is OFF except I/O pins in CANUART I/O bank to maintain I/O wakeup capability from CANUART I/O Bank I/O pins.
DeepSleep	GP Timers, RTC Timer, UART, I2C, MCU GPIO0, I/O Daisy Chain, USB wakeup events	Core domain register information will be lost. On-chip peripheral register (context) information of core domain needs to be saved by application to DDR before entering this mode. DDR is in self-refresh. Boot ROM executes and branches to peripheral context restore for wakeup, followed by system resume. This mode is primarily used for Suspend to RAM for battery lifetime or backup operation.
MCU Only	DeepSleep wakeup events, Interrupt evens supported in MCU channel	The MCU subsystem runs at the MCU PLL clock. The rest of the SoC status is the same as DeepSleep. DDR is in self-refresh. MCU can run applications with MCU domain peripherals while in this low power mode.
Standby	Any SoC interrupt event	On-chip contents are fully preserved. Any SoC interrupt event can cause a wakeup event from this low power mode. A53 and MCU M4F are in WFI or power down. DDR memory is in self-refresh. The device can run low-level processing with non-Wakeup/MCU domain peripherals and support wakeup from thos peripherals.

Partial I/O: I/O pins and small logic in the CANUART I/O Bank are active, and the rest of the SoC is turned off. The user can use the I/O pins to aggregate multiple I/O wakeup events and toggle the PMIC_LPM_EN pin to enable PMIC or discrete power solution when an I/O wakeup event is triggered. The information on the I/O wakeup event is logged in the MMR in the CANUART I/O bank and helps the software to distinguish between cold boot and wakeup to respond to the wakeup event faster. This mode can be used to support CAN wakeup or Ethernet Wakeup.

DeepSleep: DeepSleep mode enables lower power consumption than Standby or MCU-Only. DeepSleep mode is typically used during inactivity when the user requires very low power while waiting for an event that requires processing or higher performance. DeepSleep is the lowest power mode which still includes DDR in self-refresh, so wakeup events do not require a full cold boot, significantly reducing wakeup latencies. The lowest power in this mode can be achieved by disabling both oscillators when the RTC or other timer function is not required.

MCU Only: MCU-Only can be used for low power use cases that require low-level processing during a low power mode. The status of the SoC is the same as DeepSleep, except the MCU channel is fully active to run applications with MCU channel resources and peripherals. Any interrupt event in the MCU channel can initiate a wakeup from MCU-Only, and the wakeup events supported in DeepSleep can also trigger wakeup from MCU-Only.

Standby: The device can be placed in Standby mode to reduce power consumption during low activity levels. This first level of power management allows you to maintain the device context for fast resume times. Standby state results in lower power consumption than Active mode but require the user to save the switched-off power domain context to On-Chip Memory or DDR and restore the contexts to resume properly upon wakeup.

2.2 Active Power Management

Dynamic Frequency Scaling (DFS) is a power management technique that dynamically scales the operating frequency across device Operating Performance Points (OPP). An OPP is a voltage/frequency pair that defines a specific power state. The software controls the clock frequency for each OPP to adjust the performance and power to the optimum point. The device supports DFS for Cortex-A53 only.

The AM62x processor supports lower bus frequency operation as OPP Low. The OPP Low must be configured at boot time. In OPP Low, the main CBASS clock frequency is reduced in half to lower active power consumption with reduced performance. The performance of some peripheral modules is limited or not available in this operating condition.

2.3 Power Supply Simplification

When it comes to power optimization, it is imperative to consider how the SoC will be used in a given system alongside total system power optimization and not just the SoC power - a key part of the holistic approach. Minimizing the number of dedicated power rails needed by SoC not only simplifies the power-supply solution. AM62x device is architected with a shared core vdd along with flexibility to scale voltage level to meet the demands of wide range of applications.

Selecting the right core voltage for a given application results in an optimized system power. The AM62x device is able to demonstrate that by scaling core power supply from 0.8 V, the standard core voltage for the process node, to 0.75 V, there was a total of 15% reduction in active power. On the other hand, where performance is a key care about, scaling the core power supply from 0.8 V to 0.85 V resulted in 15% increase in device performance.

The AM62x processor supports simple core power supply without DVFS/AVS and enables 100K POH with the fixed core voltage for entire SoC with full performance entitlement.

2.4 Power Solutions

By leveraging the simplified power requirements mentioned above, TI developed two types of low-cost power solutions for AM62x processors. The TPS65219 is the PMIC specifically designed for AM62x processors and fully leverages the simplified power requirements to provide the lowest cost PMIC for AM62x processors. A discrete power solution can provide the scalability and flexibility to adjust the power solution to be optimized for overall system requirements or meet different current capacities or the number of power supplies required by customers. Table 2-3 compares the two low-cost power solutions designed for AM62x processors.

Table 2-3. AM62x Power Solutions

	Discrete Power	Single PMIC Solution
Availability	Now: (TPS6282x, TPS745xx, TLV7103318, TLV75518)	TPS65219

Table 2-3. AM62x Power Solutions (continued)

	Discrete Power	Single PMIC Solution
Power Features	Leverages AM62x analog integration for power supply simplification	2.7 to 5.5-V input supply
	Supports multiple input supplies: 3.3 V, 5 V	Single PMIC solution developed specifically for AM62x/AM64x processors
	Scalability to meet different custom requirements for current capacity, and lowest cost	Automotive support
Power Management Features	N/A	Programmable power sequencing and default voltages
Functional Safety	Customer driven implementation leveraging AM62x features	N/A
Power Solution Size Estimate	Scalable based on system requirements	81.54 mm2 with 4 x 4 mm2 QFN, 0.4-mm pitch 69.66 mm2 with 5 x 5 mm2 QFN, 0.5-mm pitch
AM62x EVM	AM62x SK	AM62Q SK

3 Low Power Processor Architecture Considerations

Hardware and software co-design is extremely critical to power and latency optimization. Figuring out the right hardware-software boundary, identifying which function is in hardware and which function is in software earlier on during the definition is key. Simplifying software sequences for low power mode entry and exit modes by eliminating save and restore of configuration settings supported by innovative new features such as USB and DDR Reset Isolation and Retention schemes. Optimizing IO states (pull-ups and pull-downs) based on low power use-case and ability to put IOs in retention enhances the system robustness and reliability.

Early in the development phase, several different HW/SW partitions were evaluated, to determine best implementation to meet overall system use-cases and goals (cost, performance, power, and latency). The AM62x processor is mainly divided into 4 domains, as shown in Figure 3-1.

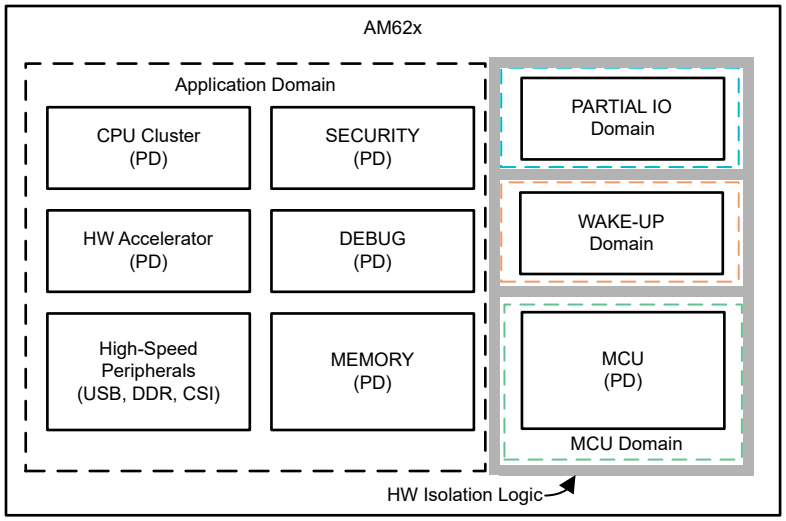


Figure 3-1. SoC Partition

Application domain comprising of high-performance CPUs, HW accelerators, and high-speed peripherals. This domain is further divided into various sub-systems with internal power switches. Depending on the system use-cases, these sub-systems can be completely powered-down using the internal power-domain switches. For example: un-used CPU cores in a cluster, HW accelerators (graphics, display), and so forth. In addition, during DeepSleep and MCU only low power modes, application domain is put to lowest power mode through internal subsystem power gating.

MCU domain comprising of real-time CPUs and peripherals. This domain can be configured to operate completely independent from the application domain: a key differentiating feature in several automotive, industrial, and battery-operated applications. During DeepSleep mode, the MCU domain can be powered-down through internal power switches.

Wake-up domain comprising of Power Management CPU and system components such as clocks, resets, power, and wake-up. This domain is responsible for device boot-up, resource configuration and management, and low power management. Hardware isolation is built around this domain to ensure that clear separation between application and MCU domains. By carefully partitioning the responsibilities between hardware and software functions, Sitara MPU devices achieve simpler and robust low power mode entry and exit sequences. In addition, to improve low power mode entry/exit latencies, Sitara MPU devices developed innovative new features such as USB and DDR reset isolation and retention schemes to avoid complex software sequences that require peripheral configuration save and restore.

4 AM62x Power Consumption

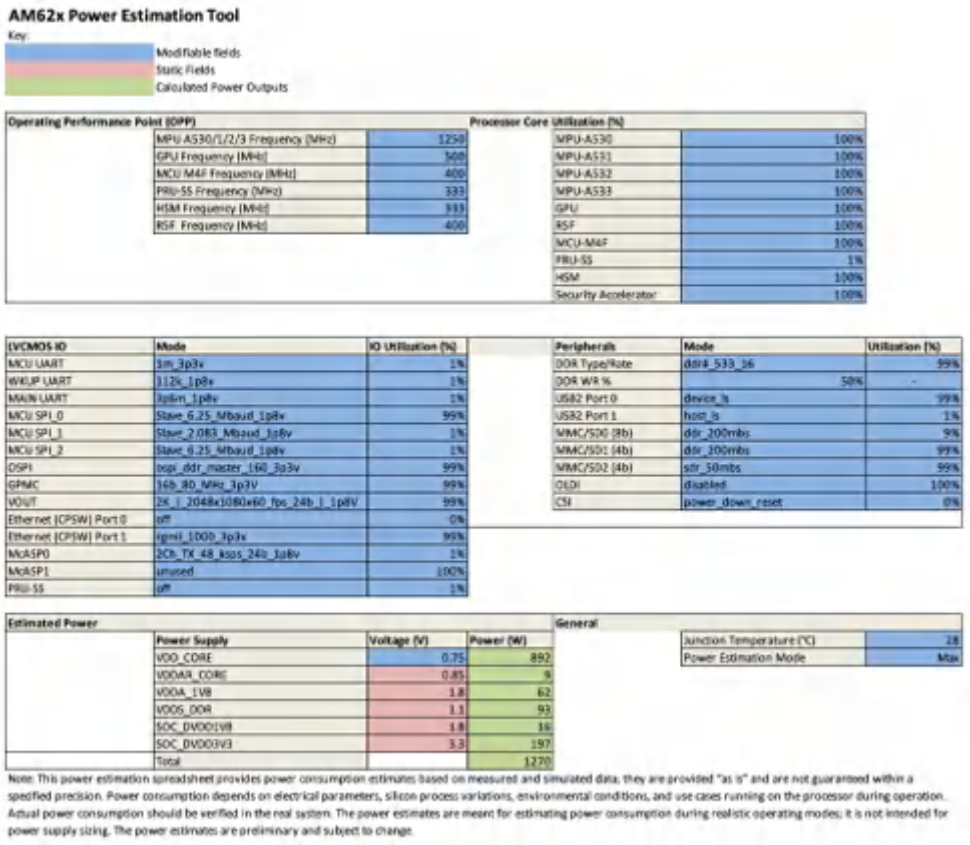
Table 4-1 shows power consumption at various SoC states and the scalability of power and performance. By leveraging low power mode implementation and techniques, AM62 processors achieve less than 500-mW power consumption for a single A53 core running at 1 GHz. The power consumption is almost half of the power consumption achieved by similar low power and low-cost processors in previous generations. AM62x processor power can still be less than 1 W when Quad A53 cores run a stressful application on all four cores at 1.4 GHz.

Table 4-1. AM62x Power Consumption

	Cortex A53 at 1 GHz 0.75-V VDD_CORE			**Cortex A53 at 1.4 GHz 0.85-V VDD_CORE**		
	Idle 1xA53 (mW)	**Dhrystone 1xA53 (mW)**	**Dhrystone 4xA53 (mW)**	**Idle 1xA53 (mW)**	**Dhrystone 1xA53 (mW)**	**Dhrystone 4xA53 (mW)**
VDD_CORE	343	395	570	466	565	880
VDDR_CORE	3	4	7	2	4	8
VDDS_DDR	45	45	45	45	45	45
Total (without I/O and Analog)	391	444	622	513	614	933

5 Power Estimation Tool

TI provides the Power Estimation Tool (PET) based on the processor power model created from measured and simulated data. Developers gain insight into the power consumption of AM62x processors for various application scenarios, electrical parameters, silicon process variations, and environmental conditions before they start designing hardware and software. The power estimations from the tool can be used for deciding the operating performance points of the AM62x processor, evaluating thermal design, or estimating the battery lifetime of the end products. The tool allows the developer to choose different operating conditions and processor configurations to make a trade-off between operating performance and power consumption with various power-saving techniques. This tool estimates power consumption during realistic operating modes and is not intended for power supply sizing.



AM62x Power Estimation Tool

Key:

Modifiable fields
Static Fields
Calculated Power Outputs

Operating Performance Point (OPP)			Processor Core Utilization (%)	
	MPU A530/1/2/3 Frequency (MHz)	1250	MPU-A530	100%
	GPU Frequency (MHz)	500	MPU-A531	100%
	MCU M4F Frequency (MHz)	400	MPU-A532	100%
	PRU-SS Frequency (MHz)	333	MPU-A533	100%
	HSM Frequency (MHz)	333	GPU	100%
	RSF Frequency (MHz)	400	RSF	100%
			MCU-M4F	100%
			PRU-SS	1%
			HSM	100%
			Security Accelerator	100%

LVCMOS IO	Mode	IO Utilization (%)
MCU UART	1m_3p3v	1%
WKUP UART	112k_1p8v	1%
MAIN UART	3p6m_1p8v	1%
MCU SPI_0	Slave_6.25_Mbaud_1p8v	99%
MCU SPI_1	Slave_2.083_Mbaud_1p8v	1%
MCU SPI_2	Slave_6.25_Mbaud_1p8v	1%
OSPI	ospi_ddr_master_166_3p3v	99%
GPMC	16b_80_MHz_3p3V	99%
VOUT	2K_I_2048x1080x60_fps_24b_1_1p8V	99%
Ethernet (CPSW) Port 0	off	0%
Ethernet (CPSW) Port 1	rgmii_1000_3p3v	99%
McASP0	2Ch_TX_48_ksps_24b_1p8v	1%
McASP1	unused	100%
PRU-SS	off	1%

Peripherals	Mode	Utilization (%)
DDR Type/Rate	ddr4_533_16	99%
DDR WR %	50%	-
USB2 Port 0	device_hs	99%
USB2 Port 1	host_hs	1%
MMC/SD0 (8b)	ddr_200mbs	9%
MMC/SD1 (4b)	ddr_200mbs	99%
MMC/SD2 (4b)	sdr_50mbs	99%
OLDI	disabled	100%
CSI	power_down_reset	0%

Estimated Power			
	Power Supply	Voltage (V)	Power (W)
	VDD_CORE	0.75	892
	VDDAR_CORE	0.85	9
	VDDA_1V8	1.8	62
	VDDS_DDR	1.1	93
	SOC_DVDD1V8	1.8	16
	SOC_DVDD3V3	3.3	197
	Total		1270

General	
Junction Temperature (°C)	28
Power Estimation Mode	Max

Note: This power estimation spreadsheet provides power consumption estimates based on measured and simulated data; they are provided "as is" and are not guaranteed within a specified precision. Power consumption depends on electrical parameters, silicon process variations, environmental conditions, and use cases running on the processor during operation. Actual power consumption should be verified in the real system. The power estimates are meant for estimating power consumption during realistic operating modes; it is not intended for power supply sizing. The power estimates are preliminary and subject to change.

Figure 5-1. AM62x Power Estimation Tool

6 Conclusion

AM62 processors enable low-power embedded systems for edge devices with analytics or human-machine interface capability. Low power modes and low active power consumption allow a wide range of battery-operated applications and small form factor product design without heatsink or fans. Unique 0.75-V core voltage operation and power management features support adjusting performance and power for optimal for each customer application and help enable a simple and low-cost power solution by leveraging advanced analog integration.

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