Application Note

Implement Three-Phase Interleaved LLC on C2000 Type-4 PWM

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ABSTRACT

This application report explains the techniques to implement three-phase interleaved LLC on generation 3 C2000™ devices with Type-4 PWM. Detailed PWM generation logics of both primary and secondary side of LLC is presented to deal with the complex frequency changing and phase shifting requirements of LLC. Additionally, the new configurable logic block (CLB) module is leveraged to ensure safe operation of LLC synchronous rectification (SR) switch. Detailed CLB configuration and test result are provided.

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1 Introduction

With the advantages of high efficiency and better EMI performance, LLC is becoming a popular DC/DC topology in power supply applications. As the single PSU power requirement is increasing, interleaved technique has become an efficient way to achieve a higher power level without significantly upgrading the power devices. In recent years, as a typical interleaved topology, three-phase interleaved LLC is widely used in telecom and server PSU. Compared to a paralleled topology, three-phase interleaved LLC can significantly reduce current ripple and is easier to implement current balance. Combined with special magnetic component design, the size of inductor and transformer could be reduced as well.

However, as a typical PFM (frequency-changing) control topology, the frequency and phase-shift between phases are varying cycle-by-cycle. Thus, it requires a highly flexible PWM peripheral to make sure the PWM is in the correct order all of the time. This application report discusses how to leverage type-4 PWM on C2000 to implement the PWM signals of a three-phase interleaved LLC.

2 Basic 3-Phase Interleaved LLC PWM Implementation

The increasing number of PWM modules on C2000 generation three devices is making it possible to support multi-phase topology control, which requires a high PWM output number. More importantly, the new real-time features supported by the new type 4 PWM peripheral is making C2000 capable of handling complicated frequency changing, phase-shifting, and cooperation between primary and secondary side (synchronized rectifier MOS), which are essential to control multi-phase topology under all conditions. This is what differs C2000 from other general-purpose MCUs, even though they may provide more PWM outputs.

2.1 Primary Side

Firstly, Figure 2-1 demonstrates how the primary side PWM control signal of a 3-phase interleaved LLC could be generated. Assuming PWM 1/2/3 represents he PWM signal of phase A/B/C, respectively, 120° phase shift is required between each phase to achieve 3-phase interleaved LLC. To achieve this, CMPA is set to 1/3*PRD, while CMPB is set to 5/6*PRD for channel 2, and CMPA is set to 2/3*PRD, while CMPB is set to 1/6*PRD for channel 3. By configuring channel 2 and channel 3's toggling action as shown in Figure 2-1, a 120° phase shift can be achieved.

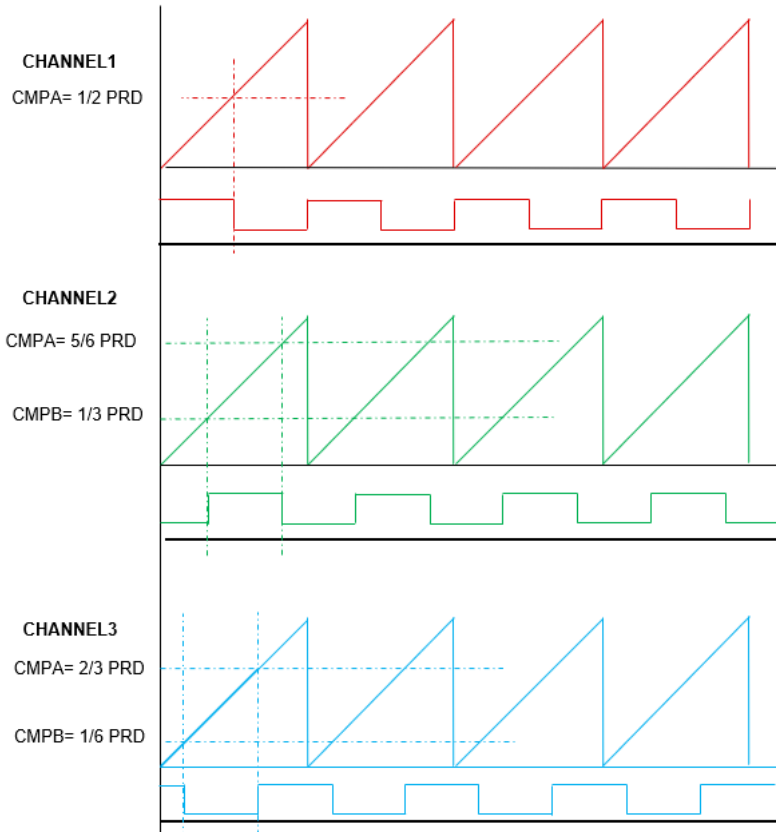

Figure 2-1. Primary Side PWM Waveform

Special consideration is needed when the frequency changes. Since CMPA/CMPB values are calculated from PWM, they must be loaded simultaneously to avoid the mismatch of PWM period and phase shifting between three PWM phases.

To achieve accurate control of load timing in multiple PWM modules, global and one-shot load features are leveraged. First, global load is configured separately in PWM 1/2/3 to make sure the period and comp A/B values are loaded simultaneously when CTR=0. Second, one-shot load is enabled, to make sure the value is loaded only after the control loop running is totally finished before the content in the shadow registers is loaded into the active registers.

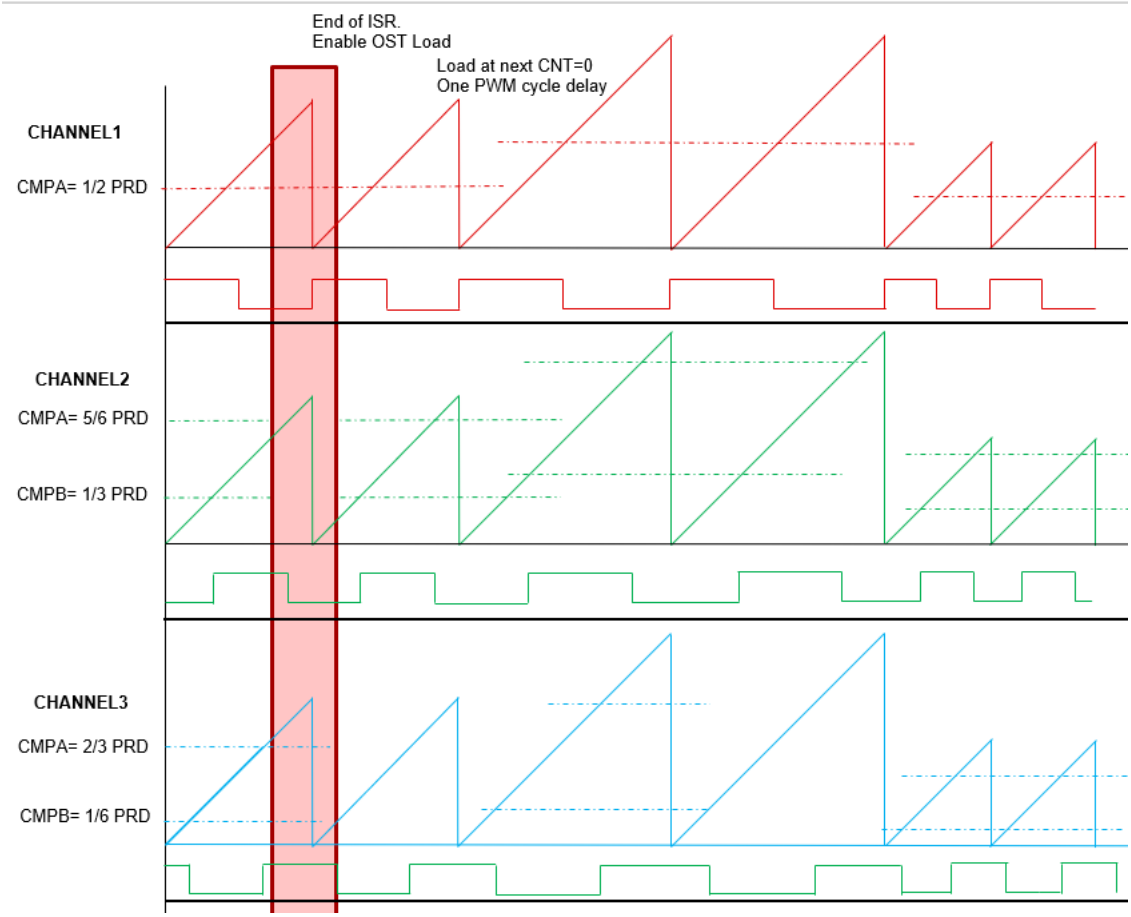

Figure 2-2. Primary Side PWM With Frequency Change

An example is shown in Figure 2-2 to explain why one-shot load is necessary. The special case to consider here is when the control ISR execution period is crossing two PWM periods. If loading to PRD and CMPA/B shadow register is not in the same PWM cycle, the phase shifting of phase B and C would be disordered. To avoid the mismatch, one-shot is enabled only at the end of the control ISR. As the result, the new PRD and CMPA/B value would become effective simultaneously at the next time base counter equal to zero match. Though this may bring a minor delay, which is less than a PWM cycle, it would ensure all the PWM channels work properly.

Normally, three-phase LLC works with a fixed 50% duty cycle, thus complimentary PWM signals are easy to generate with DB (dead-band) submodule in PWM. Figure 2-3 represents an example of Phase-A, where active-high complementary (AHC) mode is used to generate two complementary PWM signals. Similarly, the dead-band feature could be used to generate the complementary PWM for Phase-B and Phase-C.

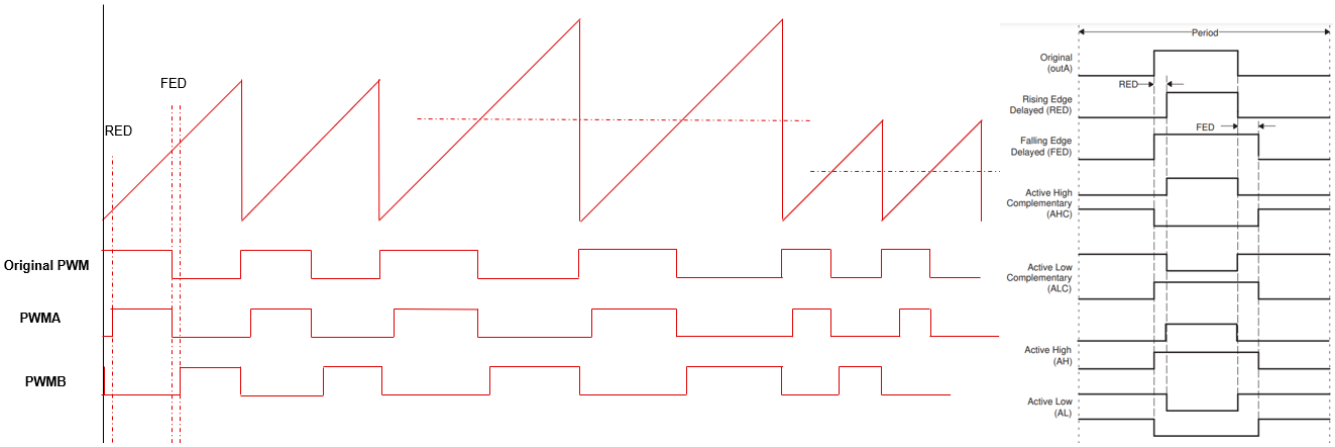

Figure 2-3. Primary Side Complementary PWM

Under certain special circumstances, LLC may not work under a fixed 50% duty cycle. For example, during power on, the converter normally requires soft-starting where the PWM duty cycle increases step-by-step to avoid problems like current inrush and output voltage over-shoot. With PWM generating logic proposed above, dead-band could be used to adjust the duty-cycle.

During power on, the dead-band Rising edge delay (RED) and Falling edge delay (FED) are set to a large value (0.95*period) and the duty cycle of both PWMA and PWMB would be limited to 5%. With the output voltage establishing, RED and FED could be decreased cycle-by-cycle and eventually down to normal dead-band value. As the result, PWMA and PWMB duty cycle would increase slowly until reaching up to 50%. The process of soft-starting is shown in Figure 2-4.

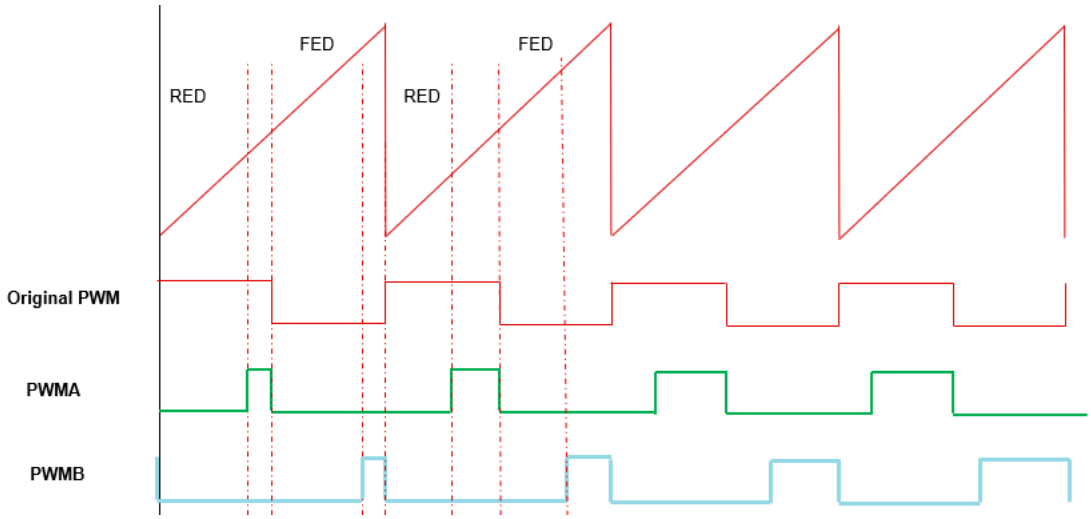

Figure 2-4. Leveraging Dead-Band to Achieve Soft-Starting

2.2 Secondary Side

With an increasing requirement for higher efficiency in LLC topology, synchronous rectification is becoming a must-have. Traditionally, it is difficult for an MCU to handle a multi-phase synchronous rectification topology, given the complex timing between the primary and secondary side, and between phases. However, the flexible type-4 PWM is making it possible with C2000.

Figure 2-5 shows the PWM configuration of synchronized rectification (SR) MOS. Note SR is using a separate PWM module from the primary side, thus a new set of CMPAs and CMPBs could be used with new action qualifier events. In order to ensure the safe operation of SR FETs, SR FETs are set to switch off slightly earlier than primary side FETs by setting $CMPA_S = CMPA_P - t_1$ and $CMPB_S = CMPB_P - t_1$. Meanwhile, the corresponding SR should also switch on later than the primary side switch, thus an AHC mode is used to delay the rising edge of the original SR signal to generate the PWM of SRA and complementary SRB. Considering a dead-band is existing in primary-side PWM, the dead-band on the secondary side must be large enough to make sure the SRx does not switch earlier than the primary side:

$DB_s > t_1 + DB_p$

To make the calculation easier, we could set t1= DB_p, thus:

$DB_s > 2*DB_p$

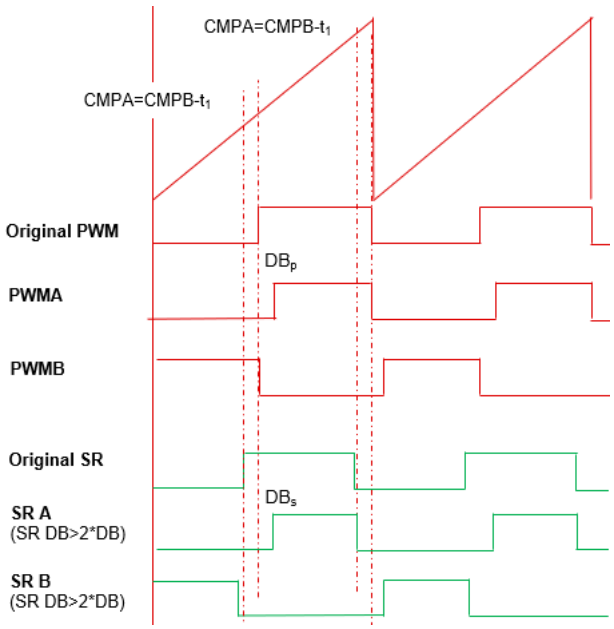

Figure 2-5. SR MOS PWM Configuration

3 Special Consideration

With the above configurations, the PWM of three-phase interleaved LLC is implemented with type-4 PWM on C2000, and the converter is supposed to work normally. In the following section, some corner cases are discussed to cover all the possible working conditions.

3.1 Phase 3 PWM Consideration

The PWM configuration of 3rd phase is shown in Figure 3-1. By following the principles mentioned above, the PWM can be generated easily. One special consideration is to make sure the comparator value for SR PWM always makes sense, which means:

$CMPB_S = CMPB_P - t_1 > 0$

$CMPA_S = CMPA_P - t_1 < PRD$

Considering $CMPB_P$ =1/6*PRD and $CMPA_P$ =2/3*PRD:

$T_1 < 1/6*PRD$

Normally, the T1 value is much smaller than PRD, and the conditions could be satisfied naturally. The condition needs to be checked especially when there is a huge frequency change or the PWM frequency is high. Note that if the loaded value of CMPx exceeds 0-PRD value range, the counter would never reach the comparator value and the configured action may not happen as expected. For information that shows the behavior if CMPA/CMPB is greater than the period, see the "Behavior if CMPA/CMPB is Greater than the Period" table within the technical reference manual.

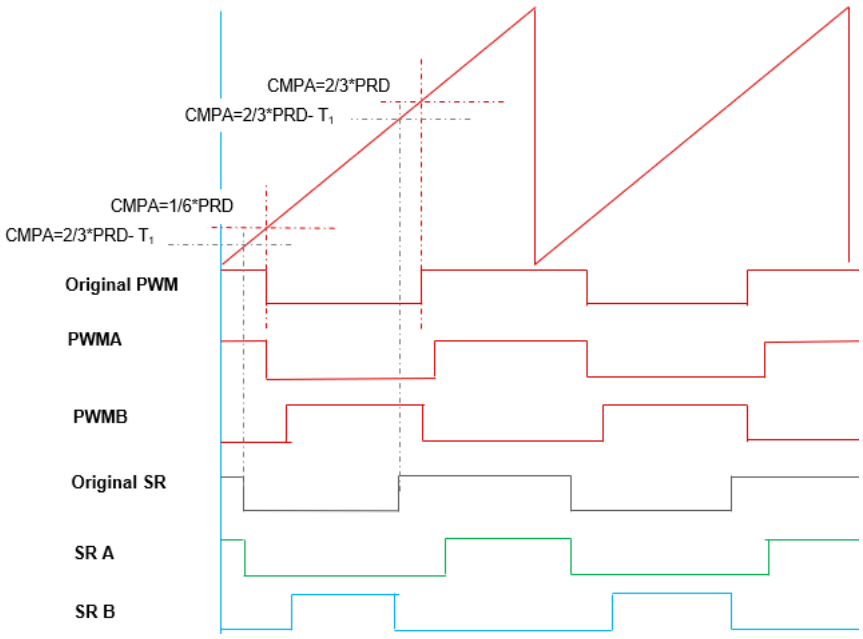

Figure 3-1. Phase 3 PWM Generation Logic

3.2 SR PWM Duty Limitation

Figure 3-2 represents a working condition where SR on time exceeds the resonant period LLC converter. If the PWM cycle actually crosses 2 PWM counter cycles, it may cause some disorder on PWM waveform when there is a huge frequency change.

When PWM frequency is lower than the resonant frequency of LLC, the on-time of SR switch needs to be limited. Otherwise, a reverse current would exist on SR MOS which would significantly influence the efficiency of the converter and even bring the converter to danger due to the reverse recovery of the body-diode.

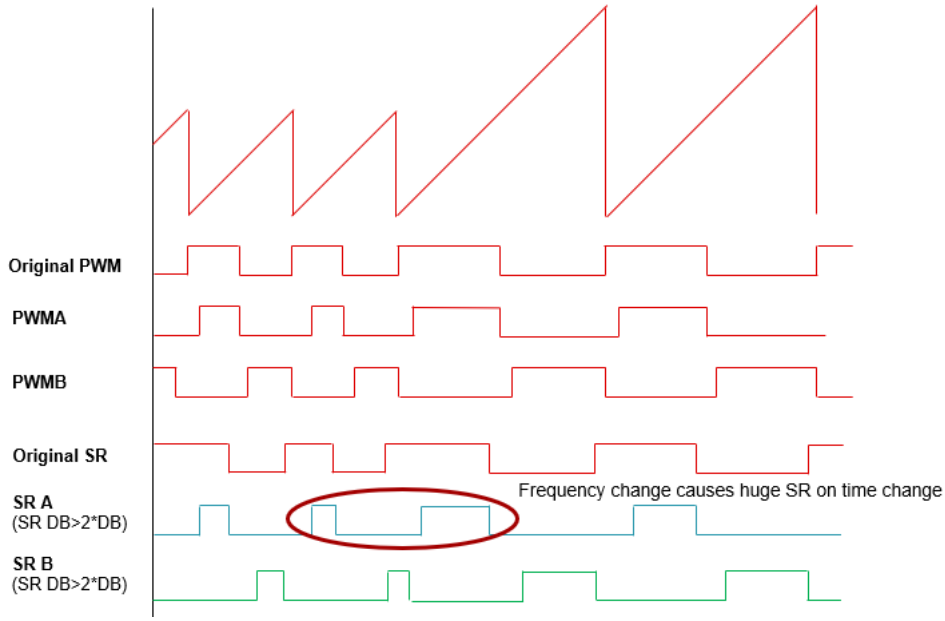

Figure 3-2. Example of SR On-Time Change

The CLB module on Gen 3 C2000 devices makes it easy to achieve highly flexible PWM waveforms. CLB implementation of PWM on time limitation is shown in Figure 3-3.

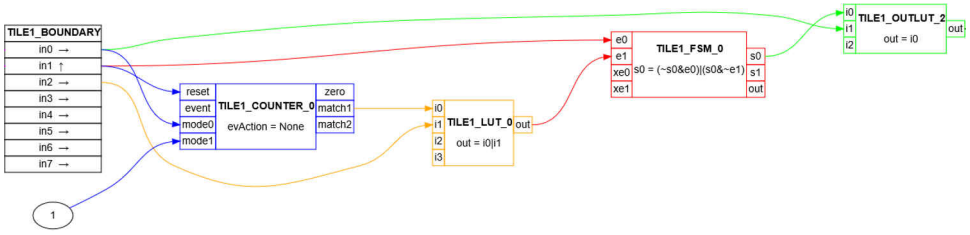

Figure 3-3. CLB Configuration

In this design, a counter is configured to limit the maximum on time of SR PWM. The counter would start to count once it receives the SR PWM rising edge and generate a pulse (match 1) when it reaches the configured match value. The match value decides maximum on time by CLB clock counts.

In LUT0, match signal is 'ORed' with input 2, which is the falling edge of original SR PWM, which is then connected into FSM_0. By correctly configuring FSM. e0 (rising edge of original PWM) would be able to pull high the S0 of FSM_S0, and e1 (falling edge of original PWM OR counter 0 match signal) would be able to pull down S0. By doing this, the S0 became the refined PWM which would be pulled down if the on-time exceeds the maximum value. The waveform of CLB internal signal is shown in Figure 3-4.

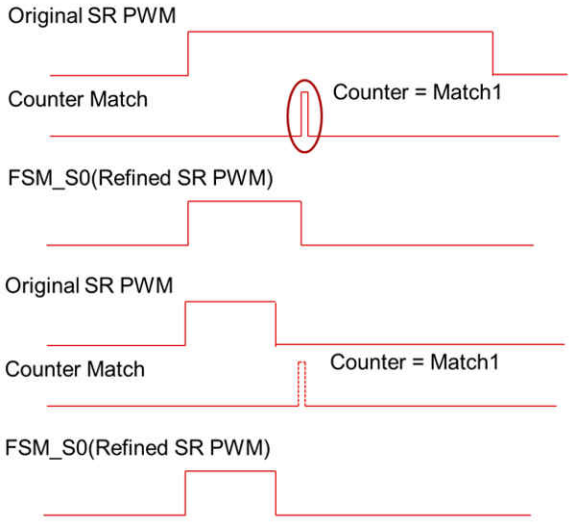

Figure 3-4. CLB Internal Waveform

Finally, FSM_S0 could be the CLB ouput through OUTLUT, and finally reflect back as PWM output by configuring CLB output MUX.

Table 29-3. Peripheral Signal Multiplexer Table

CLB Instance	CLB Output Signal	Peripheral Signal	Peripheral Name
		CLB1	
CLB1	CLB1_OUT0_0 (CLB1_OUT0)	PWMA	EPWM1
CLB1	CLB1_OUT1_0	PWMA_OE	EPWM1
CLB1	CLB1_OUT2_0	PWMB	EPWM1
CLB1	CLB1_OUT3_0	PWMB_OE	EPWM1
CLB1	CLB1_OUT4_0	AQ_PWMA	EPWM1
CLB1	CLB1_OUT5_0	AQ_PWMB	EPWM1
CLB1	CLB1_OUT6_0	DB_PWMA	EPWM1
CLB1	CLB1_OUT7_0	DB_PWMB	EPWM1
CLB1	CLB1_OUT0_1 (CLB1_OUT8)	QA	EQEP1
CLB1	CLB1_OUT1_1 (CLB1_OUT9)	QB	EQEP1
CLB1	CLB1_OUT2_1	QDIR	EQEP1
CLB1	CLB1_OUT3_1	QCLK	EQEP1
CLB1	CLB1_OUT4_1	MUX 1.2	All XBARs (CLB, OUTPUT, EPWM)
CLB1	CLB1_OUT5_1	MUX 3.2	All XBARs (CLB, OUTPUT, EPWM)
CLB1	CLB1_OUT6_1	ECAP IN 16	ECAP1, ECAP2
CLB1	CLB1_OUT7_1	ECAP IN 17	ECAP1, ECAP2
CLB1	CLB_OUT16 (CLB_OUT0_2)		CLB Global Mux
CLB1	CLB_OUT17 (CLB_OUT1_2)		CLB Global Mux
CLB1	CLB_OUT18		CLB Global Mux
CLB1	CLB_OUT19		CLB Global Mux
CLB1	CLB_OUT20		CLB Global Mux
CLB1	CLB_OUT21		CLB Global Mux
CLB1	CLB_OUT22		CLB Global Mux
CLB1	CLB_OUT23		CLB Global Mux

Figure 3-5. Multiple CLB Out is Connected to Peripheral via Multiplexer

Figure 3-6 shows the waveform when the PWM cycle is changing from 3 µs to 15 µs while the maximum on-time is limited to 5 µs. As the waveform shows, the refined PWM is pulled down immediately when the on time reaches 5 µs, thus this feature could be leveraged to limit the reverse current on SR FET in LLC convert.

Figure 3-6. PWM Limitation

4 References

- Texas Instruments: *Designing With The C2000 Configurable Logic Block*
- Texas Instruments: *TMS320F28004x Real-Time Microcontrollers Technical Reference Manual*

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