Application Note

Hardware Design Guide for F2800x C2000™ Real-Time MCU Series

Peter Luong

ABSTRACT

The third-generation family of C2000™ devices are powerful microcontrollers designed for complex systems where real-time control is essential, especially crucial in many automotive and industrial applications. These devices feature high-speed, low-latency integrated analog and control peripherals, allowing users to consolidate their controls and communication designs. This application report serves as guidance for developing hardware with these entry and mid-performance devices. In particular, information is provided for system level hardware design, part selection, schematic design, and layout recommendations. It is an essential guide for hardware developers using C2000 devices and helps streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements, general-purpose input/output (GPIO) connections, analog inputs and ADC, clocking generation and requirements, and JTAG debugging, among many others. A useful checklist is provided in Section 6 which can be used to review schematic and layout designs.

Of the third-generation of C2000 devices, this document only applies to the F280013x, F28002x, F28003x, and F28004x families. It does not apply to F2807x, F2837xS, F2837xD, F2838xS, and F2838xD.

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1 Introduction

The C2000 family of real-time microcontrollers come in a range of performance packages with varying pin packages, flash size, performance, and feature sets. This large portfolio allows for a wide variety of applications in processing, sensing and actuation. All of the TMS320F2800x devices (F280013x, F28002x, F28003x, and F28004x) feature the industry-leading TMS320C28x 32-bit digital signal processor (DSP) core and run at frequencies of 100 MHz or higher. This, along with an arithmetically-tuned instruction set, allow the C2000 MCU to run floating or fixed-point code in ultra-low latency control systems. Performance-wise, the entry and mid-performance F2800x devices range in flash sizes up to 384KB and have RAM sizes up to 100KB.

The increase in processing power and advancements in power-reduction have allowed for extremely capable devices, but have also greatly increased the complexity of designing with the C2000 MCUs. While the C2000 family of microcontrollers still remains a very scalable device, these advancements come with additional analog challenges. What is the optimal device for my system? What additional components should be added to increase stability? What layout considerations should be taken to maximize device performance? All of this information, as well as other key criteria, are outlined in this application report.

Note

The current revisions on all device-specific data manuals take precedence over the information/data in this report. This document offers guidance on best practices when designing systems with F2800x microcontrollers. For detailed device information, see the device-specific data sheet and technical reference manuals.

2 Typical F2800x System Block Diagram

A diagram of a typical C2000-based control system is pictured in Figure 2-1. The microcontroller is powered through a power supply system that accommodates the primary voltage rails, which include a 3.3 V analog voltage (VDDA), 3.3 V digital voltage (VDDIO), and a 1.2 V core power rail (VDD). The C2000 device offers rich peripheral support, and C2000-based systems typically consist of the following circuitry connected to the MCU: power management, signal conditioning of analog inputs, crystal or external oscillator, reset circuitry, communication transceivers, external interface to digital IO pins, digital sensing, pulse width modulation (PWM) interface/drivers, and any other required supporting circuitry.

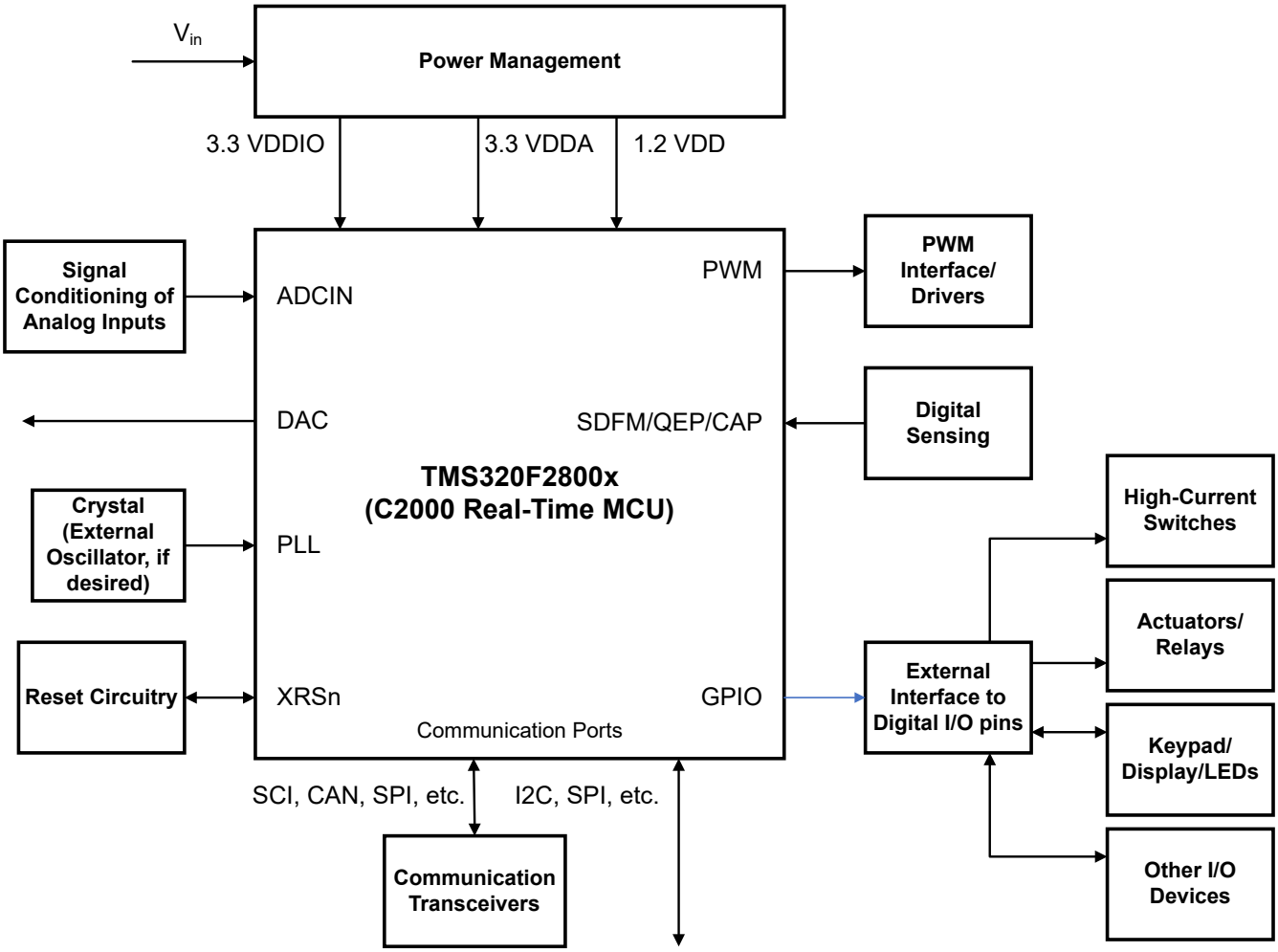

Figure 2-1. Typical TMS320F2800x System

These TMS320F2800x MCUs are complex devices, which make creating a custom well-designed board that utilizes many of the integrated peripherals a great challenge. Though not all of the included peripherals are necessary relevant in all cases, it remains imperative to become familiar with the C2000 device prior to attempting a design. Great care must be taken throughout the entire process to ensure the best and most optimized device performance. The areas which remain especially challenging include being careful about all of the different internal blocks running at different frequencies, maintaining signal integrity amongst all onboard analog signals, and EMI/EMC considerations.

3 Schematic Design

The following sections outline the steps required to design an initial schematic with the C2000 device. It details information pertaining to choosing a package, understanding the features and integrated peripherals within the device, and all of the necessary considerations to improve system and device performance.

3.1 Package and Device Decision

Determining the correct C2000 device is the first step in designing and integrating TI's C2000 platform into a system. Apart from cost and availability, peripheral support is one of the most important determining factors when considering which TMS320F2800x device to implement in the system. Performance of the C2000 device often correlates with the numbering of the device (F28002x is an entry-performance chip and F28004x is a mid-performance chip). In addition, newer devices may often include new onboard peripherals or updated versions of existing peripherals. Each device comes in various packages and form factors. For more information about the sizing of each chip package, see the *Mechanical Data* section in the device-specific data sheet.

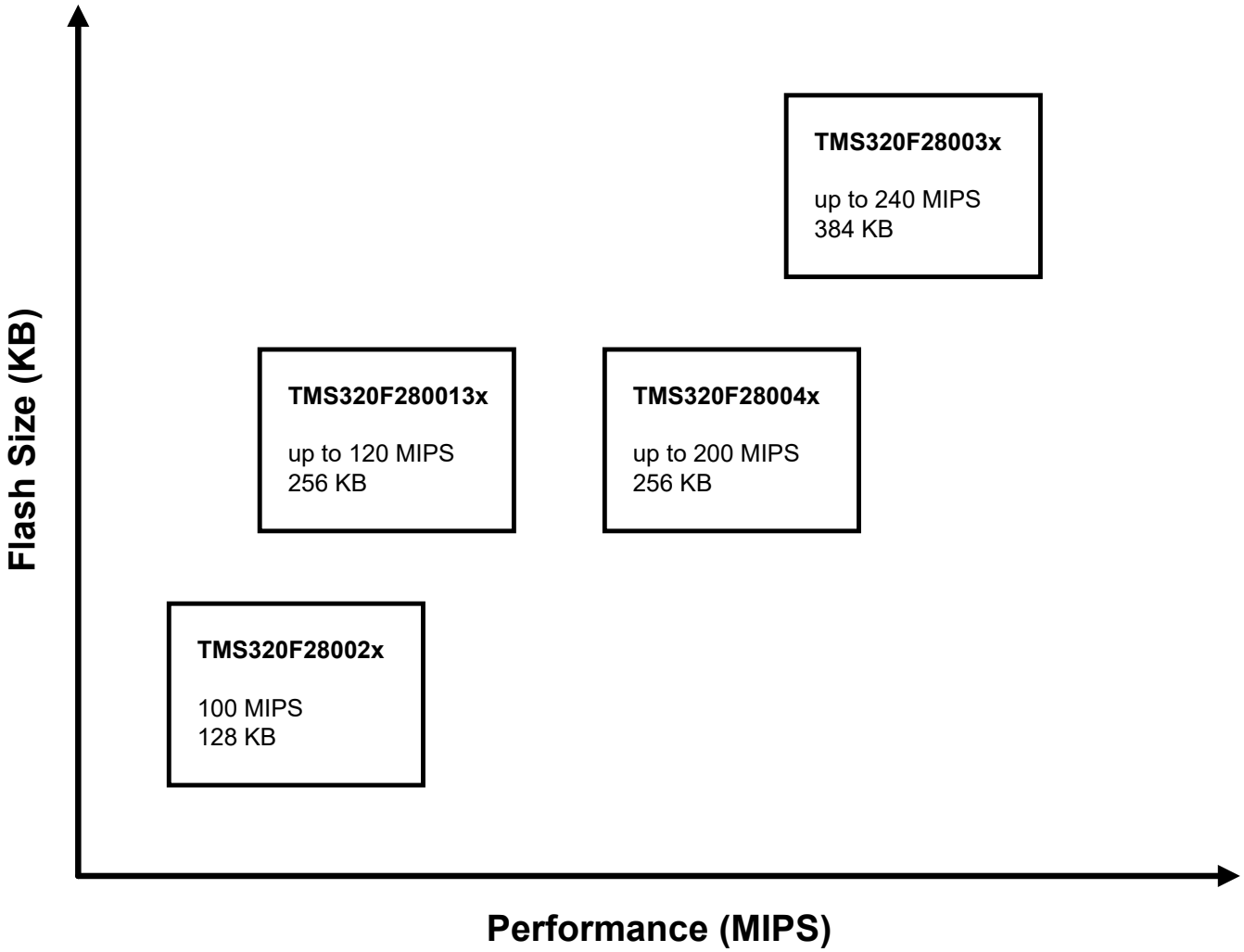

Figure 3-1. Entry and Mid-Performance C2000 MCUs by Flash Memory & Performance

3.1.1 F2800x Devices

The entry and mid-performance C2000 devices come in a variety of package options to perfectly fit a wide range of applications and systems. The C2000 devices are available in entry-performance packages for simple control systems as well as higher-performance packages for feature-rich systems. The main devices of F280013x, F28002x, F28003x, and F28004x are distinct families with different device specs and features. Branching further, each of these devices come in varying packages and pinouts. This gives a large device and pin-package library of which to choose from for designing systems. This enables users the ability to implement their systems with adequately-tuned peripheral support at an optimized cost.

All F2800x devices offer support for many communication peripherals, including CAN, I2C, SCI, SPI, LIN, PMBus, and FSI. With regard to analog peripherals, all of these devices include varying numbers of 12-bit ADCs, external ADC channels, and windowed comparators (CMPSS) with reference DACs. Control peripherals include eCAPs, ePWMs, and eQEPs.

For an exhaustive overview of the peripheral support for each of TI's available C2000 devices, see the *C2000 Real-Time Control MCU Peripherals Reference Guide*.

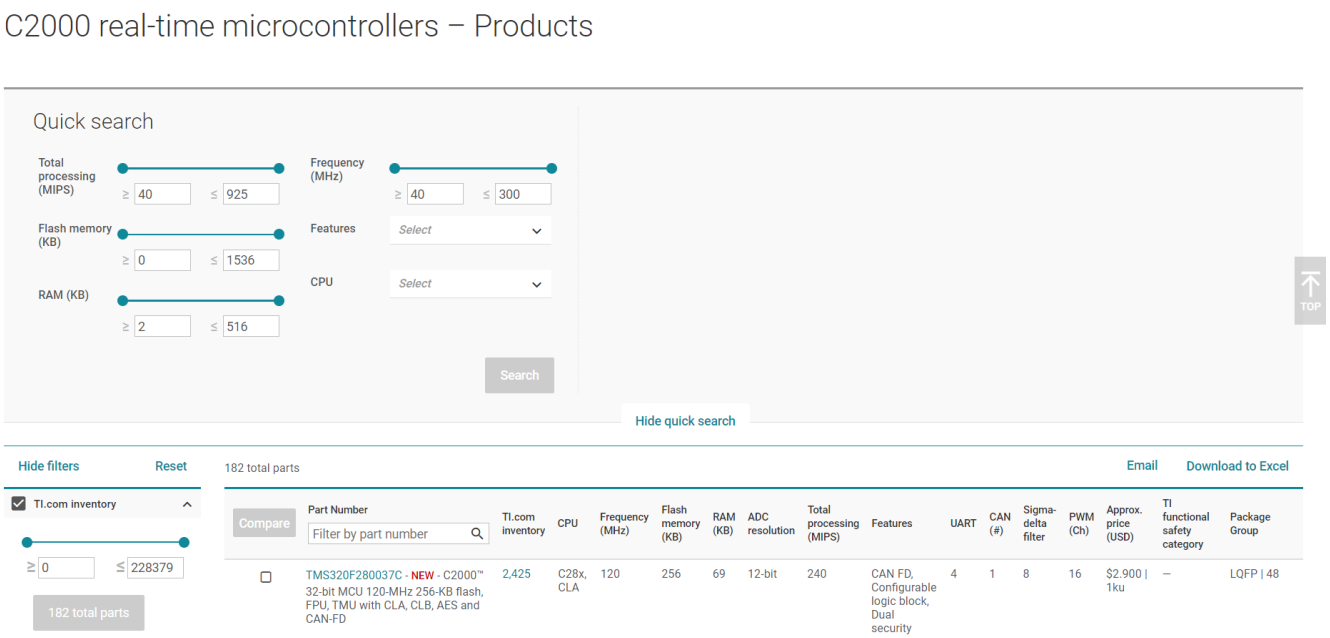

Figure 3-2. TI C2000 Product Selection Page

The C2000 product selection page offers the ability to search and filter devices by specifications such as frequency, flash size, RAM, ADC resolution, MIPS, and number of peripherals. Once the system requirements have been finalized, this tool can be a useful way to provide guidance on which specific packages would be a good fit for the system being built.

3.1.1.1 TMS320F28004x

The earliest microcontroller in this family of entry and mid-performance devices is the TMS320F28004x. It features a single-precision Floating-Point Unit (FPU) and a Trigonometric Math Unit (TMU), as well as Viterbi/ Complex Math Unit (VCU-I). This device runs at 100 MHz, has 100 KB of random-access memory (RAM), and is equipped with 128 KB or 256 KB of flash memory, depending on the package. This device comes in a 56-pin, 64-pin, and 100-pin package options which sport between 24 and 40 GPIO inputs and between 12 and 21 AIO inputs. It also features 4 configurable logic block (CLB) tiles and a programmable control law accelerator (CLA) clocked at 100 MHz.

In addition to the standard peripherals, the F28004x MCU contains 4–7 programmable gain amplifiers (PGA). It also has support for high-resolution CAPs and high-resolution PWMs on specified pins, and it contains 3 to 4 sigma delta filter modules (SDFM).

For more in-depth information about the TMS320F28004x device, see the *TMS320F28004x Real-Time Microcontrollers Data Sheet*.

3.1.1.2 TMS320F28002x

The TMS320F28002x device is an inexpensive entry-performance device fit for simple real-time control systems. It features an updated TMS320C28x 32-bit CPU possessing an improved Floating-Point Unit (FPU) with support for Fast Integer Division (FINTDIV) and improved Trigonometric Math Unit (TMU) with support for Nonlinear Proportional Integral Derivative (NLPID) control. This controller also features cyclical redundancy check (VCRC) extended instruction set.

The F28002x device is clocked at 100 MHz, has 24 KB of total RAM, and comes in pin configurations with 32 KB, 64 KB and 128 KB of flash memory. This device features 2 CLB tiles, 16 to 39 GPIO pins, and 14 to 16 AIO pins. The F28002x device features all of the standard analog, control, and communication peripherals. New to C2000 platform is the Host Interface Controller which allows for access to internal memory from an external host. Of special note is that this device does not include an onboard digital-to-analog converter (DAC) or Sigma-Delta Filter Modules (SDFM). Systems that require these peripherals will need to utilize TMS320F28004x or TMS320F28003x MCUs.

For more in-depth information about the TMS320F28002x device, see the *TMS320F28002x Real-Time Microcontrollers Data Sheet*.

3.1.1.3 TMS320F28003x

The TMS320F28003x features the updated FPU and TMU units, as well as VCRC extended instruction set. This device has a frequency of 120 MHz, contains up to 384 KB of flash memory, and sports 69 KB of volatile memory (RAM). It features 4 CLB tiles and a CLA. Inputs include up to 51 GPIO pins and up to 23 AIO pins.

This device once again features the standard peripherals common in the specified C2000 devices with some improved versions of specific peripherals, including support for CAN with flexible data rates (MCAN/CAN FD). In addition, F28003x chip sports sigma delta filter modules as is seen on the F28004x device. This device also has the Host Interface Controller introduced in F28002x. New F28003x peripherals include Advanced Encryption Standard (AES) accelerator, Embedded Pattern Generator (EPG), Secure Boot and JTAG Lock, and Live Firmware Update (LFU).

For more in-depth information about the TMS320F28003x device, refer to the *TMS320F28003x Real-Time Microcontrollers Data Sheet*.

3.1.1.4 TMS320F280013x

The TMS320F280013x device is a cost-optimized member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics. This device's low cost allows it to function in an even wider variety of applications beyond normal real-time control systems. It runs at 120 MHz and features up to 256 KB of flash and 36 KB of RAM.

For more in-depth information about the TMS320F280013x device, see the *TMS320F280013x Real-Time Microcontrollers Data Sheet*.

3.1.2 Migration Guides

When developing with C2000 microcontrollers, it is often very beneficial to transition to newer devices for added peripheral support, enhanced feature sets, and improved system optimization. TI provides a variety of documentation which assists in transitioning from older C2000 devices to newer ones and even between the newer generation of C2000 MCUs. In addition to reviewing the data sheets for each device and overviewing the supported peripherals and onboard functional blocks, it can be helpful to review these guides for specific key differences, which is especially useful if a user is already familiar with one device out of the C2000 family of microcontrollers.

The following are a list of available migration resources for transitioning from older C2000 devices to newer ones and between the newer MCUs:

- *TMS320F2802x/TMS320F2803x to TMS320F28002x Migration Overview*
- *The TMS320F28004x Microcontroller: A Comparison to the TMS320F2806x and TMS320F2803x Microcontrollers*

- *Migration Between TMS320F28004x and TMS320F28002x*
- *Migration Between TMS320F28002x and TMS320F28003x*
- *Migration Between TMS320F28004x and TMS320F28003x*

3.1.3 PinMux Tool

For a more streamlined pin assignment process, TI has developed a software tool known as the PinMux utility. This utility provides a graphical user interface for configuring pin multiplexing settings and resolving pin conflicts for C2000 devices. There is a deprecated standalone version of this software, but the most updated version can be found in TI's SysConfig application. This tool, along with helping automate the pin configuration process, is a GUI that also aids in configuring peripherals, subsystems, and other components within TI's devices. The SysConfig tool helps manage, expose, and resolve any device conflicts in real-time to ensure correct device configurations. The SysConfig tool can be found in three different forms: a standalone application, an integrated GUI within Code Composer Studio™, and an online cloud version.

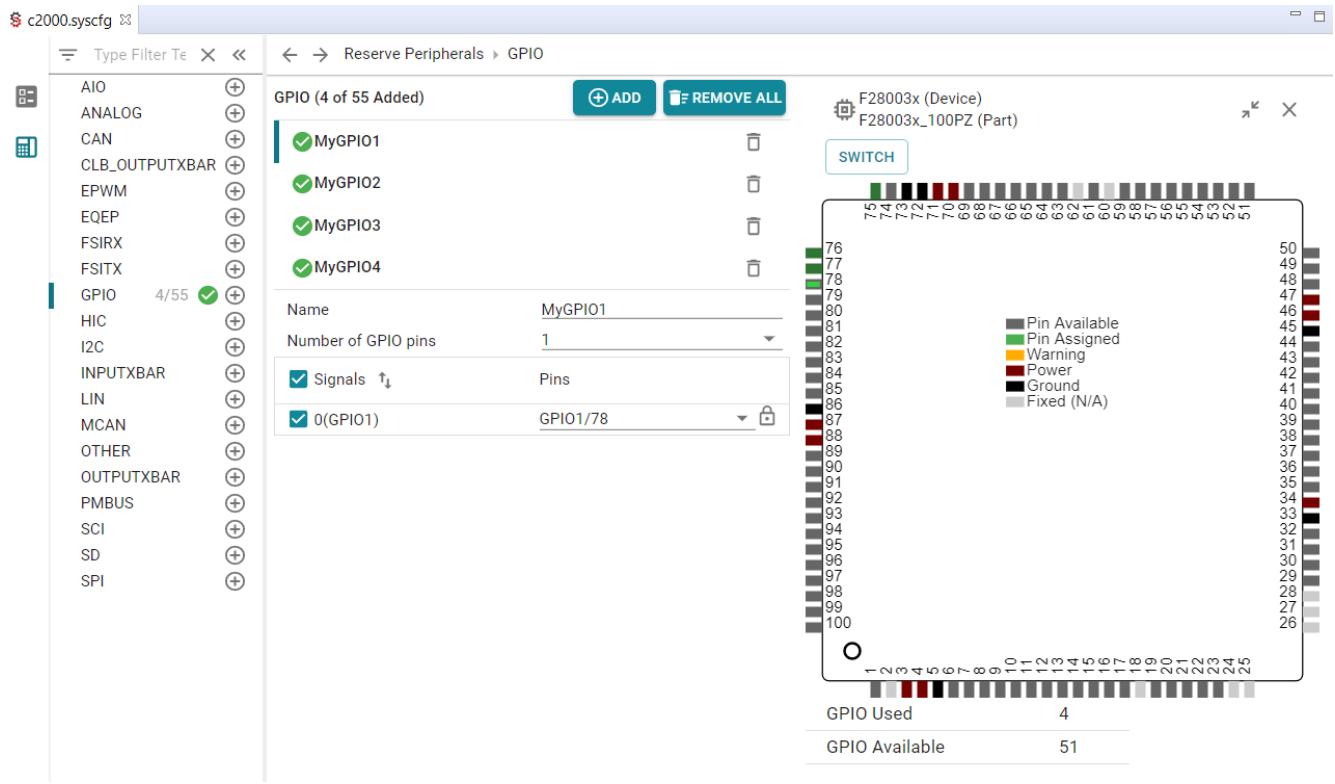

Figure 3-3. PinMux Tool Within SysConfig

3.1.4 Configurable Logic Block

The configurable logic block (CLB) is an on-device peripheral that is available on F28002x, F28003x, and F28004x devices. The CLB peripheral contains a collection of logic blocks that can be combined to create custom digital logic. It features counters, LUTs, FSMs, output LUTs, and a high-level controller. The CLB has various interconnections with the other peripherals available on the C2000 device, allowing the CLB to enhance and expand their functionality. Through this robust peripheral, functions that would have normally required external logic devices can be accomplished directly within the MCU. This is advantageous as it often reduces the need to incorporate external devices like FPGAs and CPLDs, leading to reduced board and system costs.

More detailed information about the CLB and a comparison of external logic devices to the CLB can be found in *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers*.

3.2 Digital IOs

This section describes the digital signals present within the device, ranging from GPIOs to integrated communication and control peripheral support.

3.2.1 General Purpose Input/Outputs

The TMS320F2800x microcontrollers contain varying numbers of general purpose I/O (GPIO) pins. They serve as the digital inputs and outputs of the device, and these GPIO-enabled pins can be configured to be used either as typical GPIOs or as peripheral I/O signals. This design grants great flexibility when using the C2000 devices in different applications. Up to 12 independent peripheral signals are multiplexed on a single GPIO-enabled pin, and the same peripheral can be multiplexed onto multiple GPIO pins.

For each GPIO-pin, the max drive strength (sink/source current) is 4 mA. The maximum toggling frequency for F28002x/F28004x is 25 MHz with a rise/fall time of 8 ns. Note for F28004x, this applies to all GPIOs except for GPIO23_VSW. For F280013x/F28003x, this maximum toggling frequency is 50 MHz with the same rise/fall time of 8 ns.

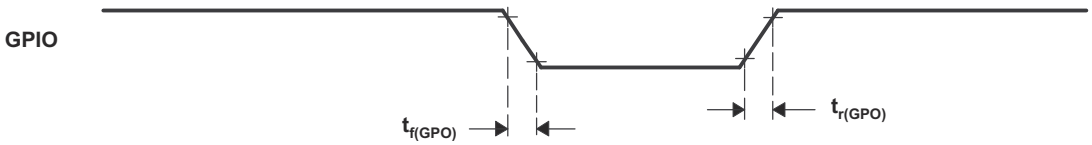

Figure 3-4. GPIO Output Timing

At reset, the GPIO pins are defined as inputs, and they all have internal pull-ups which are disabled on device boot and at reset. These pull-ups can be selectively enabled or disabled through software. To avoid any floating unbonded inputs, the Boot ROM will automatically enable internal pullups on GPIO pins that are not bonded out in a particular package. Additionally, all GPIO pins are high-impedance during device boot and until they are configured in firmware. **This means that PWM signals, relay drivers, chip selects, and so forth should have external pull-resistors to enforce a state during power-up.**

As an additional feature, GPIO inputs allow the user to filter out any unwanted noise glitches through input qualification. There are three available options for input qualification: no synchronization (asynchronous input), synchronization to SYSCLKOUT, and qualification using a sampling window. Pins that are configured as peripheral inputs can be configured with any of the three options. The GPIO-configured pins only have access to SYSCLKOUT synchronization and qualification using a sampling window. More detailed information about this feature and how to design around it can be found in the *Input Qualification* section of the device-specific Technical Reference Manuals.

In addition to configuring the pin selection of the device, it is also essential to be aware of best practices when making use of the general purpose I/O (GPIO) resources on the device. C2000 devices continually integrate more onboard analog peripherals, like ADCs, DACs, PGAs, and CMPSSs, which help to reduce system level cost. These additional peripherals, however, lead to reduced GPIO availability when trying to maintain similar pin-packages. Thus, it is important to maximize GPIO usage when designing a custom system. TI offers a guide on *How to Maximize GPIO Usage in C2000 Devices* that provides common suggestions on GPIO usage and how to reduce the need for IO expanders.

3.2.2 Integrated Peripherals and X-BARs

As mentioned earlier, each peripheral signal is multiplexed to many GPIO pins to ease the design and layout process and allow for maximal flexibility. For a detailed table listing all of the available GPIO peripheral pin configurations, see the *Pin Attributes* table in the data sheet for each device.

To route the signals from a GPIO to any of the different IP blocks—such as the ADCs, eCAPs, ePWMs, and external interrupts—the devices make use of input crossbars (X-BAR). The Input X-BAR has access to every GPIO and can route each signal to any (or multiple) of the IP blocks mentioned previously, as well as the digital input sides of the AIOs. In essence, the Input X-BARs give the ability to route the output of one peripheral to another. These C2000 MCU devices also contain GPIO Output X-BARs, which take signals from inside the device and bring them out to a GPIO.

Apart from these two crossbars, each device also contains two other kinds of X-BARs: ePWM X-BARs and CLB X-BARs. As the names imply, the ePWM X-BAR is responsible for routing signals into the ePWM modules and CLB X-BAR is responsible for routing signals to the CLB. The CLB itself also has access to CLB INPUT X-BAR and CLB OUTPUT X-BAR, which enable the ability to route signals from the GPIO pins to the CLB as inputs or outputs. The ePWM X-BAR is connected to the Digital Compare (DC) submodule of each ePWM module for actions such as tripzones and syncing.

3.2.3 Control Peripherals

The F2800x devices contain varying numbers of the following control peripherals:

- Enhanced Capture (eCAP) and High-Resolution Capture Submodule (HRCAP)
- Enhanced Pulse Width Modulator (ePWM) and High-Resolution Pulse Width Modulator (HRPWM)
- Enhanced Quadrature Encoder Pulse (eQEP)
- Sigma-Delta Filter Module (SDFM)

For specific control peripherals, their performance can be greatly impacted by the design of the board. Be sure to follow the layout guidelines outlined in Section 4 to reduce unwanted noise and maximize performance.

The Sigma-Delta Filter Module (SDFM) is available on TMS320F28003x and TMS320F28004x devices and is used with external sigma-delta modulators for current measurement and resolver position decoding in motor control applications. The SDFM makes use of an outside clock through its SDFM clock input pins, and its operation is susceptible to corruption if the clock is especially noisy. Special precaution should be taken on these signals to ensure a clean and glitch-free signal that meets the SDFM timing requirements detailed in the device-specific data sheet. Thus, it recommended to use series termination resistors for ringing due to any impedance mismatch of the clock driver and to space these traces away from other noisy signals. This helps to ensure proper SDFM functionality. Making use of the SDFM Synchronized GPIO (SYNC) option, (synchronizing the clock pins to PLLRAWCLK, can provide protection and help maintain SDFM operation against occasional clock glitches). It should be noted that there are limitations to its protection, so ensuring stable clocking is a top priority for proper SDFM function. For specific SDFM timing requirements, see the device-specific data sheet.

3.2.4 Communication Peripherals

The F2800x devices contain varying numbers of the following communication peripherals:

- Controller Area Network (CAN/DCAN)
- Modular Controller Area Network (MCAN/CAN FD)
- Inter-Integrated Circuit (I2C)
- Power Management Bus (PMBus) Interface
- Serial Communication Interface (SCI)
- Serial Peripheral Interface (SPI)
- Local Interconnect Network (LIN)
- Fast Serial Interface (FSI)
- Host Interface Controller (HIC)

Because of the nature of these peripherals and the different means through which they communicate, each system must be designed with the intended comm peripheral support in mind. Board-level interfaces, which include I2C, PMBus, and SPI, are connected to other devices, either on the board or through the system. Because these drivers are normally run directly, be sure to pay close attention to the drive capability and trace length. These factors depend on the selected frequency of these signals.

When making use of CAN, it is recommended to implement an external oscillator on the board as opposed to using the internal oscillator. Depending on the required CAN parameters like bit time settings, bit rate, bus length, and propagation delay, the accuracy of the on-chip zero-pin oscillator may not meet the requirements of the CAN protocol. More information about this can be found in Section 3.6.1 as well as the *Programming Examples and Debug Strategies for the DCAN Module*.

Notably for I2C, it is recommended that the SDAA and SCLA pins are pulled high using external pull-up resistors. Too strong of a pull-up (smaller resistor value) prevents the I2C pins from effectively being driven low, whereas too weak of a pull-up (larger resistor value) can impact the communication speeds. This value should be selected based on a compromise between power consumption and speed. To calculate the idea pull-up resistor range, refer to application report *I2C Bus Pullup Resistor Calculation*.

Interfaces that can connect two or more boards running under different processors include SCI, CAN, LIN, and FSI. These ports often require specialized transceiver parts that transform the electrical signal to combat noise and enable communication with the ports on other devices. When using a communication transceiver, some transceivers may require pull-up resistors on the communication pins of the MCU. Verify this requirement with the transceiver's data sheet.

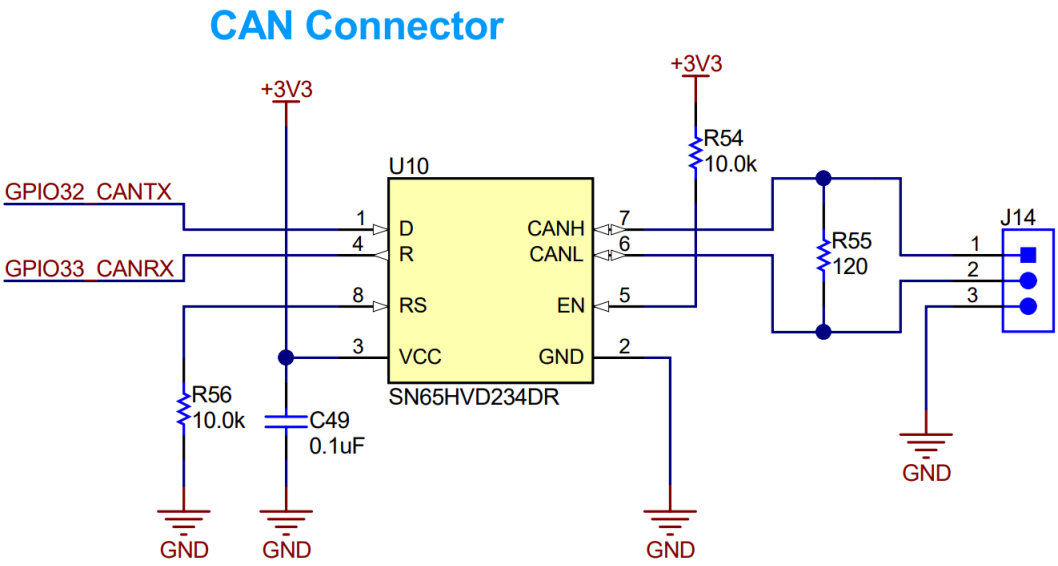

Figure 3-5. CAN Transceiver in LAUNCHXL-F280049C

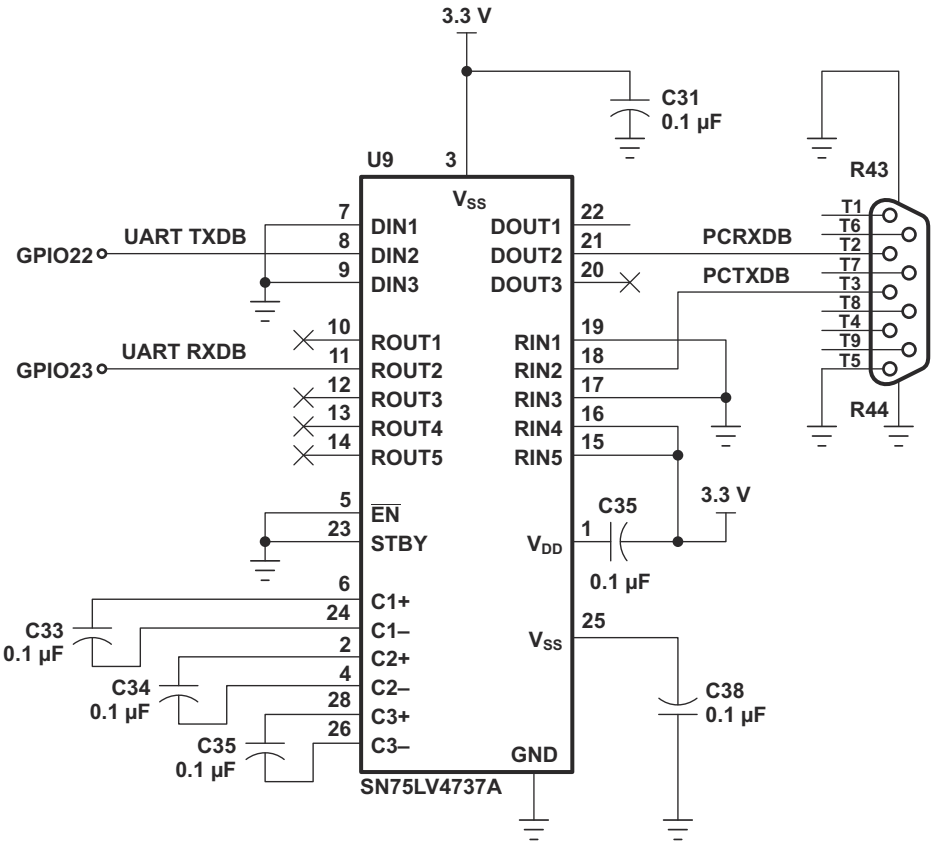

Figure 3-6. Typical RS-232 Transceiver

The SCI communication peripheral is a 2-wire asynchronous serial port with two external pins, SCITXD (SCI transmit-output) and SCIRXD (SCI receive-input). This protocol is commonly referred to as UART, and the protocol on the C2000 devices use the standard NRZ format. For some transceiver implementations, it is recommended to have a pull-up resistor on the SCI-RX pin to allow for the signal to return to high logic level without being driven. This prevents that GPIO pin from floating between values which would lead to errors and increased current consumption. Verify this pull-up resistor requirement with the data sheet of the specific transceiver being used. The pull-up resistor is especially necessary when using some types of transceivers to ensure deterministic operation of the SCI module. This resistor value should be selectively chosen and tested within the system, as the ideal value is highly dependent on the particular application. Too weak of a pull-up value (larger resistance) would prevent the resistor from actually pulling up a tri-stated or floating output from another device. Likewise, too strong of a pull-up value (smaller resistance) would prevent the output signal from toggling from the other device. A good starting point for experimenting this value would be 10 kΩ. For more information about debugging and troubleshooting SCI transmissions, see the SCI FAQ Thread on E2E.

For additional reference material for various communication peripheral protocols, see the following documentation:

- *TMDSFSIADAPEVM FSI Adapter Board User's Guide*
- *Fast Serial Interface (FSI) Skew Compensation*

3.2.5 Boot Pins and Boot Peripherals

The device boot ROM contains bootloading software. When the C2000 device powers on (or upon reset) and after it has been initialized, the bootloader will determine the boot mode to execute. Each device features two GPIO boot pins whose states indicate the desired boot mode to boot in. By default, these two boot pins are GPIO24 and GPIO32. The four default boot modes are parallel IO, SCI/Wait boot, CAN, and Flash.

To ensure a defined state during boot, place pull resistors at the GPIO boot pins. Users may choose to have weak pull-ups for boot mode pins if they use a peripheral on these pins as well, so the pull-ups can be overdriven. Apart from being used as boot pins, they can also be used in the application only as outputs whose state is irrelevant during boot and as inputs if it can be guaranteed that the signal will only be driven the desired way.

Table 3-1. Device Default Boot Modes

BOOT MODE	GPIO24 (DEFAULT BOOT MODE SELECT PIN 1)	GPIO32 (DEFAULT BOOT MODE SELECT PIN 0)
Parallel IO	0	0
SCI/Wait boot	0	1
CAN	1	0
Flash	1	1

All F2800x devices feature the ability to assign custom boot mode select pins (BMSP), ranging from 0 pins up to 3 pins. From these, the user is then able to create a custom boot table with support for 1 configured boot mode all the way to 8 configured boot modes. To change the factory default boot mode pins, program the user-configurable Dual Mode Security Module (DCSM) one-time programmable memory (OTP) locations. For select communication peripherals (ex. SCI, MCAN, DCAN, I2C, SPI), there are default and alternative GPIOs that the device expects to boot from. For more information on this, see the *GPIO Assignments* section in the device-specific data sheet.

3.3 Analog IOs

This section describes the key careabouts when dealing with analog signals on the device. It describes key information such as choosing ADC pins and analog references.

3.3.1 Analog Peripherals

The F2800x devices contain varying numbers of the following analog peripherals:

- Analog-to-Digital Converter (ADC)
- Programmable Gain Amplifier (PGA) (exclusive to F28004x)
- Temperature Sensor
- Buffered Digital-to-Analog Converter (DAC)
- Comparator Subsystem (CMPSS)

3.3.2 Choosing Analog Pins

Like the GPIO pins, the analog peripherals offer flexible pin usage. Buffered DAC outputs, CMPSS inputs, PGA functions, and digital inputs are multiplexed with ADC inputs. Furthermore, all ADCs have an internal connection to VREFLO allowing for offset self-calibration.

When choosing analog pin connections, take into consideration the peripherals available on each pin. Analog inputs with comparators allow for those analog signals to be able to quickly trip PWMs (as a fault signal) or to detect zero-crossing. Because these devices contain multiple ADCs, also consider if sampling certain analog signals simultaneously is beneficial. In these situations, three simultaneous analog signals could be connected to ADC-A, ADC-B, and ADC-C.

The F2800x devices feature varying numbers of digital GPIOs multiplexed with analog pins. These are known as AIOs and AGPIOs. All of the F2800x devices feature AIOs, which are multiplexed analog pins that can only function in input mode. By default, they will function as analog pins while the GPIOs are in a high-impedance (high-Z) state. A new type of analog pin is the AGPIO. These are available on F28003x and F280013x, which feature both AIOs and AGPIOs. These AGPIOs function similarly to AIOs except that they offer full input and output capabilities. By default, the AGPIOs are not connected and have to be configured. Note that if digital signals with sharp edges are connected to the AIOs or AGPIOs, cross-talk can potentially occur on directly adjacent analog signals.

3.3.3 Internal vs. External Analog Reference

The ADCs onboard use VREFHIx and VREFLOx as voltage references. For most applications, the internal voltage references offer sufficient performance. The VREFHIx pin voltage is thus driven by an internal bandgap voltage reference whose voltage can be selected as a 1.65 V output (0 V to 3.3 V) or a 2.5 V output (0 V to 2.5 V). If even more accuracy is a design requirement for the system being implemented, then an external reference voltage can be used instead.

When using the internal reference mode, no additional voltage sources should be placed on the VREFHI pin as the voltage is driven onto this pin by the device itself. In external reference mode, externally drive the high reference voltage pin using an external circuit, such as REF3030 and high-speed operational amplifier. This voltage must be 2.4 V to VDDA. In all instances, ensure a 2.2 µF capacitor is placed on the pin.

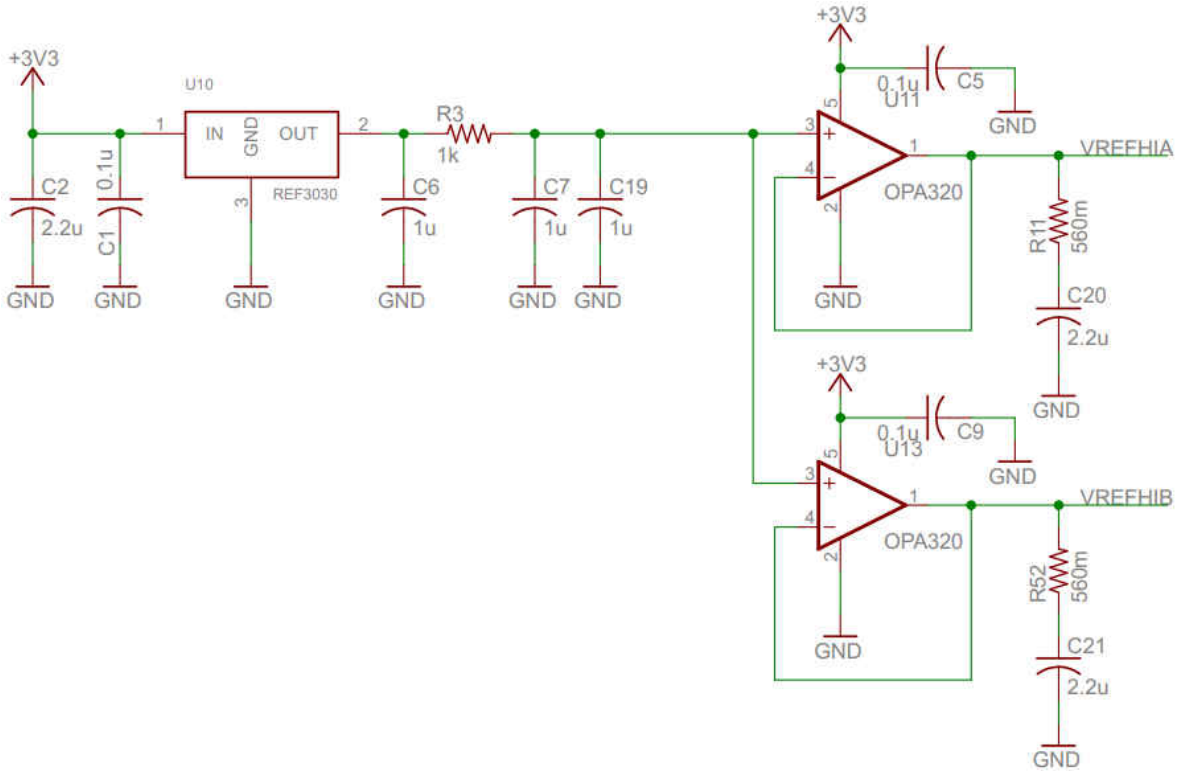

Figure 3-7. Reference Circuitry for External Analog Reference

3.3.4 ADC Inputs

The ADCs should be properly designed and evaluated to ensure proper performance. The analog-to-digital converters have input impedance and bandwidth requirements which could lead to memory cross-talk and significant sample-and-hold (S+H) circuit settling errors.

The diagram below outlines the ADC Input Model, where C_p describes the parasitic input capacitance, R_{on} describes the sampling switch resistance, C_h describes the sampling capacitor, and R_s describes the nominal source impedance. The data sheet documents the ADC per-channel parasitic capacitances that can help in deciding which ADCs to use. Note that the acquisition window duration can be adjusted for each SOC by adjusting ACQPS or lowering the sampling frequency, or a combination of both. To evaluating the driving circuit, simulate it in TINA-TI to ensure correct performance and settling.

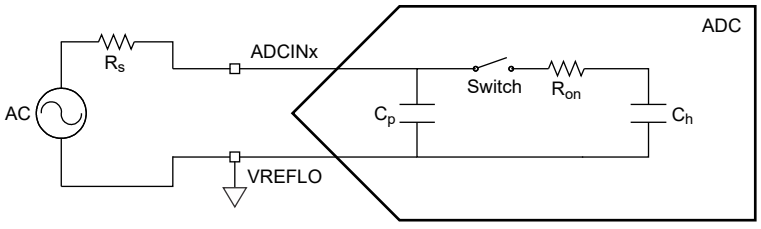

Figure 3-8. ADC Input Model

For a deeper dive into this topic, see the *ADC Input Circuit Evaluation for C2000 MCUs*. Additionally, to improve the ADC performance and reduce memory cross-talk, see the *Methods for Mitigating ADC Memory Cross-Talk*.

3.3.5 Driving Options

For the most optimal performance, ADCs should be driven with a high-speed op-amp buffer stage. This design has the capability for high-speed sampling, short S+H times, and high impedance sources. Driving the ADCs without an op-amp is possible in some instances, but this usually results in reduced control latency due to the very long S+H times.

Another possible ADC driving implementation is charge-sharing with a very large capacitor. This method works best in systems where both the sampling and signal bandwidth requirements are slow because it results in a sample rate limitation based on the source impedance. Charge sharing can be combined with a very low-cost op-amp to support faster sampling and higher input impedance. For more information, see the *Charge-Sharing Driving Circuits for C2000 ADCs*.

3.3.6 Low-Pass/Anti-Aliasing Filters

Selecting the RC circuit driving the ADC to provide low-pass filtering should not be a primary design consideration, although it can be done as a secondary constraint once satisfactory settling has been achieved. Furthermore, a very common error is selecting RC as an anti-aliasing filter for the ADC is, in most scenarios, a bad practice. It can lead to poor settling performance for high-speed sampling. If a system requires an anti-aliasing filter, it should ideally be built in a separate op-amp stage prior to the ADC drive stage for high-speed sampling. It can also be possible to implement anti-aliasing in the ADC drive stage when using the charge-sharing input model and when sampling is low-speed.

3.4 Power Supply

This C2000 device family has multiple power supply pins, though not all are available on every device. They include:

- Core Power Pins (VDD)
- Analog Power Pins (VDDA)
- Digital I/O Power Pins (VDDIO)
- Internal DC-DC Regulator Supply Pin (VDDIO_SW) (exclusive to F28004x)

For proper device function, all available power pins must be correctly connected to the proper supply voltage. These power supplies include 3.3 V and 1.2 V. The core power pins (VDD) require 1.2 V, which can be supplied in various ways. For F28003x/4x, the 1.2 V can be generated by the on-chip LDO or supplied externally. For the F28002x device, the 1.2 V can only be provided by the on-chip LDO. The analog (VDDA), digital I/O (VDDIO), and internal DC-DC regulator pins (VDDIO_SW) require external 3.3 V.

3.4.1 Power Requirements

An important aspect in ensuring a robust and noise-resistant power supply to the device is including decoupling/bypass capacitors to ground for every power pin. These help to limit the spread of noise into other areas of the system, particularly to low-level analog signals. Decoupling capacitors minimize voltage drops/spikes on the power supply by acting as a filter and temporary energy storage, leading to a more stable power supply solution for the device.

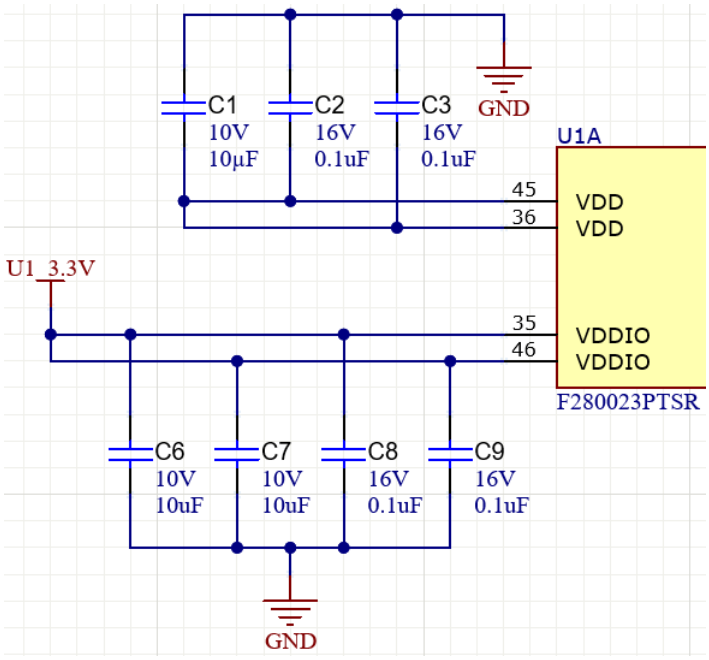

Figure 3-9. Decoupling Capacitors on VDD Pins

When using an external voltage regulator (on supported devices) to power VDD, all VDD pins should be routed together to the same 1.2 V power rail. Decoupling capacitors are required on these pins to ensure stable voltage supplies. The value of this decoupling capacitor is device-dependent, so see the device-specific data sheet for the required value of C_{VDD}. The VDDA and VDDIO power pins, likewise, also require decoupling capacitors to maintain a stable voltage supply. On all devices, all of the analog power pins (VDDA) should include a minimum 2.2 µF decoupling capacitor connected to analog ground (VSSA). The digital I/O power supply (VDDIO) requires a minimum 0.1 µF decoupling capacitor near each power pins, as shown in the figure above. For some devices, it is also recommended to place an additional bulk capacitor C_{VDDIO} shared across all the pins. This bulk capacitance value is dependent on the regulator being used, so see the device-specific data sheet.

Of special note is the F28004x device, which contains an internal DC-DC regulator supply pin (VDDIO_SW). This pin should have a bulk input capacitance of 20 µF. The recommended configuration for this is two 10 µF capacitors in parallel. Additionally, this pin should be tied to the VDDIO pin and both pins must be supplied from the same 3.3 V source. If desired, a ferrite bead may be used for isolation.

3.4.2 Power Sequencing

The F2800x devices offer only a few requirements to ensure proper power sequencing. Prior to powering the device, ensure that no voltage larger than 0.3 V above VDDIO is applied to any digital pins; likewise, ensure that no voltage larger than 0.3 V above VDDA is applied to any of the analog pins. For these respective pins, also ensure that no voltage 0.3 V below VSS and VSSA should be applied. All of the 3.3 V power pins—VDDIO, VDDIO_SW (on F28004x), and VDDA—should be powered up together and kept within 0.3 V of each other during functional operation.

The ADC inputs can be damaged when the above voltage requirements are not maintained. In instances where there is the potential to drive a higher voltage than VDDA on the ADC pins, care should be taken to isolate the signals. This can be done by buffering the signal with an op-amp that is powered by VDDA or to use an enable controlled by the C28x core. An analog mux or switch can be used in place of an op-amp buffer. An alternative to these designs would be to design current limiting on the pins, keeping in mind the maximum clamping current outlined in the device-specific data sheet.

When using the internal VREG, the VDD sequencing requirements are handled by the device. For devices with VREGENZ, internal VREG mode corresponds to when VREGENZ is tied to VSS. However, when supplying VDD externally (VREGENZ is tied to VDDIO) on devices without the Power Management Module (PMM) (ex. F28004x), be sure that VDD is powered up together with the 3.3 V supplies. VDDIO should thus not be powered on when VDD is off. During the ramp, VDD should be kept no more than 0.3 V above VDDIO.

On those devices with PMM (ex. F28003x) , VDD can be powered on after VDDIO, meaning that VDD and VDDIO do not have to power at the same time. For more information on the power sequencing requirements, see the *Power Sequencing* section in the device-specific data sheet.

3.4.3 VDD Voltage Regulator

Voltage regulation is an important aspect in maintaining a reliable power supply system for the device. All F2800x devices feature an internal voltage regulator (VREG). On devices which do not include a VREGENZ pin (F280013x, F28002x, some packages of F28003x and F28004x), the internal VREG is always enabled, so VDD cannot be supplied externally on these devices. When using the internal VREG, the two recommended capacitor configurations for the VDD rails are:

- Place a small decoupling capacitor to VSS on each pin as close to the device as possible. In addition, a bulk capacitance must be placed on the VDD node to VSS. The recommended components values depend on the device used. On

  F280013x, F28002x, and F28003x, the recommended components are either one 10 µF capacitor or two parallel 4.7 µF capacitors. On F28004x, the bypass capacitor configuration should be one 20 µF capacitor or two parallel 10 µF capacitors.
- Distribute the total capacitance to VSS evenly across all VDD pins (total capacitance divided by number of available VDD pins).

3.4.3.1 Internal vs. External Regulator

On devices with VREGENZ, choosing between the internal and external voltage regulator can offer many challenges. Making use of the internal voltage regulator is the most cost-effective solution and should be used in systems where the cost of the design is of great importance. Additionally, in designs with limited board real estate, the internal voltage regulator remains a good solution.

An external supply should be used if power efficiency is deemed most critical. In power designs which utilize a buck converter or other DC/DC converter, increased noise may be present on the ADCs and HRCAPs.

On devices that have it, tie the internal voltage regulator enable pin (VREGENZ) to VSS (low) to make use of the device's internal regulator. Otherwise, if one chooses to use an external voltage regulator, tie VREGENZ directly to VDDIO (high).

3.4.3.2 Internal LDO vs. Internal DC-DC Regulator

F28004x contains both an internal 1.2 V LDO voltage regulator (VREG) and an internal 1.2 V switching regulator (DC-DC). When implementing this device into a system, deciding between the internal LDO and the internal DC-DC solutions for the 1.2 V power rail is an important design decision when an external supply is not desired. The DC-DC regulator is significantly more efficient than the LDO, with the DC-DC regulator having 80% efficiency compared to the LDO regulator's 30% efficiency. However, the DC-DC solution comes with a few trade-offs. Depending on the board layout, there is the potential for analog performance degradation, mostly impacting the ADC. Additionally, the DC-DC requires an external inductor and capacitors to function, leading to increased component cost. Finally, GPIO22 and will be occupied by VFBSW and GPIO23 by VSW, leading to reduced I/Os on the board. Overall, the DC-DC voltage regulator is useful for systems which require efficient voltage regulation and reduced noise (since its switching is external to the MCU) and where the additional component cost is not an issue.

Figure 3-10 (also found in the *TMS320F28004x Real-Time Microcontrollers Data Sheet*) showcases the recommended design and required additional components when using the DC-DC regulator. Of special note is that an external connection should be made from the output of the internal DC-DC regulator to the VDD rail.

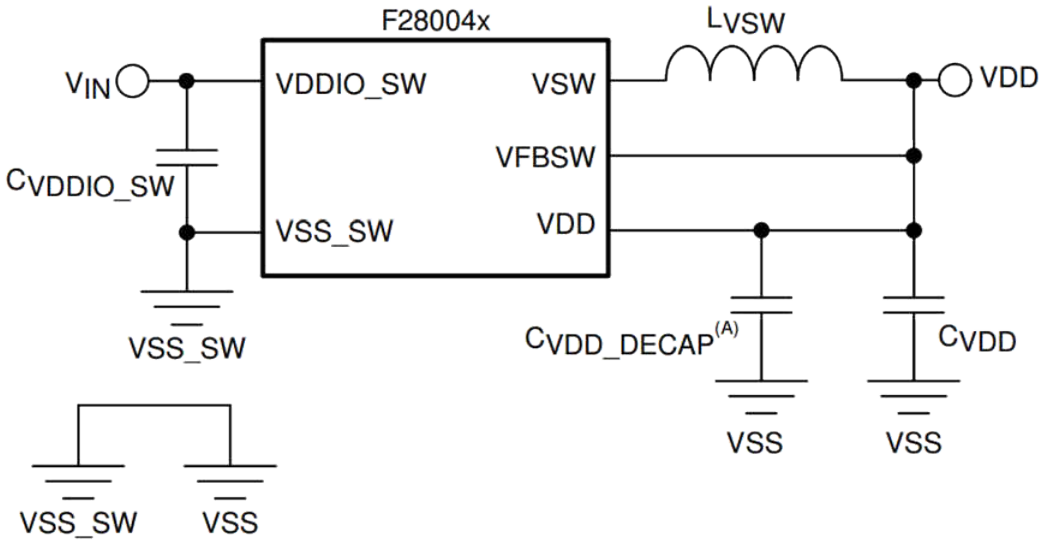

Figure 3-10. DC-DC Regulator Circuit Schematic

3.4.4 Power Consumption

Because the power consumption of C2000 chips can vary drastically depending on the device and specific use case, it is essential to consult the device-specific data sheet for extensive information on estimated power consumptions. An important note is that if the application requires in-circuit flash programming, additional current will be drawn during erase/write cycles. The tables within the data sheets give typical and worst-case maximum values. Power consumption can thus be further reduced with aspects such as unused peripherals, clock frequency, and temperature conditions. A final note to consider is that power consumption arising from I/O toggling and loading needs to be factored on top of these initial power consumption figures.

3.4.5 Power Calculations

Calculating the required power supply sizing requires taking into consideration the loads that plan to be present on the power supply, the noise tolerated by the system, as well as overall current requirements.

Firstly, calculate the current requirement for each voltage rail. Be sure to add the peak current values for each chip/module, which is typically each power supply pin. Additionally, plan to also account for all other passive and active loads, which include components such as LEDs and other loads.

For added precaution and to ensure a safe design, multiply these currents by a value between 1.3 to 2 to arrive at the recommend current specifications of the voltage regulator. This avoids current-starving any blocks connected to the power supply system. Select between the choice of linear regulators and DC-DC converters. This decision primarily depends on the amount of power supply noise tolerated by the system as a whole. In systems that require very low noise, linear regulators/LDOs are recommended. DC-DC converters, on the other hand, offer better power efficiency.

The following scenarios provide example guidance on calculating the recommend power supply specifications:

- An application makes use of F28002x and all of its available peripherals. The device's flash will not be upgraded in the field, ten of its GPIO pins will drive 1.5 mA static loads, and two additional GPIOs are toggling waveforms at 200 kHz with a 10 pF load.

$$P_{est} = \{Operating\ Mode\} + \left(n_{GPIO,static} \times I_{load}\right) + n_{GPIO,active} \times \left(n_{transitions/period} \times f \times C \times V^2\right) \quad (1)$$

$$P_{est} = (0.072A + 0.005A) + (10 \times 0.0015A) + 2 \times \left(2 \times 200k \times 10p \times 3.3^2\right) \quad (2)$$

$$P_{est} = 92mA \quad (3)$$

In this scenario, though flash-programming will not occur in the field, initial programming will occur. Thus:

$$92mA < (106mA + 2.5mA) = 108.5mA \quad (4)$$

Multiplying by a margin value of 1.5, the final supply current requirement is determined:

$$108.5mA \times 1.5 = 162mA \ @ \ 3.3V \ (535mW) \quad (5)$$

- An application uses the F28002x and the following peripherals: two ADCs, one CAN, and four HRPWM modules. It will need to be upgraded in the field.

$$P_{est} = \{Flash\ Program\ Mode\} + (2 \times I_{ADC}) + (1 \times I_{CAN}) + (4 \times I_{HRPWM}) \quad (6)$$

$$P_{est} = (0.106A + 0.0025A) + 2 \times 0.67A + 1 \times 1.18A + 4 \times 0.87A \quad (7)$$

$$P_{est} = 114mA \quad (8)$$

Multiplying by a margin value of 1.5, we arrive at our final supply current requirement:

$$114mA \times 1.5 = 171mA \ @ \ 3.3V \ (564mW) \quad (9)$$

3.5 XRSn and System Reset

Each of the F2800x devices contain a device reset (XRSn) pin that resets the device when driven low. This pin is also driven low upon power-on reset (POR), brownout reset (BOR), or watchdog reset. The internal POR circuit drives the XRSn and keeps all of the I/Os in a high-impedance state while the device is powering on. Once VDDIO crosses the POR threshold, control of the device is then given to the BOR. The BOR keeps holding the device in reset until VDDIO crosses the BOR threshold and arrives within the device's operational range. Once this occurs, the device is no longer in reset and is functional. The BOR circuit itself is responsible for monitoring the VDDIO and checking that the supply rails remain within operational range. At any point during the operation of the device, if the VDDIO voltage drops below the BOR threshold, XRSn is pulled low and the device remains in reset until the voltage returns to the operational range. During the watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 oscillator clock (OSCCLK) cycles.

Figure 3-11 showcases the device boot thresholds.

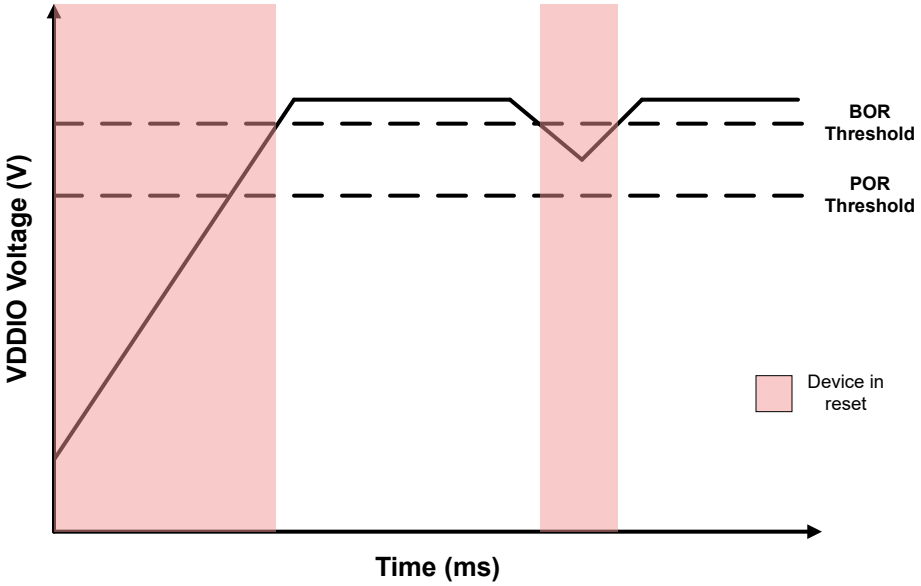

Figure 3-11. Device Boot Reset Thresholds

Apart from these internal reset circuits, a user may implement external circuitry that drives the XRSn pin and asserts a device reset. Note that this external circuitry should be done using an open-drain device. Examples of these outside circuits include external watchdogs, power management ICs, and voltage supervisors (for use in ASIL applications).

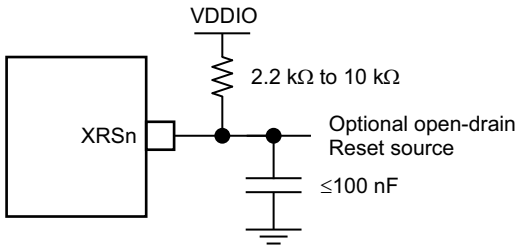

Figure 3-12. External Reset Circuit

When designing the XRSn schematic, a strong pull-up resistor is required between the XRSn pin and VDDIO. This resistor should be between 2.2 kΩ and 10 kΩ in value. Furthermore, to improve noise filtering, a small capacitor is recommended between XRSn and VSS. This capacitor should be 100nF or less, as a larger capacitor will inhibit the ability of the watchdog reset to properly drive the XRSn pin. Due to significance of this pin, ESD protection diodes may also be added.

Note

The reset pulse-width should be in excess of 1.5 milliseconds to overcome oscillator start-up and other delays.

3.6 Clocking

Proper clock generation is critical for proper system operation, especially in real-time control systems. The F2800x devices offers flexible clock generation options which allow users to tune the device for their specific system requirements. All devices feature two internal 0-pin 10 MHz oscillators, support for on-chip crystal oscillator and external clock input, and an on-chip phase-locked loop (PLL). While these internal sources are fairly performant, users may elect to make use of an external clock source for more accurate clocking requirements. These C2000 devices support three types of external clocking methods: a single-ended 3.3 V external oscillator, an external crystal, and an external resonator.

3.6.1 Internal vs. External Oscillator

An important decision in the design process is choosing whether to make use of the on-board clocking options or incorporating an external oscillator into the system. The following design considerations should provide ample assistance in the decision-making process, although the final choice is dependent on cost and system-clocking requirements.

The two internal 0-pin on-chip oscillators (INTOSC1 and INTOSC2) run at 10 MHz and can be used to provide clock for the main PLL and CPU-Timer 2. In addition, INTOSC1 can also provide clock for the watchdog block. These oscillators are both enabled by default at power up, where INTOSC2 is set as the source for the system reference clock and INTOSC1 Is used as the backup clock source. This clocking option is useful for designs which prioritize cost-savings and shorter design schedules. The trade-off with this decision is lower accuracy compared to an external clock source. Depending on the environmental conditions, the clock could have frequency stability of approximately 1.5% to 3% outside of the typical 10 MHz. The stability is different for every device, so see the device-specific data sheet for the specific values and test conditions. Additionally, note that for F28004x, GPIO18 and its mux options are only available when the system is clocked by INTOSC and X1 has an external pull-down resistor. For the other devices, GPIO18 and GPIO19 can be used as additional digital signals when INTOSC is used.

Another clocking option is using the internal oscillator in conjunction with an external crystal. This approach should be used if clocking precision better than 1% is required. An important consideration when choosing this approach is that making any other additional connections to the crystal circuit is not recommended. Additionally, the crystal oscillator needs to be designed very carefully to ensure proper function. These crystals have multiple parameters, so it is recommended to consult with crystal vendors to incorporate a crystal that works well with the C2000 device. Special attention must be placed so that the crystal chosen accurately matches the load capacitance for the system. A crystal with a load capacitance C_{load} outside of the ideal range will inhibit the oscillator driving the crystal from starting up and running reliably. The effective load capacitance appears as the series combination of C1 and C2, which are the capacitors connected to X1 and X2, respectively. To calculate the value for C_{load}, take into consideration C1 and C2 as well as stray capacitance for routing on the PCB.

$$C_{\text{load, XTAL}} = \frac{C1 \times C2}{C1 + C2} + C_{stray} \tag{10}$$

Assume C1 and C2 are equivalent. This is not a requirement, but aids in simplifying the calculation to the following equation:

$$C_{load, \text{XTAL}} = \frac{C}{2} + C_{stray} \tag{11}$$

For example, suppose a system has known load capacitance of 12 pF and stray capacitance of 2 pF. Appropriate calculations give a suggested capacitor value of 20 pF.

$$12pF = \frac{C}{2} + 2pF \tag{12}$$

$$C = 20pF \tag{13}$$

For current F2800x devices, the recommended crystal load capacitance should be around 12 pF to 24 pF. In future devices, this value may be different. For additional requirements, see the device-specific data sheet. As shown in Figure 3-13, the crystal should be connected across X1 and X2 with its load capacitors connected to VSS.

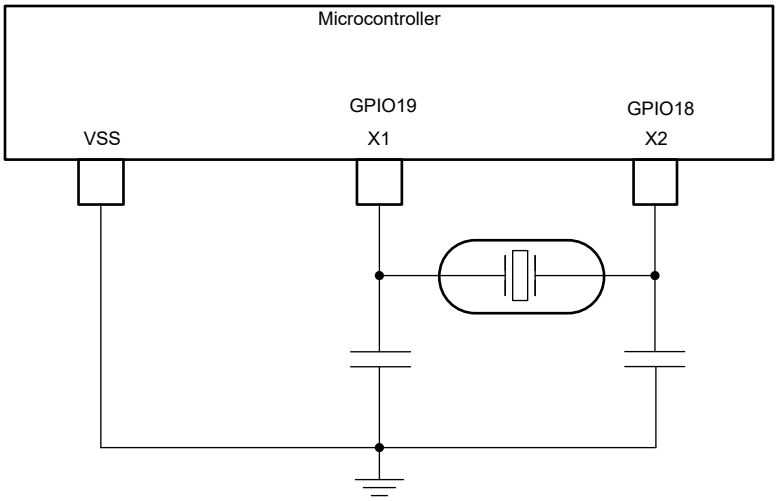

Figure 3-13. External Crystal Circuit

A resonator may also be used in a similar fashion as the crystal and offers similar tradeoffs and considerations. When implementing the resonator, it should be connected across X1 and X2 with the ground connected to VSS, as shown in Figure 3-14.

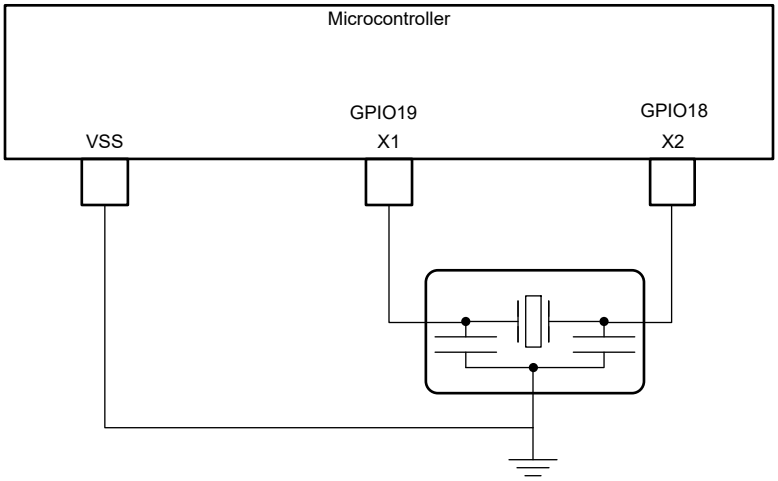

Figure 3-14. External Resonator Circuit

A third and final clocking source option is using an external oscillator completely. This is a simpler approach than using an external crystal and can provide the most accuracy for real-time systems. Furthermore, other devices within the system can share the clock signal being output from the external oscillator. The clock signal should be connected to the MCU as shown in Figure 3-15, with the output of the external oscillator connected to X1 and the XTALCR.SE bit set to 1.

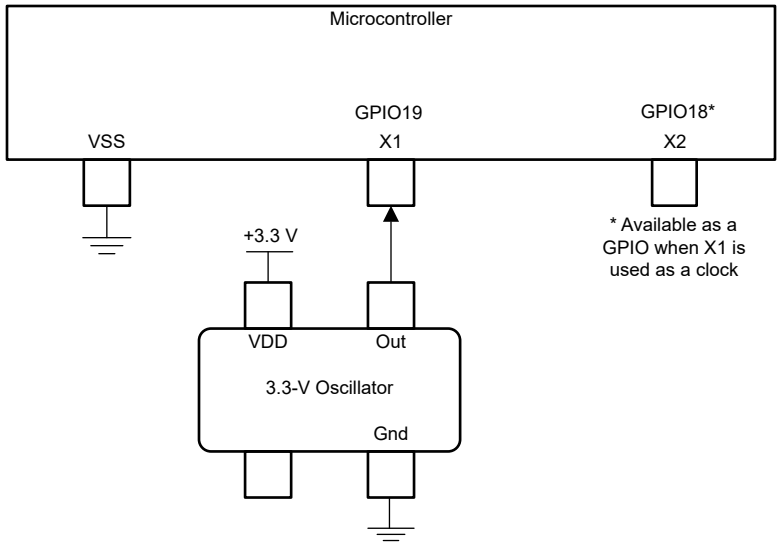

Figure 3-15. External Oscillator Circuit

3.7 Debugging and Emulation

Incorporating a device to assist in debugging the microcontroller system is an important consideration that greatly helps in the prototyping and development phase of the design process.

3.7.1 JTAG/cJTAG

The F2800x devices feature a JTAG port with four dedicated pins: TMS, TCK, TDI, and TDO. These correspond to test-mode select, test clock, test data input, and test data output. An external 2.2 kΩ pull-up resistor on the board should tie the TMS pin to VDDIO to keep JTAG in reset during normal operation. There is also a cJTAG (IEEE Standard 1149.7) port, which is a compact 2-pin JTAG interface that only features TMS and TCK. When using cJTAG, other device functionality can be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins to allow for full emulation and debugging capabilities.

When choosing between JTAG and cJTAG, consider the system requirements in terms of interface speed, debug functionality, and pin constraints. JTAG should be used if interface speed is of great importance, as JTAG is around 2-3 times faster than cJTAG. Additionally, using JTAG also enables the ability to daisy-chain multiple devices on a single JTAG header. cJTAG should be used if pin usage is constrained, as using cJTAG frees up 2 GPIO pins on the device. Apart from the performance drawback, the TMS pin is bidirectional when cJTAG is used, which could impact isolation strategies. Overall, if pins usage is not constrained, normal JTAG is recommended because of its performance advantages.

Although JTAG debug probes are included in all C2000 evaluation modules, TI does not recommend including the JTAG debug probe directly on the board. All EVMs include these headers to allow for streamlined debugging and emulation as well as the ability to use the EVM as a standalone debug probe. In actual C2000 applications, an on-board debug probe is not necessary and adds additional costs. Instead, if JTAG functionality is desired, it is recommended to include a JTAG header for connecting to an external probe. In instances where the MCU target and the JTAG header are farther than 6 inches (15.24 cm) apart or other devices are present on the JTAG chain, then each JTAG signal should be buffered.

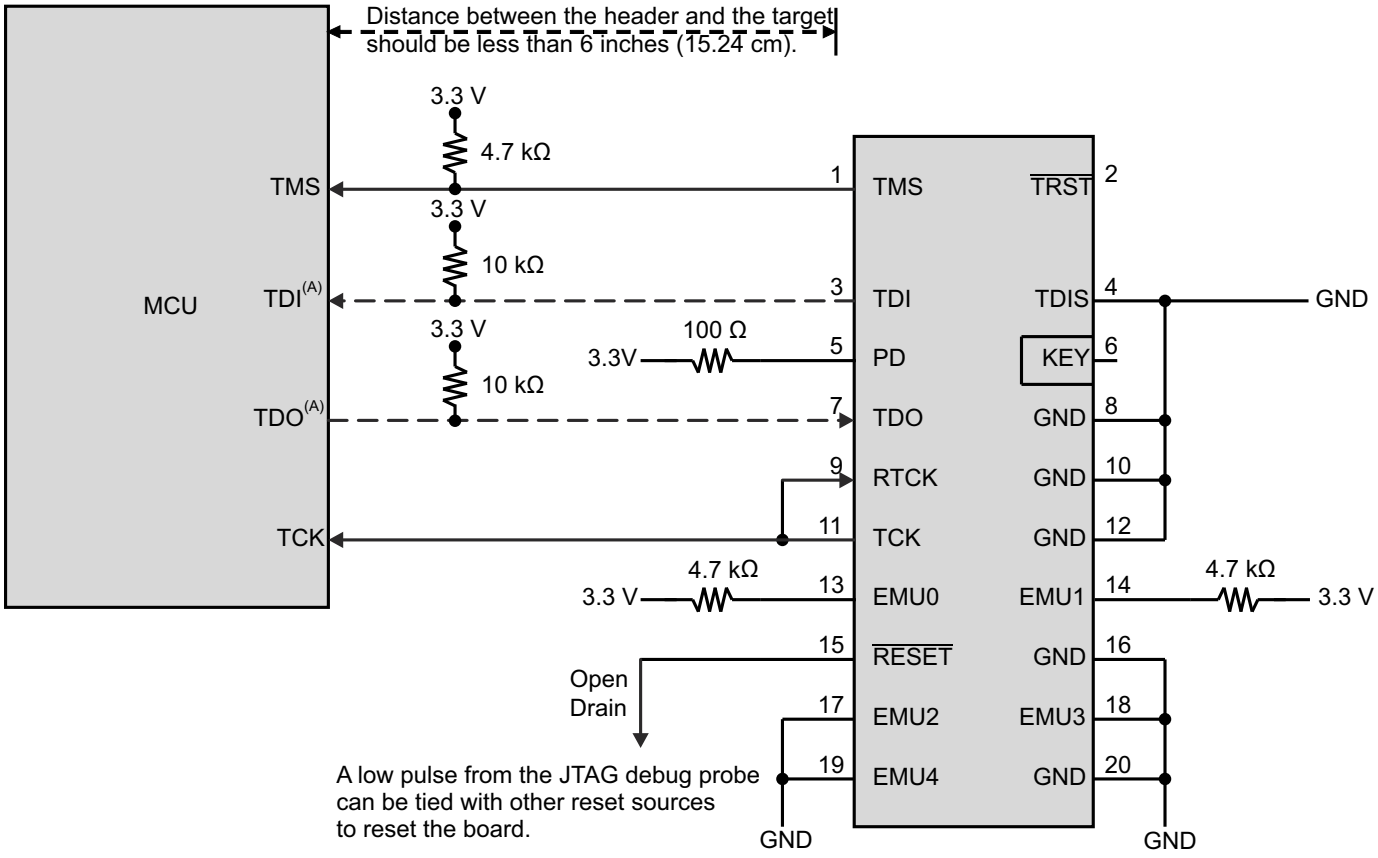

Figure 3-16. Typical JTAG Probe Connections

Note

TDI and TDO are the default mux selection for their respective pins. The internal pullups are disabled by default. When using JTAG, the internal pullups should be enabled or external pullups added on the board to avoid floating pins. If using cJTAG, these pins can be used as GPIO.

For even more information about using JTAG with C2000 devices, see the *C2000 MCU JTAG Connectivity Debug*.

3.7.2 Debug Probe

There are many debug probe options that can be used with C2000. The following are just a few recommended probes, though other debug probes may be used if they are supported under the latest Code Composer Studio (CCS) version.

Table 3-2. Recommended Debug Probes

Part Number	Description
XDS110	Preferred low-cost debug-probe. Performance is roughly equivalent to the XDS100V2. Supported only by CCS v7 and greater.
XDS200	Preferred mid-class external debug probe for C2000 users. Supports new 2-pin cJTAG mode.
XDS560	Preferred advanced debug-probe with increased performance over XDS200.
Isolation adapters	Provides electrical isolation to any debug probe.

3.8 Unused Pins

For applications and systems that do not require all functions of the device, there are explicit acceptable practices that should be followed on some unused pins. These practices are device and pin-specific, but can include placing pull-resistors on them, tying them to another pin, or leaving them as no-connects. For more details and all the pins that this pertains to, see the *Connections for Unused Pins* section in the device-specific data sheet.

4 PCB Layout Design

After creating and validating that the system schematic is properly designed and meets all engineering specifications, the next step is to create the PCB layout in your preferred PCB design software. Placement of the components is critical to good design and good device performance.

4.1 Layout Design Overview

It is not simply enough to be able to route all the connections as in the schematic; moreover, good layout practices must be employed to ensure proper functionality and reliability of the board. All aspects of the board, including the physical dimensions, board constraints, and key components, should be considered thoroughly.

4.1.1 Recommend Layout Practices

C2000 systems typically include the following: low-level analog, high-speed digital, and high-power (switching) circuits. These three different types of signals should be sectioned off and separated on the PCB. High current paths and high frequency signals are especially disruptive to any analog signals present on the board.

4.1.2 Board Dimensions

The dimensions of the board are highly-dependent on the system being built and the application that C2000 is being implemented into. The PCB board can range from small boards which consist of a few devices to large boards with a comprehensive number of components. If possible, allot a large enough PCB to make the layout design process as easy as possible and to assist in routing traces and separating different kinds of signals.

4.1.3 Layer Stack-Up

Choosing the number of board layers and the layer stack-up is dependent on the number of connections that need to be made on the PCB along with the cost of producing the PCB. A 4-layer board or more is often the best choice for C2000 devices. This enables the designer to include a clean ground plane and split power plane. In terms of configuration, two diagrams showcasing common 4-layer and 6-layer board stack-ups are shown. The 4-layer board stack-up consists of a signal/component layer, ground plane, split power plane (3.3 V, 1.2 V, and so forth), and signal/component layer. For the 6-layer board, the stack-up is as follows: signal/component layer, ground plane, split power plane (3.3 V, 1.2 V, and so forth), signal layer, another ground plane, and signal/component layer.

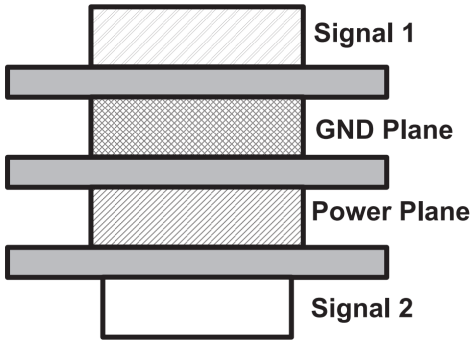

Figure 4-1. Layer Stack-Up for 4-Layer Board

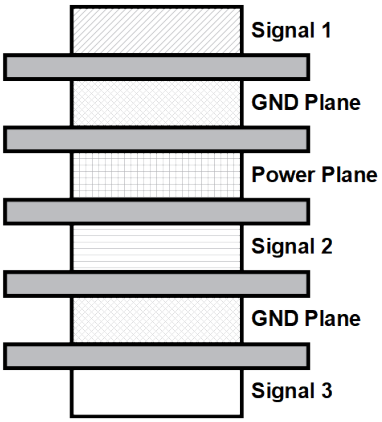

Figure 4-2. Layer Stack-Up for 6-Layer Board

4.2 Recommended Board Layout

To ensure that the signals routed on the board do not experience any cross-talk or degraded performance, a good practice is to partition the board similar to that shown in Figure 4-3. As mentioned earlier, the three types of signals (digital, analog, and high-current) should all be sectioned off from each other on the PCB.

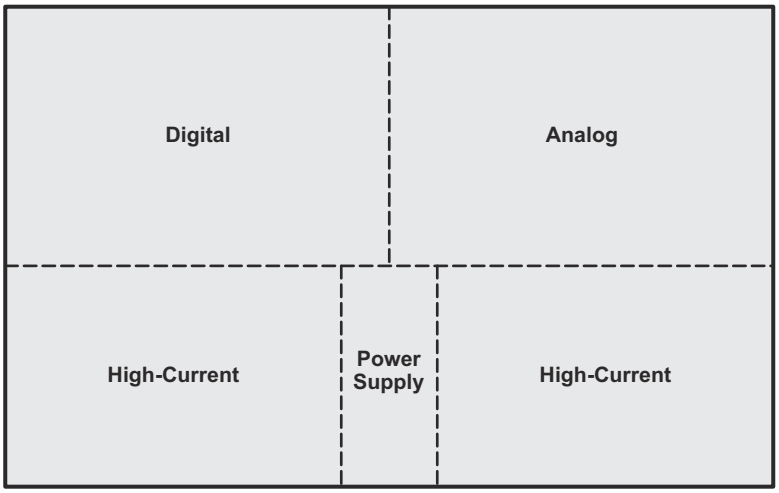

Figure 4-3. Ideal C2000 Board Partitioning

4.3 Placing Components

Once the position of the C2000 chip has been decided on the board, the next component that should be placed is the crystal/oscillator. This should be placed as close to the device as possible to ensure the most effective clocking solution. Specifically, traces to X1/X2 should remain as short as possible. Depending on the additional components required by the specific crystal being used, there are different ways in which a crystal/resonator can be routed on a board. Figure 4-4 is one example given a 2-layer board and a crystal that requires an additional series resistor R_S. When routing the clock traces from one device to another, try to use the 3W spacing rule. The distance from the center of the clock trace to the center of any adjacent signal trace should be at least three times the width of the clock trace. Many clocks, including slow frequency clocks, can have fast rise and fall times. Using the 3W rule cuts down on crosstalk between traces. In general, leave space between each of the traces running parallel between the devices. Avoid using right angles when routing traces to minimize the routing distance and impedance discontinuities. For further protection from crosstalk, run guard traces beside the clock signals (GND pin to GND pin), if possible. This lessens clock signal coupling.

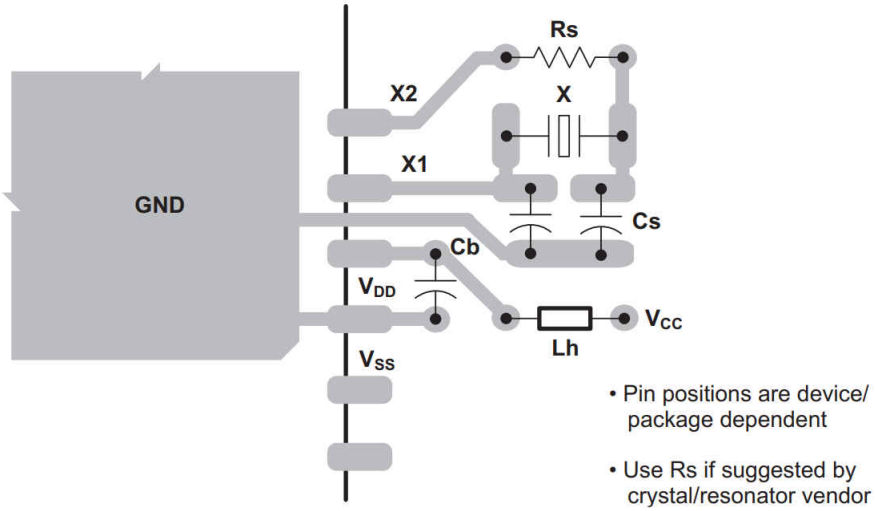

Figure 4-4. Recommended Oscillator Layout

The next most important components to place are the decoupling/bypass capacitors. These capacitors should be placed as close to their respective pins as possible and will further reduce noise and help ensure that the device's power supplies are stable. Decoupling capacitors placed more than an inch away from the pins offer poor performance. Bulk capacitors, on the other hand, can be placed relatively further away from the chip without greatly impacting their performance. Figure 4-5 showcases good decoupling capacitor placement.

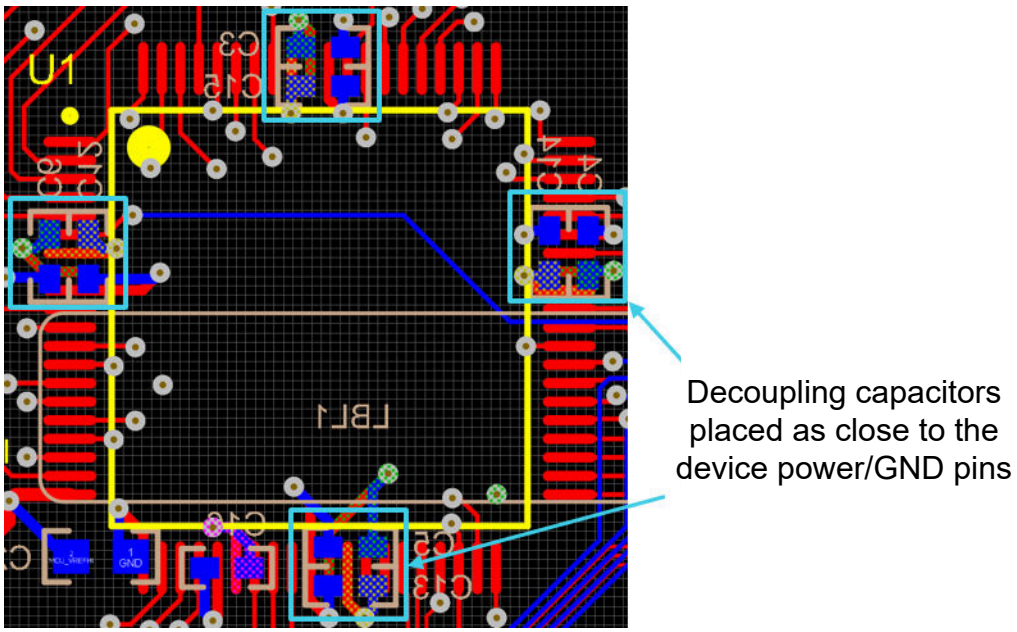

Figure 4-5. Decoupling Capacitors on Board Layout

Other components that should follow are the JTAG header/circuitry and the XRSn circuitry.

For systems which make use of the internal 1.2 V DC-DC regulator on the TMS320F28004x device, the following outline key guidelines to ensure proper design of the DC-DC circuitry.

- TI recommends star-connecting VDDIO_SW and VDDIO to the same 3.3-V supply.
- All external components should be placed as close to the pins as possible.
- The loop formed by the VDDIO_SW, input capacitor (C_{VDDIO_SW}), and VSS_SW must be as short as possible.
- The feedback trace must be as short as possible and kept away from any noise source such as the switching output (VSW).

- It is necessary to have a separate island or surgical cut in the ground plane for the input cap (C_{VDDIO_SW}) and VSS_SW.
- A VDD plane is recommended for connecting the VDD node to the L_{VSW}-C_{VDD} point to minimize parasitic resistance and inductance.

4.3.1 Power Electronic Considerations

Power electronics are very noisy components that can severely hinder the performance of the device. The placement of these components and their signals with respect to other types of signals is an important consideration. Any high-current paths should be designed such that its loop area is small. Any high di/dt currents should not cross other di/dt paths, any sensitive analog signals or control circuitry, or any test points. Any current sense op amps can be placed in two manners. They can be placed next to shunt, with any low-pass filtering remaining close to the C2000 chip and being grounded to analog ground (VSSA). Alternatively, they can be next to the C2000 chip and routed differentially to the op amp using Kelvin sensing.

Another note is that heatsinks can have high dV/dt and should be routed externally to ground. Routing the heatsink to the board ground may make the heatsink live. Any gate drivers should be near the FETs.

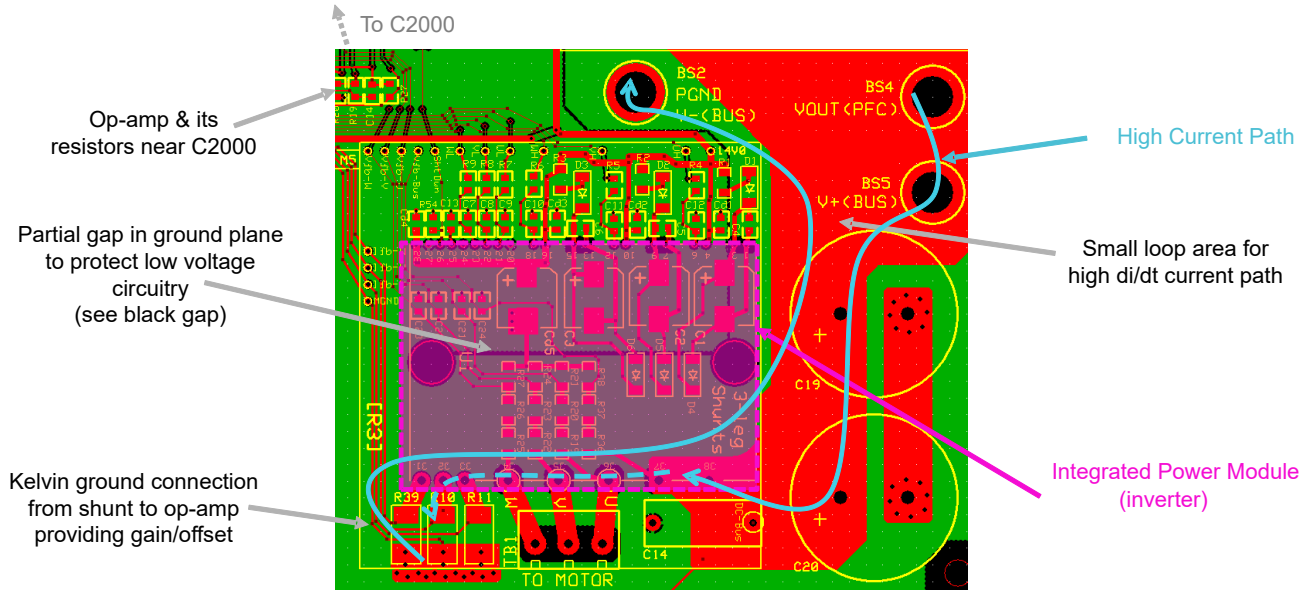

Figure 4-6. Power Electronics on Board Layout

4.4 Ground Plane

Copper planes on a PCB are excellent high-frequency capacitors and can be utilized for high-frequency bypassing along with the recommend capacitors. Another benefit of solid planes are that they can act as a good heat sink to mitigate excess thermal levels.

If the board has ample layers, a good practice is to place a ground place on the PCB. This ground plane not only assists in routing the ground signals on a board, but also helps in combating ground noise. Each signal on the board has a return current (via GND), and this ensures that the return path is through the path of least impedance. For boards with multiple ground planes on different layers, it is helpful to employ via stitching to connect these ground planes and further minimize impedance. For more information about return paths, see the *Return Current and Loop Areas* section of the High-Speed Layout Guidelines.

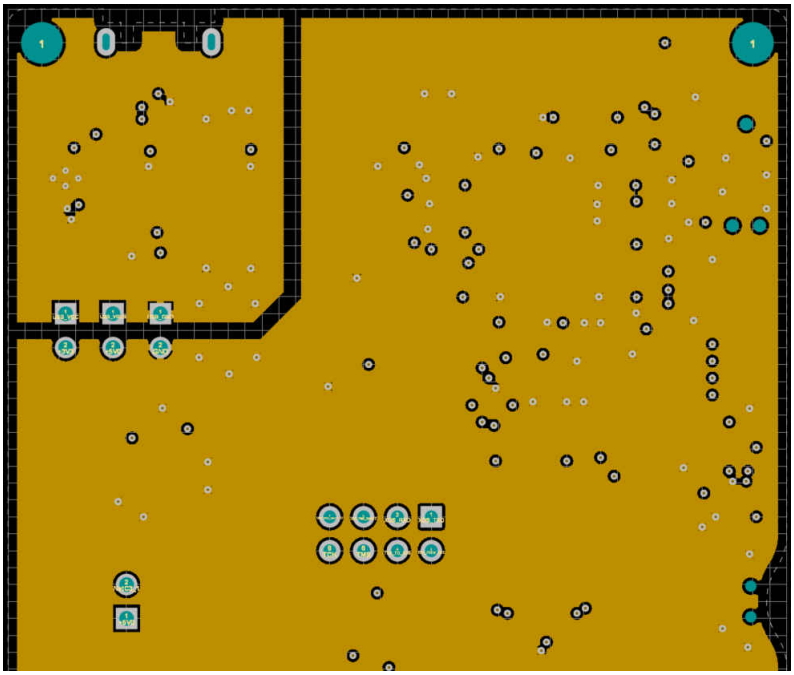

Figure 4-7. Ground Plane on LaunchPad

The key to an effective ground plane is making sure that the plane remains intact and has good connections throughout the entire layer of the board. Onboard connections, such as vias and traces, can cut up the ground layer and reduce its effectiveness. Vias create a hole through multiple layers of the board and traces can sever the connection between different parts of the ground plane. In the left figure below, notice that the RGND vias only have a single connection to the ground plane and that the surrounding ground pore connections are very thin. Furthermore, in the Figure 4-8, notice that the top left of the pore is connected to the bottom left of the pour only through a thin sliver of copper. Both of these figures showcase undesirable ground planes. It would be helpful to rearrange the vias and traces to ensure that there are no thin ground plane connections or a severely cut-up ground pour.

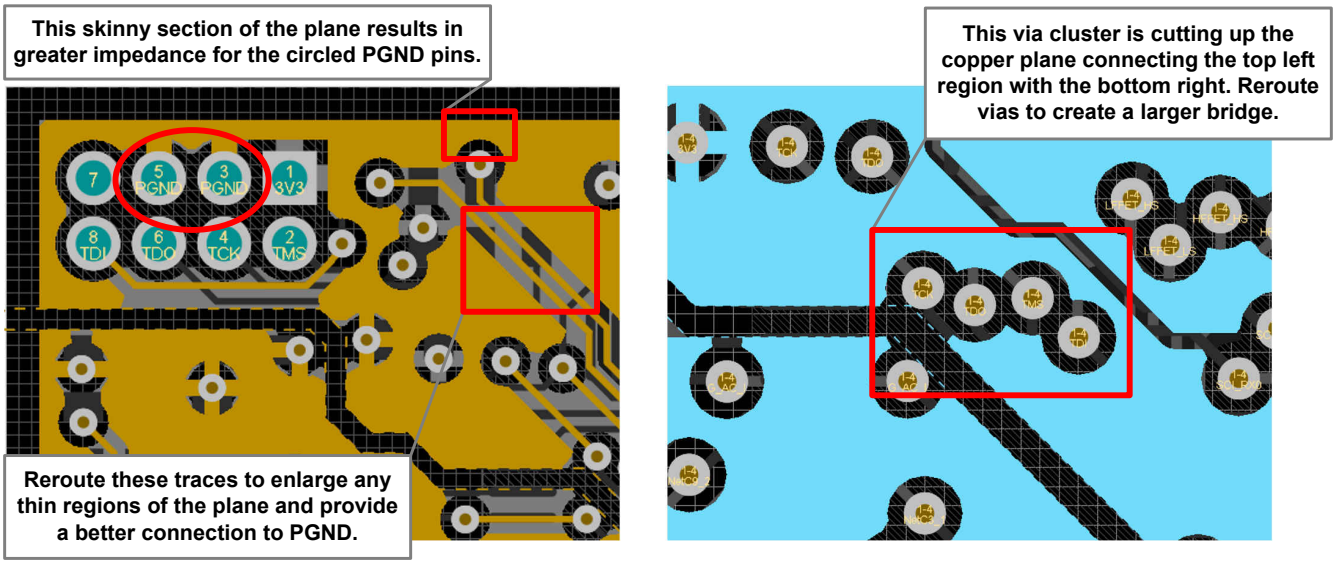

Figure 4-8. Examples of Cut-Up Ground Planes

When applying a ground plane to a layer, examine the plane to see if it has good connection throughout. Areas with missing planes or thin connections should be redesigned to maximize the ground plane area. Typically, this can be done by reducing the number of vias and by routing groups of traces closer to each other. In some cases, it may be helpful to modify the pinmux selection and schematic to improve routing. Sometimes these benefits may not be apparent until the layout routing process begins, but optimizing the pinmux can result in shorter trace lengths and reduced via usage, and thus a better ground plane.

4.5 Analog and Digital Separation

As another reiteration, splitting the analog and digital ground (and their supply) is good practice. However, if this is not done well, it could lead to worse performance. The benefit of analog/digital separation is that it ensures that signals cannot cross the isolation boundary, except in cases where the signals crossing are static. The split signals should connect at only point, ideally being the source of the signal. This connection could be a ferrite bead, a simple resistor, or even a break in a plane. Note that ferrite beads provide negligible capacitance and low DC resistance. When electing to use a ferrite bead, undergo proper simulation to ensure that the ferrite bead is properly filtering noise and not limiting current to the device. If proper analog and digital separation cannot be achieved, a designer should consider using just a single ground plane.

The C2000 device is designed to have an “analog corner” whereby all of the analog pins of the device are located. The source for many of these ADC inputs usually comes from the power electronics part of the design. This area is usually the noisiest part of the board and can impact analog performance severely. It is best to keep the analog ground area small and close to the C2000 chip to suppress noise from affecting the device’s ADCs. A reduction in the size of the analog ground plane, when done properly, translates to a reduction in noise pickup.

An example of analog/digital separation is shown in Figure 4-9. Note the clear isolation boundary in the ground plane that separates the analog ground and digital ground.

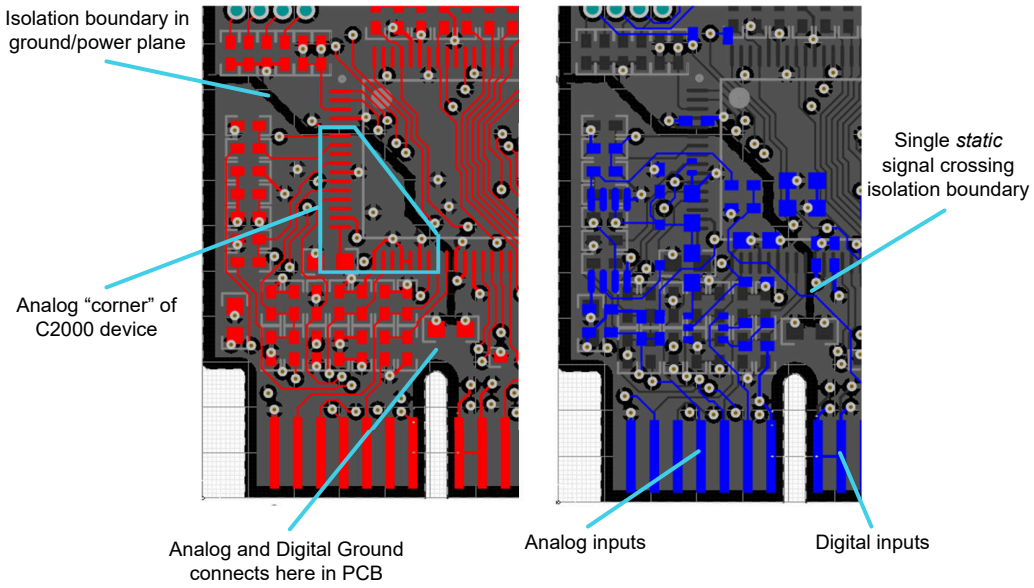

Figure 4-9. Analog/Digital Isolation

In this example, there is only a single ground plane for both digital and analog grounds (VSS/VSSA). The grounds are shorted at only one point: the bottom gray area of the isolation boundary near the source. Additionally, notice that there is only a single signal crossing the isolation boundary. The signal being highlighted is a static signal that will rarely, if ever, change states during the entire operation of the system. This means that it will not generate any significant noise and will not be a problem for the system.

4.6 Signal Routing With Traces and Vias

For proper signal routing, ensure that none of the traces bend at a 90° angle. While this is automatic in most PCB design software, confirming this property amongst all traces is good practice. Traces should be routed with a bend of at most 45°, or along a curve if possible. This reduces reflections and changes in characteristic impedance along the trace, leading to reduced radiation. This is because right angles cause increased capacitance in the region of the corner and thus impedance change, which moreover leads to reflections. Additionally, a good practice is to have the signals on adjacent layers cross perpendicular to each other (at a 90° angle). This can reduce crosstalk between the signals and ensure that disturbance between signals is minimized. Including ample spacing between traces can also reduce cross-talk, especially for signals with fast rise/fall times.

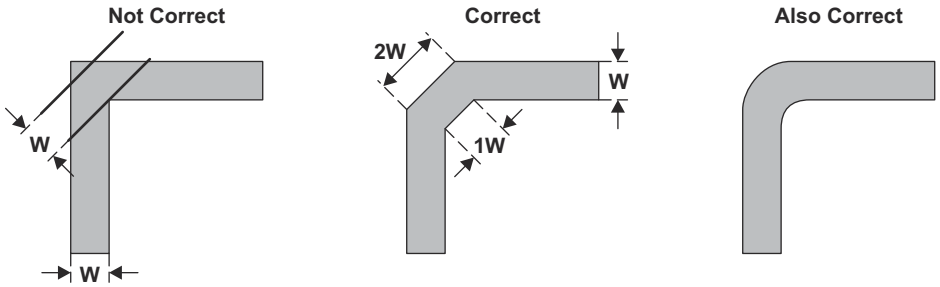

Figure 4-10. Proper Trace Signal Routing

Certain signals on the board require thicker trace widths. Most notably, any power routes and high-current paths should use wide traces. Wide traces help to maintain a low-inductance path on these routes. This can help with reducing the voltage drops and power loss on these paths as well as reducing unwanted thermal dissipation.

When routing traces on a multi-layer board, oftentimes it is necessary to route signals on different layers. Vias are used to cross signals between different layers, but they should be used sparingly and only when necessary. Apart from creating holes throughout the planes on the board, these vias can also have negative impacts on the EMI produced by the board, especially for high-switching signals. Improved signal routing may be achieved by making modifications to the pinmux selection and schematic of the system. Reassigning pins can help in optimizing the trace routing and lead to shorter trace lengths and a reduced need for vias.

When using vias, an important consideration is whether to tent the vias. This practice offers many benefits but adds additional cost to board production. Tenting vias with solder mask offers corrosion protection to the vias and can reduce via degradation. On high-density boards, tented vias ease in the placement and readibility of silkscreen, as silkscreen does not stick to plain, un-tented vias. Additionally, the tent can help prevent any accidental shorts. For example, if a connector is placed over an un-tented via, an electrical short can be made. The ability to tent a via depends on the size of the via. Small vias are easier to fill than larger vias, and the feasibility of tenting large vias is dependent on the board manufacturer.

4.7 Thermal Considerations

For each C2000 device, the thermal characteristics and temperature specification limits are heavily documented. Systems and end products that exceed any of the data sheet's recommended maximum power dissipation may require additional thermal dissipation incorporated into the design. The primary thermal consideration is the junction temperature (T_J). This specification should be carefully tested so that it remains in the absolute and recommended limits. Doing this will ensure reliable and function operation for the lifetime of the device. Another thermal consideration is the ambient temperature (T_A), though this varies depending on the end application environment and the product design.

To minimize T_J through the PCB board design, design the system such that the board-to-ambient thermal resistance (Θ_{BA}) is small. The GND and power pins are the primary method by which heat is dissipated out of the device. Thus, if the device has a thermal pad pin, be sure that it ties to a large copper area on the PCB. In most packages, the thermal pad will either be connected to GND inside the device or tied externally to GND. Likewise, ensure that any GND and power pads have a good connection to a solid plane and that any vias remain close to the C2000 device.

For more information on thermal metrics and definitions, see the Semiconductor and IC Package Thermal Metrics.

5 EOS, EMI/EMC, and ESD Considerations

With any electronics system, it is important to consider the possible effects of outside electrical factors and to take steps to limit and mitigate their impacts. Insufficient care may result in non-optimal performance, reduced reliability, and even damage to the components.

5.1 Electrical Overstress

The data sheet for each device provides in great detail the recommended and maximum conditions in which the device will function properly and reliably. The following points detail the most important considerations to be aware of when using the F2800x devices.

- The GPIO input voltages cannot be above VDDIO + 0.3 V nor below VSS – 0.3 V.
- Similarly, the ADC input voltages cannot be above VDDA + 0.3 V nor below VSSA – 0.3 V. Voltages outside of this range can result in improper ADC function and degraded performance.
- For all GPIO and ADC input pins, the input clamp current should be not be above 20 mA or below -20 mA. The continuous clamp current per pin is ±2 mA, but it is not recommended to sustain this condition continuously as this could cause the voltages of VDDIO and VDDA to internally rise and impact other electrical specifications.
- Any signals which may be powered prior to the C2000 device is powered should be current limited and protected such that the signals do not exceed the specifications listed in the data sheet.
- Use of 3.3 V powered operational amplifier (op amp), steering diodes, or series resistance, or any combination of the three, may be necessary to remove the risk of damage to the device.

5.2 Electromagnetic Interference and Electromagnetic Compatibility

Electromagnetic compatibility (EMC) describes the ability of electronic components to function properly amidst interferences and disturbances from other systems. The most pertinent to consider is electromagnetic interference (EMI), which is radio frequency energy that is emitted by the device and other nearby devices. This disturbance can propagate and impact the device through conduction and radiation.

Thus, when designing a system, it is important to ensure that the EMI emitted by the board from both radiation and conduction does not exceed the maximum allowed per regulated standards. Hardware designers should work to minimize radiated and conducted EMI to levels far below the limits for certification. Similarly, the board should be designed with adequate shielding to function properly even whilst being in contact with radiated and conducted electromagnetic energy from other systems around it.

Most components in the system, including the PCB, connectors, cables, and so forth, serve as a source of EMI. Especially when designing a board that makes use of high frequencies and fast-switching currents and voltages, all of the traces essentially act as antennas which radiate electromagnetic energy. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, and PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another, building up EMI. Switching power supplies radiate the energy which can fail the EMI test.

To reduce any unwanted EMI generated by the board and its components, follow these guidelines throughout the schematic and layout design process:

- Use multiple decoupling capacitors with different values and appropriate power supply decoupling techniques. Be aware that every capacitor has a self-resonant frequency.
- Provide adequate filter capacitors on the power supply source. These capacitors and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias; creating a quarter-inch via grid is ideal.

- The high frequency signals (lower address lines, clock signals, serial ports and so forth) are usually terminated by a CMOS input, which is a load of > 100 K parallel with typically 10 pF. Charging/discharging of such a load results in high current peak. A possible fix is to add a series termination resistor (about 50Ω) and fine tune the resistors for optimal signal integrity. As per the transmission line theory, if the total output resistance (internal + external) is less than the line impedance (typically 70Ω–120Ω), it has no negative influence on speed. In general, reduce the risetime of the signal if timing is not critical by adding a series termination resistor. Substantial benefits can be achieved with this approach at a low cost.
- Typically, PWM signals driving a 3-phase H-bridge switch on and off cause current spikes. Symmetrical PWM reduces EMI related to dU/dt and di/dt by approximately 66% compared to asymmetrical PWM. The space vector PWM is symmetrical with respect to the PWM period, too. However, since only two transistors are switched during one PWM period, the switching losses as well as the EMI radiation are reduced by 30% compared to the symmetric PWM.
- Keep the current loops as small as possible. Add as many required decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.
- Apply current return rules to connect the grounds together while isolating the ground plane for the analog portion. If the project does not use ADC and there are no analog circuits, do not isolate grounds.
- Avoid connecting the ground splits with a ferrite bead. At high frequencies, a ferrite bead has high impedance and creates a large ground potential difference between the planes or PC board stack-up, add as many power and ground planes as possible. Keep the power and ground planes next to each other to ensure low-impedance stack-up or large natural capacitance stack-up.
- Add an EMI pi filter on all the signals exiting the box or entering the box.
- If the system fails EMI tests, find the source by tracing the failed frequencies to their source. For example, assume the design fails at 300 MHz but there is nothing on the board running at that frequency. The source is likely to be a third harmonic of a 100 MHz signal.
- Determine if the failed frequencies are common mode or differential mode. Remove all the cables connected to the box. If the radiation changes, it is common mode. If not, then it is differential mode. Then, go to the source and use termination or decoupling techniques to reduce the radiation. If it is common mode, add pi filters to the inputs and outputs. Adding a common choke onto the cable is an effective solution but an expensive method for EMI reduction.

For additional information on reducing EMI/EMC issues throughout the PCB design process, see the *PCB Design Guidelines for Reduced EMI* and *Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility*.

5.3 Electrostatic Discharge

A buildup of electrical charge can result in electrostatic discharge (ESD) to the device while in operation. Care should be taken when handling these microcontrollers and when storing them. All of the F2800x devices are tested to comply with the TI standard ESD specifications, including the peripherals and the port pins. They are rated to withstand the following ESD tests: human-body model (HBM), at 2 kV and charged-device model (CDM) at 500 V.

A supply voltage glitch or ESD will put the device in an unknown state. Therefore, it is important to have a good PCB layout for optimum noise and ESD performance. The similar ESD protection diodes can be utilized for JTAG pins as well. Keep the loop area of critical traces (in this case, JTAG, XRS, X1, X2) as small as possible. If your design needs to bring any pin, like a GPIO, to a connector (for external connectivity) be sure to take special ESD care by adding ESD protection parts. Some systems may require mechanical fixes like metallic shielding, rerouting of cabling, and so forth, to maintain ESD protection. When using these external ESD protection devices, be sure to carefully follow the layout guidelines specified in the device-specific data sheet to maximize its effectiveness.

6 Final Details and Checklist

The C2000 family of devices are feature-rich devices that can be utilized across a large range of systems. For the most optimal performance, these systems should be carefully designed and tested. To ease this process, TI has provided a quick spreadsheet outlining the most important care-abouts that should be made when utilizing these devices. At the end of each stage of the design process to mitigate overlooking important considerations, see the *F2800x Hardware Design Guide Checklist*.

7 References

- Texas Instruments: *TMS320F28004x Real-Time Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F28002x Real-Time Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F28003x Real-Time Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F280013x Real-Time Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F28004x Real-Time Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28003x Real-Time Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F2802x/TMS320F2803x to TMS320F28002x Migration Overview*
- Texas Instruments: *The TMS320F28004x Microcontroller: A Comparison to the TMS320F2806x and TMS320F2803x Microcontrollers*
- Texas Instruments: *Migration Between TMS320F28004x and TMS320F28002x*
- Texas Instruments: *Migration Between TMS320F28002x and TMS320F28003x*
- Texas Instruments: *Migration Between TMS320F28004x and TMS320F28003x*
- Texas Instruments: *C2000 Real-Time Control MCU Peripherals Reference Guide*
- Texas Instruments: *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers*
- Texas Instruments: *How to Maximize GPIO Usage in C2000 Devices*
- Texas Instruments: *I2C Bus Pullup Resistor Calculation*
- Texas Instruments: *Programming Examples and Debug Strategies for the DCAN Module*
- Texas Instruments: *TMDSFSIADAPEVM FSI Adapter Board User's Guide*
- Texas Instruments: *Fast Serial Interface (FSI) Skew Compensation*
- Texas Instruments: *ADC Input Circuit Evaluation for C2000 MCUs*
- Texas Instruments: *Methods for Mitigating ADC Memory Cross-Talk*
- Texas Instruments: *Charge-Sharing Driving Circuits for C2000 ADCs*
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- Texas Instruments: *Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility*
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- Texas Instruments: *C2000 F28004x Series LaunchPad™ Development Kit User's Guide*
- Texas Instruments: *C2000™ F28002x Series LaunchPad™ Development Kit*
- Texas Instruments: *Getting Started with C2000 Real-Time Control Microcontrollers (MCUs)*
- Texas Instruments: *Guidelines for Using Decoupling Capacitors on DSP Designs*
- Texas Instruments: *High-Speed DSP Systems Design Reference Guide*
- Texas Instruments: *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments: *High Speed PCB Layout Techniques*
- Texas Instruments: *PCB Layout Tips for High Resolution*
- Texas Instruments: *Latch-Up, ESD, and Other Phenomena*
- Texas Instruments: *High-Speed Layout Guidelines*

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (December 2022)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updated document to include information about TMS320F280013x family of C2000 devices	6

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