Application Report

Leverage New Type ePWM Features for Multiple Phase Control

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ABSTRACT

The enhanced pulse width modulator (ePWM) peripheral in C2000™ devices is the heart of the digital control systems, which are highly programmable, extremely flexible, and easy to use, while being capable of generating complex pulse width waveforms with minimal CPU overhead. With years of evolutions, more and more features are added or optimized in the new generation C2000 devices, especially for the ePWM peripheral. This application report discusses some of the new features that can help for the multiple phase topologies, including load on sync, simultaneous writes, global load and one shot reload.

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1 Introduction

In the digital power or industrial drive applications, multiple phase topologies are much more popular with the increasing power level requirement. Even for the same power level, compared with the single power stage, using multiple converters in parallel can generally bring the below benefits:

- Better efficiency with lower conduction loss, by averaging the whole current on different modules
- Lower voltage/current ripples with interleaved control

However, the control for multiple phase applications will be more complicated, considering how to manage time-base synchronization and maintain correct phase relationship among different ePWM modules. Building on 20 years of real-time control expertise, C2000 microcontrollers have developed lots of dedicated features in ePWM peripheral to handle the proper control for multiple phase applications. In this report, it will address how to better use the new features in Generation 3 devices(F2838x, F2837x, F2807x, F28004x, F28002x), including load on sync, simultaneous writes, global load and one shot reload. For a list of all devices with an ePWM module of the same type, to determine the differences between the types, and for a list of device-specific differences within a type, see the *C2000 Real-Time Control MCU Peripherals Reference Guide*.

2 New Features for Multiple Phase Control

For a typical multiple phase power converter, there are two factors shown below, which require careful consideration.

- Proper phase control

  Each ePWM module can be configured to allow a SyncIn pulse to cause the phase register (TBPHS) contents to be loaded into the time-base counter (TBCTR). Thus, by programming appropriate values into TBPHS, multiple PWM modules can address some power topologies that rely on phase relationship between legs (or stages) for correct operation, like interleaved PFC, interleaved LLC, and so forth. Basically, the phase relationship for N phases by setting the TBPHS values can be given with the following formula shown in Equation 1.

  $$TBPHS(N,M) = (TBPRD/N) \times (M-1) \quad (1)$$

  where, N = number of phases M = PWM module number.

  For example, for the 3-phase case (N=3), TBPRD = 600; TBPHS(3,2) = (600/3) x (2-1) = 200 (that is, Phase value for sync receiver module 2); TBPHS(3,3) = 400 (that is, Phase value for sync receiver module 3).

Figure 2-1 shows the associated timing waveforms for this phase relationship of 120°, and both sync receiver modules are synchronized to the sync source module.

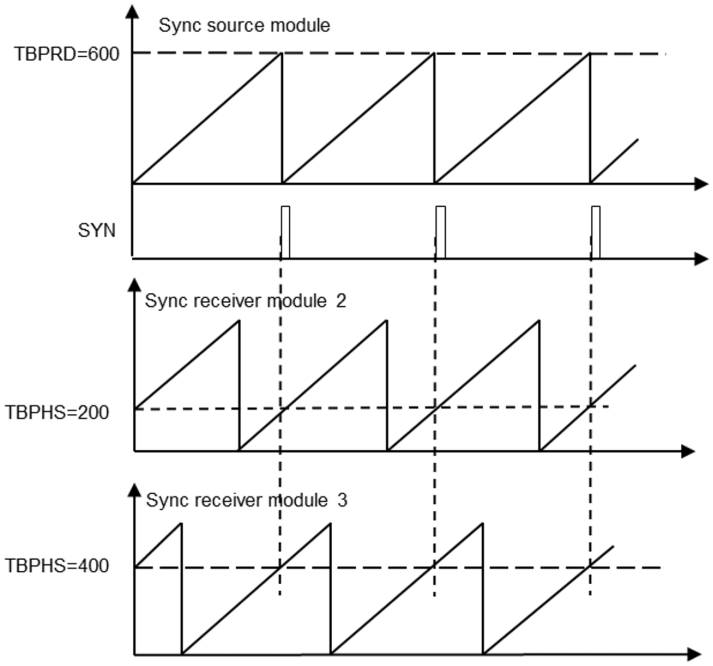

Figure 2-1. Timing Waveforms Associated With Phase Control Between Three Modules

- Update the registers across multiple ePWM modules properly

  In the actual applications, it is common that the EPWM outputs will change as required by the control loop, like variable duty cycles, frequencies, and so forth. It is critical to maintain the same phase relationship and synchronization among different ePWM modules after the change. Generally, in order to avoid corruption or spurious operation due to the register being asynchronously modified by software, shadow registers are enabled. The shadow register buffers or provides a temporary holding location for the active register. Users are responsible to select an event, when the shadow register's content will be transferred to the active register, which controls the hardware actions.

2.1 Shadow to Active Load on SYNC

In the previous generation C2000 devices, with Type 0 or Type 1 ePWM, the shadow register contents are transferred to the active register (TBPRD (Active) ← TBPRD (shadow)) when the time-base counter equals zero (TBCTR = 0x0000). It might cause the phase mismatch issue during variable frequency applications.

Figure 2-2 shows one example with 2 phase interleaved control, using 120° phase shift between ePWM1 and ePWM2 modules. And the ePWM1_ZERO event is selected as the SyncIn pulse for ePWM2. Assuming the ISR, to change the frequency, occurs between the ePWM1_ZERO event and ePWM2_ZERO event, and the TBPRD shadow registers of both ePWM1 and ePWM2 are updated with the new period value (1200), and TBPHS of ePWM2 is updated with 400 immediately. As shown in the waveforms, since the active TBPRD value can not be updated until the next ePWM2_ZERO event, so the phase shift relation is incorrect right after the frequency changes. Even worse, if the new TBPHS value of ePWM2 is larger than the previous period register value, it might cause unpredictable results when the TBCTR is loaded with this value at SyncIn event. As a result, the time-base counter keeps counting up beyond the period register value and goes all the way until it eventually rolls over.

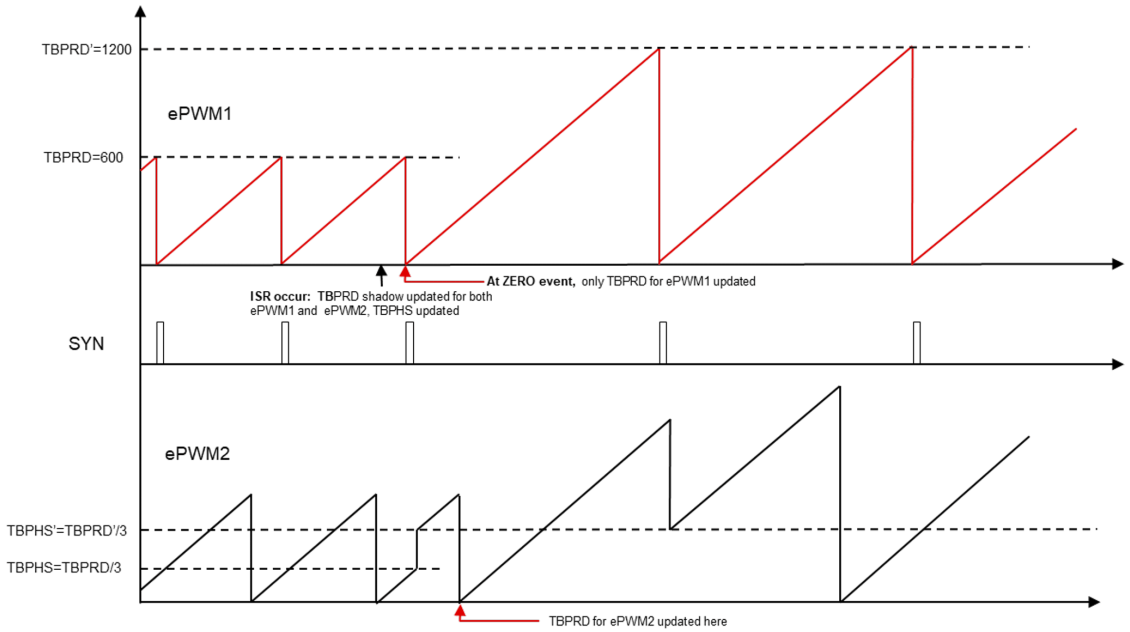

Figure 2-2. Phase Control Limitation With the Previous Generation C2000 Devices

The above risk has been resolved from Type 2 ePWM, which enables a sync event additionally, as determined by the TBCTL2[PRDLDSYNC] bit, to make the shadow to action loading effective for TBPRD and CMP registers. In this way, the correct phase shift can be obtained as shown in Figure 2-3.

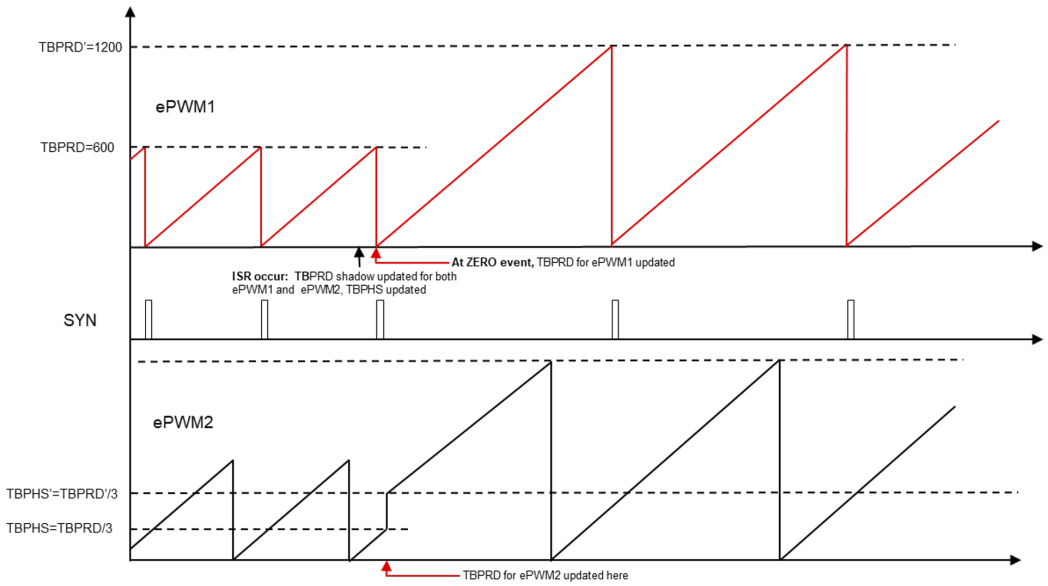

Figure 2-3. Correct Phase Shift Control With Shadow to Active Load at Sync Event

2.2 Simultaneous Writes to Registers Between Modules

In variable frequency applications, like LLC, the control ISR, where the period and compare registers will be updated, runs at a fixed frequency, which is asynchronous to the PWM switching frequency. Thus, it may happen that the ISR is triggered at a point in time close to the end of the switching cycle. If this is the case, it is possible that some part of the ISR code that updates the ePWM registers executes before the end of the cycle, while the remainder of the code executes in the next switching cycle. As shown in Figure 2-4, the period register for ePWM1 gets updated before the end of the switching cycle, while the period register for ePWM2 does not get updated on time. As a result, ePWM2 operates with the old PWM frequency, while ePWM1 operates with the new frequency, which can be disastrous for the power stage.

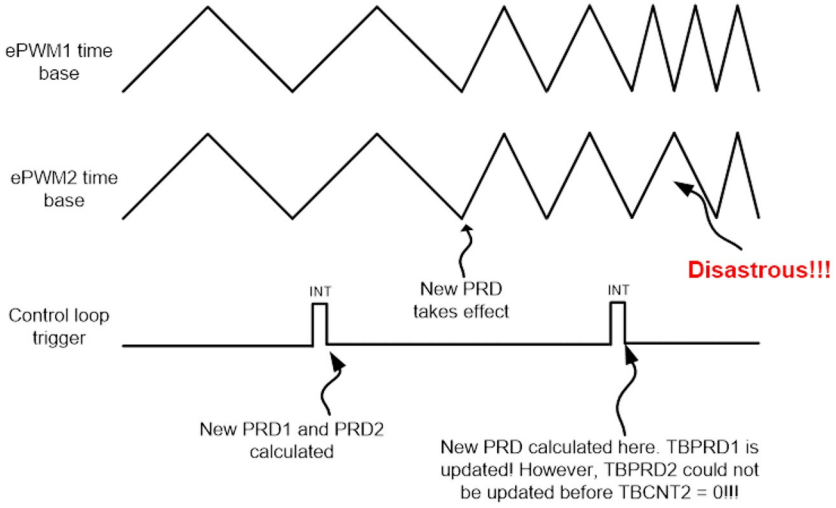

Figure 2-4. Potential Issue if the ISR Occurs at the Switching Cycle Boundary

A. Since this is a variable frequency application, Shadowed Period Load was used.

In order to update the shadow registers of different ePWM modules as soon as possible, new types of ePWM provide register linking scheme, with the link register EPWMXLINK. This prevents situations where a SyncIn pulse forces a shadow to active load of these registers before all registers are updated among ePWM modules. TBPRD:TBPRDHR, CMPA:CMPAHR, CMPB:CMPBHR, CMPC, and CMPD registers can be enabled with EPWMXLINK. The corresponding register will simultaneously be written with the same value which is written to the register of the ePWM module being linked to.

With the simultaneous write feature, the same register among different ePWM modules can be ensured to be updated always at the same time. However, since different shadow registers within the same ePWM module are still required to be updated in software manually one by one, it might happen that not all the ePWM registers are updated before the shadow to active load event. One disastrous result might occur as shown in Figure 2-5.

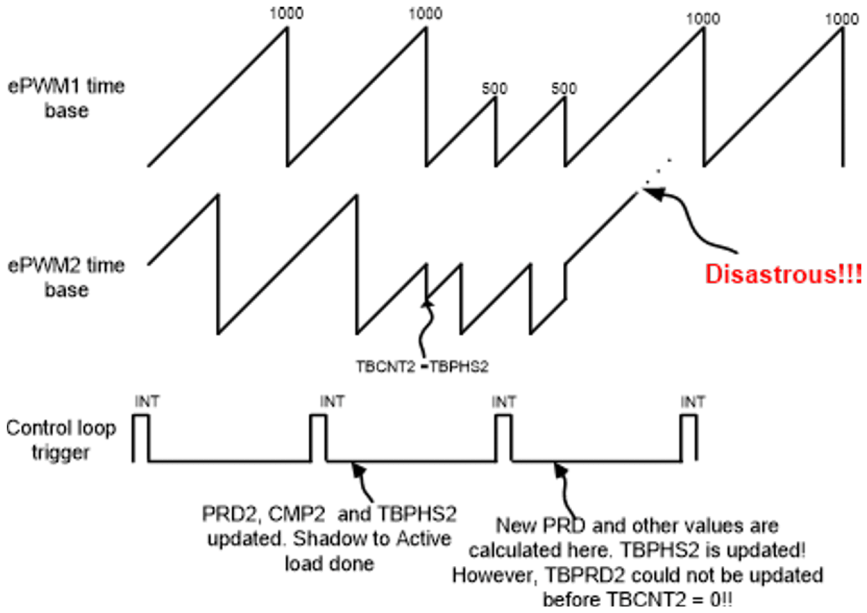

Figure 2-5. Disastrous Result When Different Registers are not Updated Simultaneously

2.3 Global Load and One Shot Load Mode

Global load and one shot load mode have been introduced to further address the optimized control for multiple ePWM modules, especially in variable frequency applications. The traditional shadow mode is defined as the local load mode, which is configured individually, while the global load mode applies for all the shadow registers enabled with GLDCFG[REGx]=1. When this feature is enabled (GLDCTL[GLD] = '1'), the transfer of contents from the shadow register to the active register, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL[GLDMODE]. The block diagram is shown in Figure 2-6.

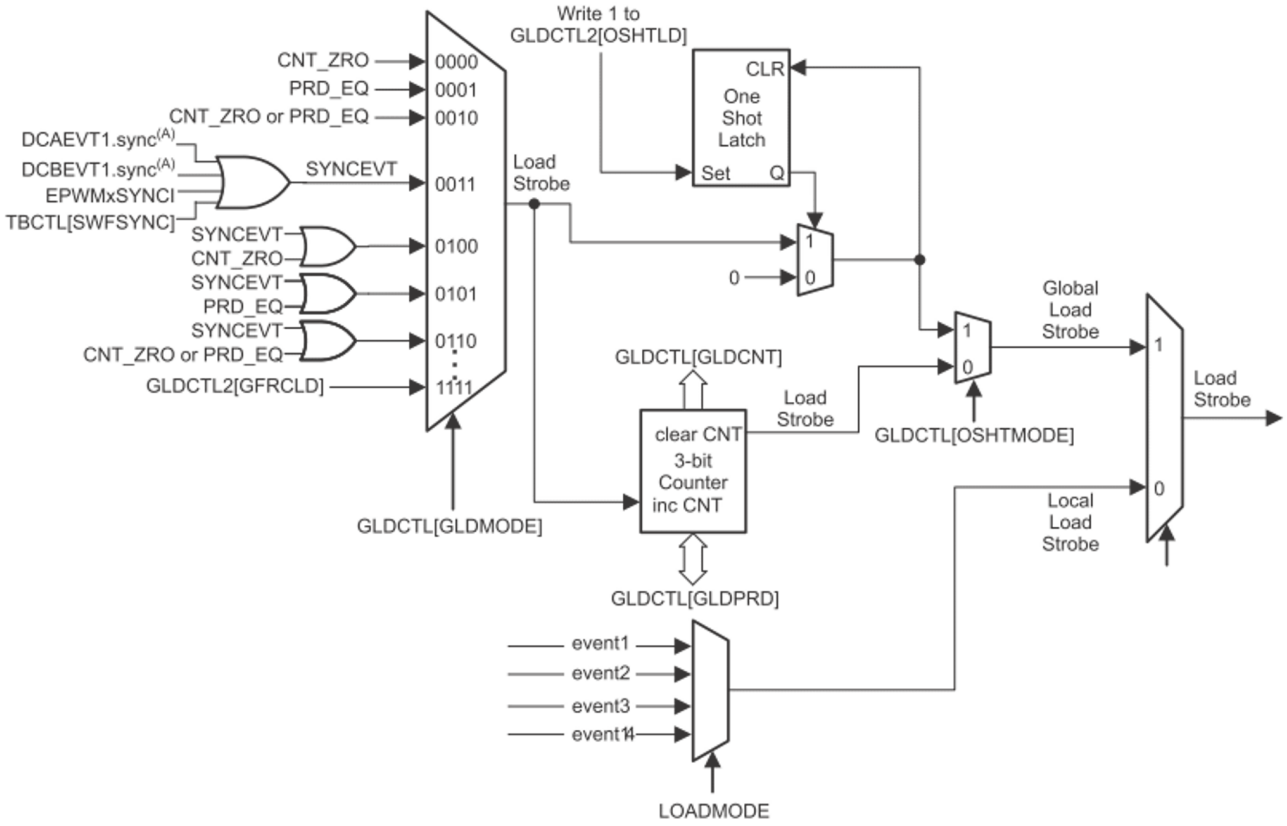

Figure 2-6. Global Load and One Shot Load Block Diagram

If the control ISR is asynchronous to the PWM switching frequency, one shot load mode is further required together with global load mode to ensure all the registers in multiple PWM modules are up to date at the selected event.

One shot load mode allows users to ensure the shadow register to active register transfers to occur once, with GLDCTL2[OSHTLD] = '1' under the global load mechanism. In another word, all the global load events are blocked until GLDCTL2[OSHTLD] = '1'. Besides, the GLDCTL2 register can also be linked across multiple PWM modules by using EPWMXLINK[GLDCTL2LINK]. Thus, with ePWM linking scheme, when enabling the one shot load mode after all the registers are updated, multiple PWM registers in one or more PWM modules will only take effect in the 1st global load event, and further events will be ignored.

2.3.1 Application Example

One configuration example, from TIDA-00961, is the showcase of using global load and one shot mode, located within the following directories after installing C2000Ware Digital Power SDK:

C:\ti\c2000\C2000Ware_DigitalPower_SDK_<version_number>\\solutions\tida_00961

The *TIDA-00961:High-Efficiency, 1.6-kW High-Density GaN-Based 1-MHz CrM Totem-Pole PFC Converter Reference Design* is a 2 phase interleaved totem pole PFC reference design, with critical-conduction-mode (CrM) in variable frequency operation up to 1 MHz, while the control ISR is running with 50 kHz. The following steps show the key configurations on how to use global load and one shot load mode, together with the example codes in TIDA-00961.

1. Select the related registers to enable the global load mode for both sync source and sync receiver ePWM modules, in the global load configuration register (GLDCFG[REGx]).
2. Define the global load event, in global shadow to active load control register (GLDCTL[GLDMODE]).
3. Enable the one shot load mode, by writing 1 to GLDCTL[OSHTMODE]).
4. Enable the global shadow to active load mode of registers, by writing 1 to GLDCTL[GLD]).
5. Use the linking scheme EPWMXLINK to link the GLDCTL2 register of the sync receiver ePWM modules to the sync source ePWM module's, in the register EPWMXLINK[GLDCTL2LINK].
6. During the ISR, after the related registers are updated manually, turn the one shot latch condition ON by writing 1 to GLDCTL2[OSHTLD] for the sync source ePWM module. In this way, the sync receiver ePWM modules will be also enabled with one shot mode under the linking scheme.

The below code shows the partial configurations of the sync source ePWM1 and the sync receiver ePWM2 in TIDA-00961.

- During initialization

```
// Sync source ePWM1 settings
EPWM_enableGlobalLoadRegisters(base1, EPWM_GL_REGISTER_CMPA_CMPAHR|
      EPWM_GL_REGISTER_TBPRD_TBPRDHR|EPWM_GL_REGISTER_DBRED_DBREDHR|
      EPWM_GL_REGISTER_DBFED_DBFEDHR|EPWM_GL_REGISTER_CMPC);
EPWM_setGlobalLoadTrigger(base1, EPWM_GL_LOAD_PULSE_CNTR_PERIOD);
EPWM_enableGlobalLoadOneShotMode(base1);
EPWM_enableGlobalLoad(base1);

// Sync receiver  ePWM2 settings

EPWM_enableGlobalLoadRegisters(base2, EPWM_GL_REGISTER_CMPA_CMPAHR|
      EPWM_GL_REGISTER_TBPRD_TBPRDHR|EPWM_GL_REGISTER_DBRED_DBREDHR|
      EPWM_GL_REGISTER_DBFED_DBFEDHR);
EPWM_setGlobalLoadTrigger(base2, EPWM_GL_LOAD_PULSE_SYNC);
EPWM_enableGlobalLoadOneShotMode(base2);
EPWM_enableGlobalLoad(base2);

EPWM_setupEPWMLinks(base2, EPWM_LINK_WITH_EPWM_2, EPWM_LINK_GLDCTL2);
```

- During control ISR

```
EPWM_setGlobalLoadOneShotLatch(HIGH_FREQ_PWM1_BASE);
```

2.3.2 Boundary Case

Considering all the possible operation conditions, the below corner case will be discussed, as shown in Figure 2-7. ePWM2 is configured to enable the phase shift to ePWM1 with 120°, where the TBPHS is PRD/3=200. And ePWM2 output sets high at CTR = Zero, and clears low at CTR = CMPA, where CMPA=300 at the beginning. All the registers of ePWM1 and ePWM2 are enabled with global load and one shot mode, with the global load event defined as CTR = Zero of ePWM1. Assuming a sudden frequency change event occurs during the ISR, before the global load event, where the new period value PRD' changes to 2*PRD=1200, and TBPHS'= PRD'/3=400, while CMPA stays the same as previous. Then, as shown in the Figure 2-7, when the next global load event comes, the time-base counter of ePWM2 will jump from 200 to 400, which means CTR = CMPA event will be missed in the first PWM cycle after the frequency changes. This might cause severe risks for the system, with the ePWM2 output on time extending unexpectedly.

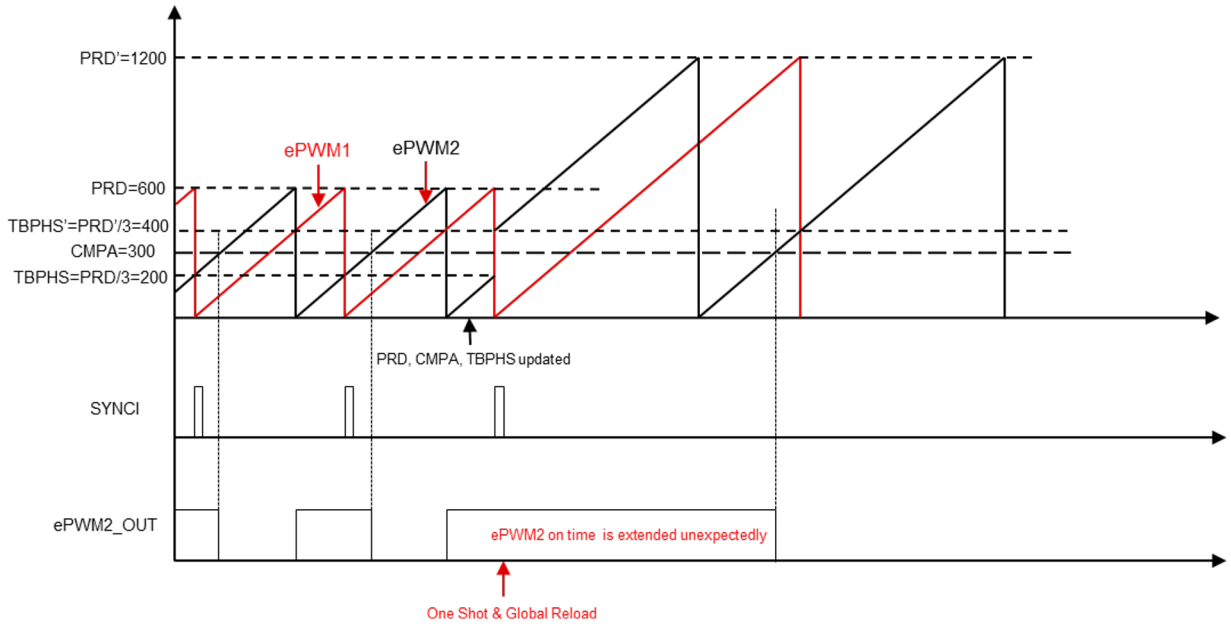

Figure 2-7. Corner Case During Variable Frequency Applications

2.3.2.1 Workaround Option 1

To avoid the above results, the below workaround could be an option, as shown in Figure 2-8. The global load event of ePWM1 is defined as CTR = Zero, while the global load event of ePWM2 is defined as sync event or CTR = Zero. During the ISR to update the ePWM registers, it is suggested to monitor the new CMPA and TBPHS values with their previous ones. If the new TBPHS register value and counter-compare register value will cause the PWM counter to jump over the CMPA value, the counter-compare register value can be changed temporarily, and then changed back to the required one in the next ISR.

Using the same example as above, when the new phase register TBPHS' is updated to 400, CMPA is required to be changed to CMPA'= TBPHS'+1=401. Then, one shot load mode is enabled, so when the next global event occurs, the expected phase shift can be still maintained, while the duty cycle of ePWM2 is also clamped under the control. Then, during the next ISR, it is required to change the CMPA value back to the expected one, and also enable one shot load mode again, so that the duty cycle is corrected in the following switching cycle.

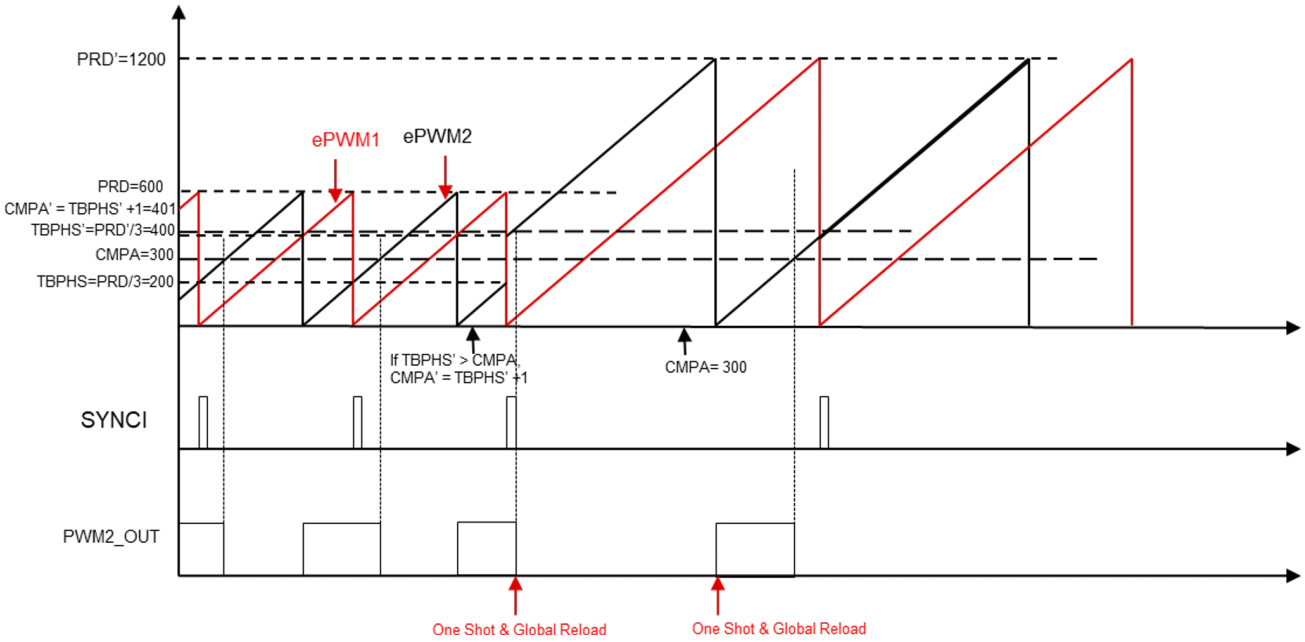

Figure 2-8. Workaround for the Corner Case

2.3.2.2 Workaround Option 2

The above workaround option requires extra software bandwidth to deal with such corner case, while another option with the configurable logic block (CLB) is hardware based and more straightforward. The basic idea is to use CLB to monitor the on time of the specific ePWM output, and clamp it within the expected duty cycle if the above corner case is going to occur.

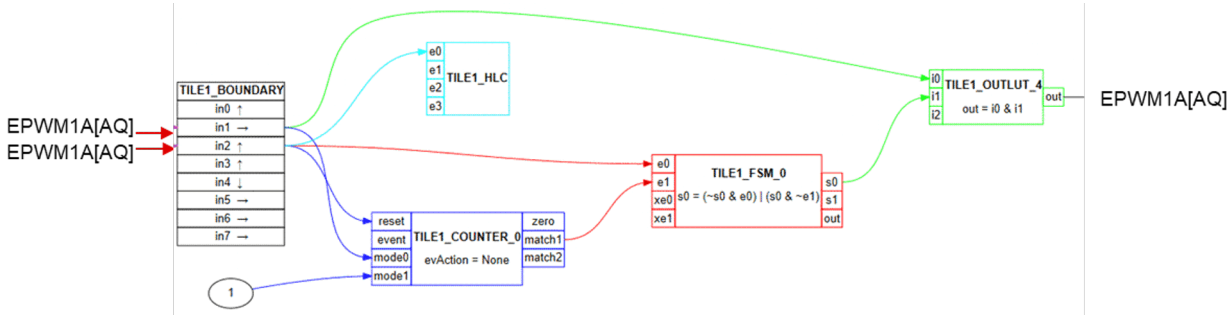

Figure 2-9. CLB Option Block Diagram

As shown in Figure 2-10, with ePWM1A as an example, the output of the AQ submodule of ePWM1 is used for the CLB input signals, and COUNTER0 is used to count the on time of ePWM1A. FSM0 will provide the clamped signals, where FSM0 e0 refers to the rising edge of EPWM1A[AQ], and FSM0 e1 refers to the COUNTER0 match1 event. Thus, the actual EPWM1A[AQ] signal is the AND logic with FSM0 s0.

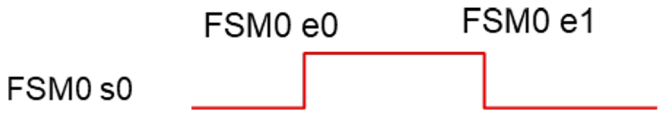

Figure 2-10. FSM Operation

Based on such scheme, every time the multiple ePWM registers are updated, the match1_val register of COUNTER0 is also updated with the clamped duty cycle, which is the CMPA value in Section 2.3.2.1. In this way, the ePWM output can be always ensured in a safe status. The above configuration has been validated with the F280049 control card, as shown in Figure 2-11, where the duty cycle of ePWM1A is initially set with 50%, and it is finally clamped to 30% by CLB.

Figure 2-11. Example Waveform Validated

3 References

- Texas Instruments: *C2000 Real-Time Control MCU Peripherals Reference Guide*
- Texas Instruments: *TMS320F28004x Real-Time Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28004x Microcontrollers Data Manual*
- Texas Instruments: *High-Efficiency, 1.6-kW High-Density GaN-Based 1-MHz CrM Totem-Pole PFC Converter Reference Design*

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