Application Report

Jacinto 7 Camera Capture and Imaging Subsystem

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ABSTRACT

This application report summarizes TDA4VM and DRA829 System-on-Chip (SoC) [1, 2] camera capture capabilities and imaging processing pipeline features. For more information on the complete feature set, see the Jacinto 7 Technical Reference Manual (TRM) [3].

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Trademarks

1 Introduction

Cameras are key component of vision based systems in industrial and automotive markets. The number of cameras, frame rates and resolutions of those cameras have been increasing significantly in industrial and automotive applications including machine vision, robotics, video surveillance, Advanced Driver Assistance Systems (ADAS), and so forth. It is critical for an application processor used in such applications to capture and process those camera inputs including raw input. Jacinto 7-based high-performance heterogenous application processors, including TDA4VM and DRA829 [1] and [2], provide capabilities to capture and process multiple camera inputs to optimize performance, power and memory throughput.

1.1 Jacinto 7 Imaging Subsystem Overview

Jacinto 7 camera and capture system is Texas Instruments' 7th generation imaging subsystem (ISP) built on the top of more than 20 years of innovation in multiple SoC families deployed in millions of products. Some of the differentiated features include:

- Compatible with all image sensor formats
- Low power, higher performance, full-image pipeline with optimized memory throughput
  - Lens Shading Correction, Noise Filter, WDR, Demosaicing, Color Space Conversion, Image Pyramids
- Two high-speed interfaces for high resolution multi-camera capture
  - Up to 16 virtual channels per interface. Up to 32 camera capture.
- Concurrent Human + Machine Vision Outputs
  - Human Vision ISP features:
    - 140 dB WDR
    - Locally adaptive Tone Mapping
    - Dual noise filters
    - 8b output
  - Machine Vision ISP features:
    - Advanced CFA Interpolation supports all 2x2 CFA formats

2 Camera Capture Subsystem

TDA4VM/DRA829 camera capture subsystem includes 2x MIPI CSI-2 interface and video processing front end (VPFE) as shown in Figure 2-1.

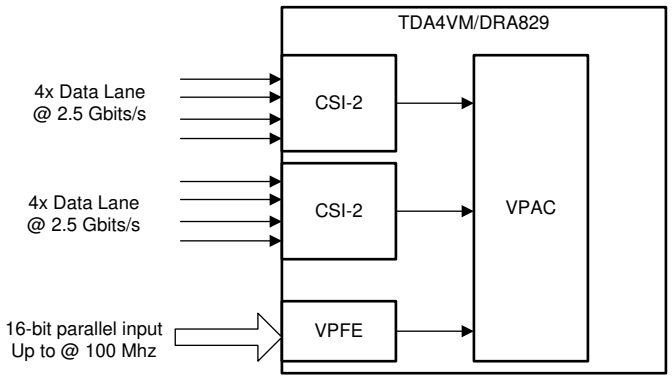

Figure 2-1. TDA4VM/DRA829 Camera Capture Subsystem

2.1 MIPI-CSI2

TDA4VM/DRA829 MIPI-CSI2 interface supports following features:

- 2x MIPI D-PHY with 4 lanes (2.5Gbps/lane)
- Supports 8 sensors with de-serializer Hubs
- 2x Camera Adaptation Layer (CAL)
  - Protocol stack for MIPI CSI2
  - Supports all MIPI supported formats
    - RAW/DPCM/YUV
    - RAW 8, 10, 12, 14, 16 bits
      - Companded or linear
    - Concurrent read of pixel stream from SDRAM
  - Real-time priority on I/F port traffic

2.2 The Video Processing Front End

The Video Processing Front End (VPFE) is an input interface module that receives raw image/video data or YUV digital video data from external imaging peripherals such as image sensors. VPFE supports following features:

- Support for conventional Bayer pattern and Foveon sensor formats.
  - Generates HD/VD timing signals and field ID to an external timing generator or can synchronize to the external timing generator
  - Support for progressive (non-interlaced) and interlaced sensors
  - Support for up to 110-MHz sensor clock.
  - Support for REC656/CCIR-656 standard (YCbCr 422 format, either 8- or 16-bit).
  - Support for YCbCr 422 format, either 8- or 16-bit with discrete HSYNC and VSYNC signals.
  - Support for up to 16-bit input.

3 The Vision Pre-Processing Accelerator

The Vision Pre-processing Accelerator (VPAC) subsystem is a set of common vision primitive functions, performing pixel data processing tasks, such as: color processing and enhancement, noise filtering, wide dynamic range (WDR) processing, lens distortion correction, pixel remap for de-warping, on-the-fly scale generation, and on-the-fly pyramid generation. The VPAC offloads these common tasks from the main SoC processors (ARM, DSP, and so forth), so these CPUs can be utilized for differentiated high-level algorithms. The VPAC is designed to support multiple cameras by working in time-multiplexing mode. The VPAC works as a front end to vision processing pipeline and provides for further processing by other vision accelerators or processor cores inside the SoC.

Figure 3-1 shows the VPAC high-level block diagram.

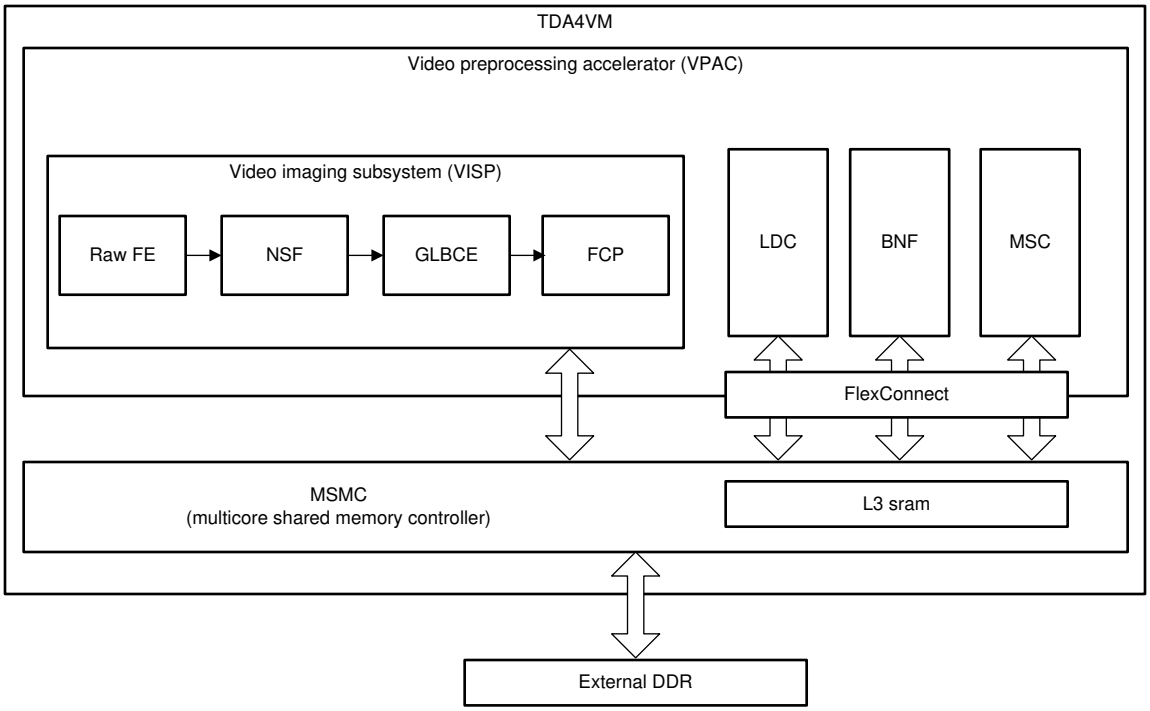

Figure 3-1. VPAC Block Diagram

The VPAC is composed on following major blocks:

- Video Imaging Subsystem (VISS)
- Lens Distortion Correction (LDC)
- Bilinear Noise Filter (BNF)
- Multi-scaler (MSC)

3.1 Video Imaging Subsystem (VISS)

VISS performs image processing on raw data and outputs RGB and/or YUV image. Video Imaging Subsystem (VISS) includes following components:

- Raw Front End (Raw FE) that implements:
  - Wide Dynamic Range (WDR) merge
  - Defect Pixel Correction (DPC)
  - Lens Shading Correction (LSC)
  - Decompounding
  - 3A Statistics
  - White Balance
- Noise Filter (NSF)
  - Bayer domain spatial noise filter
- Global and Local Brightness Contrast Enhancement (GLBCE) for adaptive local tone mapping
- Flex Color Processing (FCP),which supports
  - Demosaicing, color correction, color space conversion and gamma conversion

VISS pipeline can process data at 1 pixel per cycle. On TDA4VM, VISS system can be clocked at 720 Mhz, which enables 720 Mpixel/s processing capability.

3.2 Lens Distortion Correction (LDC)

LDC module remaps pixels from a distorted input space to an undistorted output space applying perspective transform/homography operations. LDC supports following features:

- Lens distortion correction, stereo rectification, generic pixel remap
  - Multi-region mode for enhanced image quality
  - Superior correction mode - Look Up Table based backmapping method
  - Sub-pixel accuracy using bicubic interpolation
  - DDR b/w optimized architecture
    - Supported Formats:
  - YUV 420 (NV12/NV21)
  - Up to 12 bits/component
    - Interpolation Type:
  - Bicubic (2 cyc/Pixel)
  - Bilinear (1 cyc/Pixel)

3.3 Multi-Scalar (MSC)

MSC generates up to 10 scaled output from a given input with various scaling ratios. MSC supports following features:

- Multi-scaling capable: 10 simultaneous scaled outputs from 1 or 2 input planes
- Each scaling engine can be configured to perform Pyramid or inter-octave scale generation
- Supported scaling ratios between 1x to 0.25x
- 7 scales between each octave → 1.09 x
- Single cycle/pixel performance

3.4 Bilateral Noise Filtering (BNF)

BNF implements Bilateral filtering to remove noise and it supports following features:

- Bilateral and General Filtering
- Filter size up to 5x5
- True 2D Bilateral filtering
- Filter size up to 5x5 of programmable static weights
- 1 cycle/pixel Performance
- Supported Formats:
  - YUV 42, 12 bit
  - 8 bit can be supported using LDC/Scaler
  - Line based input and Output

3.5 Software Availability for Camera Sensors

For the camera sensor drivers available, see the Jacinto 7 processor SDK imaging release notes (https://software-dl.ti.com/jacinto7/esd/processor-sdk-rtos-jacinto7/latest/exports/docs/imaging/imaging_release_notes.html#ImageSensor_Support).

4 Example Use-Cases

Some common example camera use-cases are shown below assuming 12-bit per pixel raw camera input.

4.1 4x Camera Use-Case With MIPI Aggregator

Figure 4-1 shows high-level block diagram where 4x 2Mpixel @30fps camera inputs are directly connected to TDA4VM using MIPI CSI-2 aggregator and data flow.

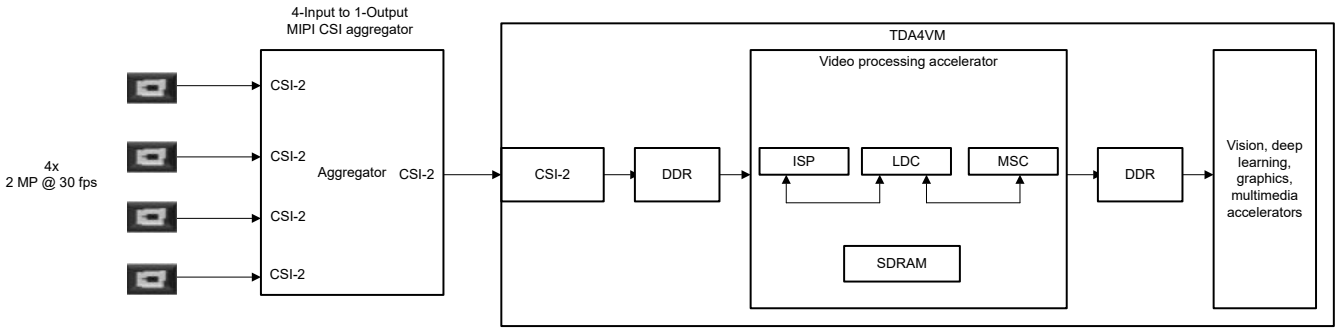

Figure 4-1. 4x Camera Use-Case With MIPI CSI-2 Aggregator and Data Flow

Table 4-1 summarizes total utilization for this use-case.

Table 4-1. Total Utilization for This Use Case

IP	Max Throughput	Utilization	Utilization (Percentage)
CSI-2	10 Gbits	2.88 Gbits	28.80%
VPAC	720 MP/s	240 MP/x	33.33%

4.2 Generic 8-Camera Use-Case

Figure 4-2 shows high-level block diagram for 8x 2Mpixel @30fps camera inputs remotely connected over FPDLink serializers and deserialiers and data flow.

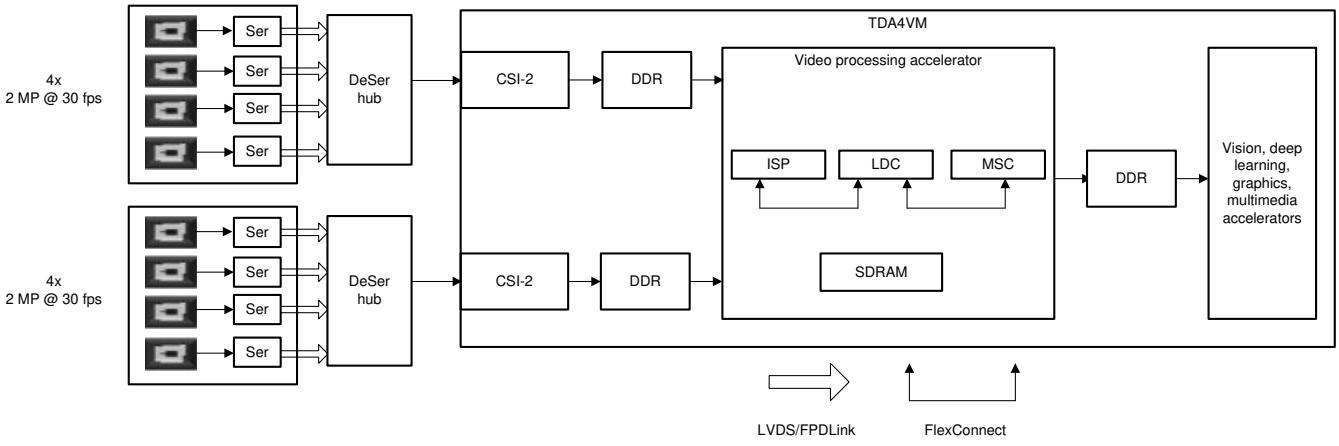

Figure 4-2. 8x 2Mpixel Block Diagram and Data Flow

For the FDPLink-based multi-camera setup, see [5].

Table 4-2 summarizes total utilization for this use-case.

Table 4-2. Total Utilization for This Use Case

IP	Max Throughput	Utilization	Utilization (Percentage)
CSI-2 (1st instance)	10 Gbits	2.88 Gbits	28.80%
CSI-2 (2nd instance)	10 Gbits	2.88 Gbits	28.80%
VPAC	720 MP/s	480 MP/x	66.66%

4.3 ADAS Use Case

Figure 4-3 shows high-level block diagram for a common ADAS use-case where

- 1x 8Mpixel @30 fps is used for front camera
- 1x 1Mpixel camera is used for DMS and
- 4 x 2Mpixel @30 fps is used for 3-D SRV.

These cameras are remotely connected over FPDLink serializer and deserializer.

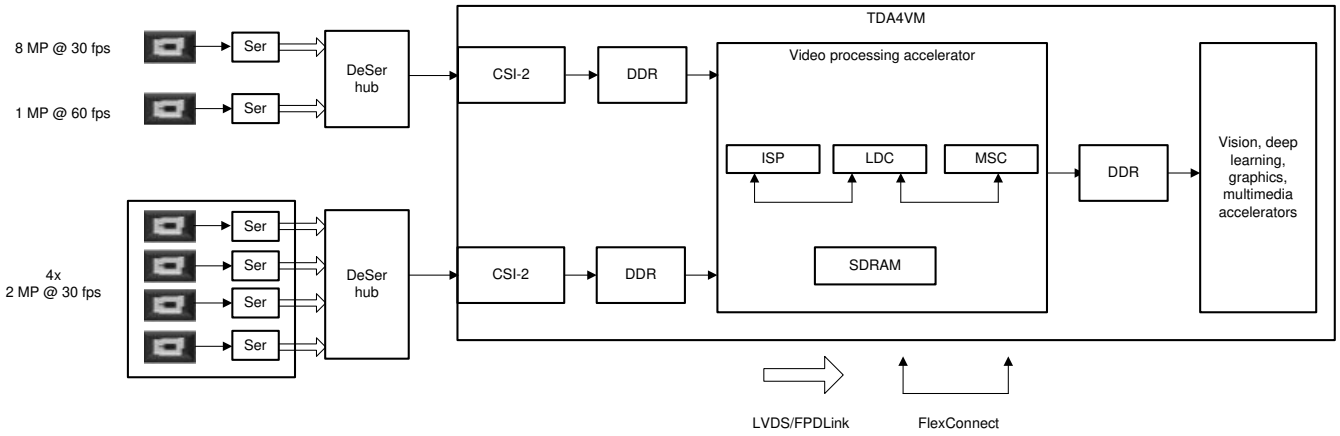

Figure 4-3. An Example ADAS Use Case and Data Flow

For FDPLink-based multi-camera setup, see [5].

Table 4-3 shows total utilization for this use-case.

Table 4-3. Total Utilization for This Use Case

IP	Max Throughput	Utilization	Utilization (Percentage)
CSI-2 (1st instance)	10 Gbits	3.6 Gbits	36%
CSI-2 (2nd instance)	10 Gbits	2.88 Gbits	28.80%
VPAC	720 MP/s	480 MP/x	66.66%

5 References

1. TDA4VM product page
2. DRA829V product page
3. Texas Instruments: *DRA829/TDA4VM/AM752x Technical Reference Manual*
4. Software Development Kit for TDA4VM/DRA829 Jacinto Processors
5. TDA4VM/DRA829 Evaluation Module

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