

Application Note

MMC SW Tuning Algorithm



ABSTRACT

This application report describes how to perform software tuning with Multi-Media Cards (MMCs) at speed modes at or above 50 MHz (DDR50, SDR50, SDR104, HS200, HS400) on the AM65x, DRA80x, DRA82x, TDA4VM family of devices. This document describes why the tuning algorithm is needed and how it works to achieve a functional system.

Table of Contents

1 Tuning Algorithm Overview	2
2 Hardware Tuning Algorithm	2
3 SW Tuning Algorithm	3
4 Revision History	5

List of Figures

Figure 3-1. MMC SW Tuning Algorithm.....	3
Figure 3-2. Setup Hold Time Requirements.....	4
Figure 3-3. Selection of Tuning Ratio for Functionality With DLL Enabled.....	4

Trademarks

All trademarks are the property of their respective owners.

1 Tuning Algorithm Overview

The read tuning algorithm is recommended by the SD Group and JEDEC Solid State Technology Association to compensate for timing variations due to a collection of system factors above 50 MHz high speed of operation. These factors include changes in silicon processes, operating temperature and voltage, PCB loading, as well as SD and eMMC slave device output timing.

During the read tuning process, the CLK-DAT latching position is adjusted through the delay module in single steps increments across a full range of 32 ratio elements. This adjustment can be done via automatic hardware tuning or manual software tuning. Limitations exist with the hardware tuning mechanism so the software tuning mechanism is the preferred method of implementation. This application report briefly describes the hardware tuning mechanism limitation and then goes over the software tuning algorithm in detail.

2 Hardware Tuning Algorithm

Hardware tuning is executed by setting MMCSDx_HOST_CONTROL2[6] EXECUTE_TUNING bit to '1' and issuing CMD19/CMD21 repeatedly. The hardware then automatically sequences through all 32 delay ratios and selects the optimal one for functionality runs.

When the hardware tuning mechanism is used, you do not have visibility into the pass and fail result of each delay ratio elements, nor the final delay ratio element chosen to be utilized during functionality runs. This means a lack of visibility into the inner working of the hardware tuning module for debug needs. As a result, the software tuning algorithm is the recommended method of implementation on all systems.

3 SW Tuning Algorithm

For software tuning, everything that would have been done automatically by the hardware module is now enabled via software coding. The software program will sequence through all 32 delay ratio elements, issue CMD19/CMD21 and record the pass and fail results at each ratio element. Then, the program will find the optimal delay ratio element for functionality use. Figure 3-1 describes the process in detail.

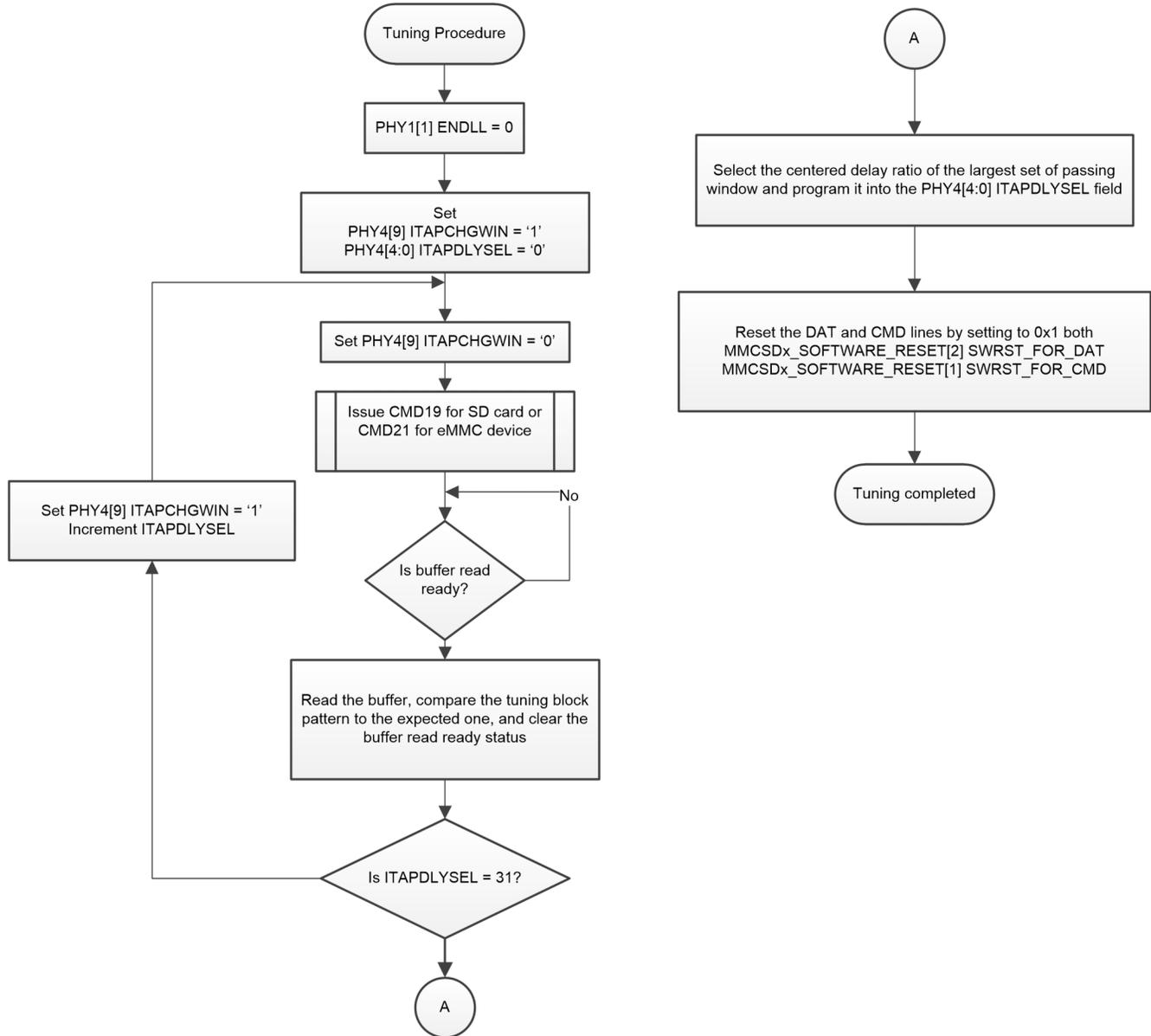


Figure 3-1. MMC SW Tuning Algorithm

If DLL is used (ENDLL = '1'), then the 32 ratio elements will constitute a whole clock cycle. Delaying the CLK by Ratio 32 will mean delaying the CLK by Ratio 0. As a result, the biggest passing window should be taken as the window that wrapped around from the end to the beginning of the delays. If DLL is not used (ENDLL = '0'), the biggest passing window should be taken as the window without the wraparound applied.

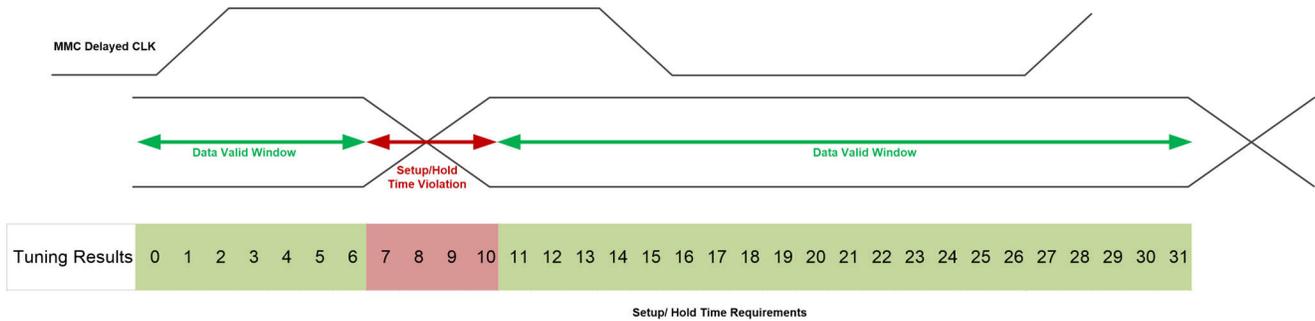


Figure 3-2. Setup Hold Time Requirements

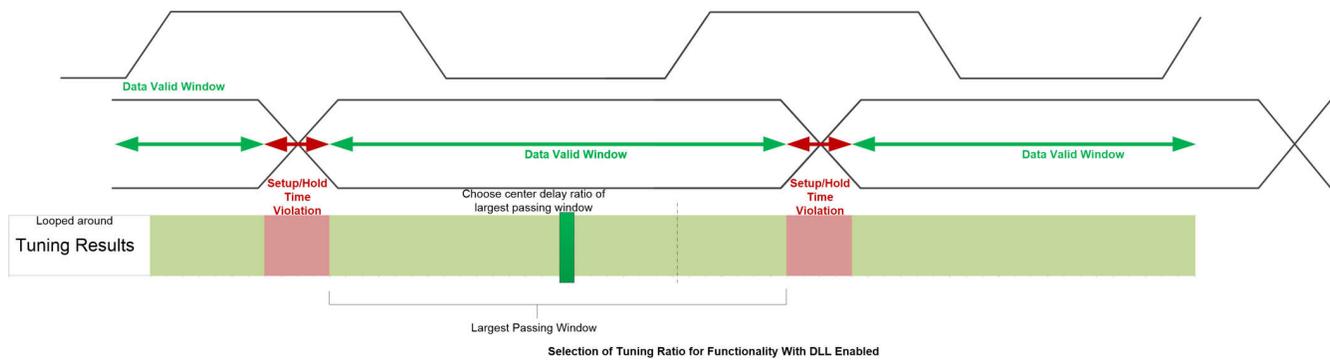


Figure 3-3. Selection of Tuning Ratio for Functionality With DLL Enabled

As a safety precaution, software code should also implement a re-tuning mechanism to re-tune the delay module if the MMC functionality fails. This can be done by checking for data line status bits for errors. If errors occurred, re-execute the tuning sequence. Re-tuning should also be done at timer expiration by using the re-tuning functionality.

Note

Uncommon Data Error During Tuning

Note that during software tuning there can be a few uncommon data errors, such as data or cmd line being reset. These data errors that happen during software tuning should be ignored by the driver because these errors are expected while tuning.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from September 1, 2020 to May 15, 2024 (from Revision * (September 2020) to Revision A (May 2024))

Page

-
- Added Note.....3
-

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated