TMS320F2802x/TMS320F2803x to TMS320F28002x Migration Overview

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ABSTRACT

This application report describes the differences between the Texas Instruments TMS320F2802x/TMS320F2803x and the TMS320F28002x microcontrollers for the purpose of assisting with application migration. Functions that are identical in both devices are not necessarily included. All efforts have been made to provide a comprehensive list of the differences between the two device generations within the C2000™ product family; however, the descriptions are explained only to the extent of highlighting areas that require attention when migrating from one device to another. For a detailed description of features specific to each device, see the most recent device-specific data sheet, technical reference manual, errata, user guides, and software packages.

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1   Introduction

The TMS320F2802x/TMS320F2803x and TMS320F28002x are device members of the C2000™ MCU product family. These devices are most commonly used within embedded control applications. The TMS320F28002x devices feature an updated version of the enhanced control peripherals found on the TMS320F2802x/TMS320F2803x, which allows for greater flexibility and improved application performance. In addition, the TMS320F28002x devices feature a boot mode flow which enables expanded booting options that provide the ability to use alternate, reduce, or completely eliminate boot mode selection pins, and an analog subsystem interconnect which enables a very flexible pin usage, allowing for smaller device packages. Central to the analog subsystem interconnect are multiple analog comparator subsystems (CMPSS). Enhancements to the CPU include the addition of a floating-point unit (FPU), a trigonometric math unit (TMU), a fast integer division unit (FINTDIV), and a cyclic redundancy check unit (VCRC). Other device enhancements include a direct memory access (DMA) controller and three cross-bars (XBARs) for providing a flexible means for interconnecting multiple inputs, outputs, and internal resources. A PMBus communication interface is available for additional connectivity. Expanded debug and system analysis capabilities are supported with the Embedded Real-Time Analysis and Diagnostic (ERAD) module.

For the purposes of migration, these devices will be referenced in two groups:

- TMS320F2802x and TMS320F2803x – these devices will be referenced as the F2802x and F2803x, respectively. When referenced as both the F2802x and F2803x, this combined group of devices may be referenced as F2802x/03x. If a feature is unique to a specific device type, it will be referenced as F2802x or F2803x.
- TMS320F28002x – this device will be referenced as the F28002x.
  - The TMS320F28002xC devices have a Configurable Logic Block (CLB) and it will be referenced as F28002xC.

For a full list of devices currently available within the F2802x, F2803x, and F28002x families, see the TI website at http://www.ti.com/c2000.

As the focus of this document is to describe the differences between the two device groups, the descriptions are explained only to the extent of highlighting areas that require attention when moving an application from one device to the other. For a detailed description of features specific to each device, see the device-specific technical reference manuals and user's guides available on the TI website at http://www.ti.com/c2000. This application report does not cover the silicon exceptions or advisories that may be present on each device.

Consult the following silicon errata for specific advisories and workarounds:

- *TMS320F28002x MCUs Silicon Errata*
- *TMS320F2803x MCUs Silicon Silicon Errata*
- *TMS320F2802x, TMS320F2802xx MCUs Silicon Errata*

> **NOTE:** Always refer to the TMS data sheet for information regarding any electrical specifications.

1.1 *Abbreviations*

The following abbreviations are used in this document:

- F2802x: Refers to the TMS320F2802x devices. For example, TMS320F28027, TMS320F28026, TMS320F28023, TMS320F28022, TMS320F28021, TMS320F28020, and TMS320F280200. The individual devices in this group are abbreviated as F28027, F28026, F28023, F28022, F28021, F28020, and F280200.
- F2803x: Refers to the TMS320F2803x devices. For example, TMS320F28035, TMS320F28034, TMS320F28033, TMS320F28032, TMS320F28031, and TMS320F28030. The individual device in this group is abbreviated as F28035, F28034, F28033, F28032, F28031, and F28030.
- F28002x: Refers to the TMS320F28002x devices. For example, TMS320F280025, TMS320F280025C, TMS320F280024, TMS320F280024C, TMS320F280023, TMS320F280023C, TMS320F280022, and TMS320F28021. The individual devices in this group are abbreviated as F280025, F280025C, F280024, F280024C, F280023, F280023C, F280022, and F280021.

For a full list of devices currently available within the F2802x, F2803x, and F28002x families, see the TI website at http://www.ti.com/c2000.

2 Central Processing Unit (CPU)

The F28002x devices extend the capabilities of the existing TI C28x 32-bit fixed-point CPU architecture by adding a floating-point unit (FPU), a trigonometric math unit (TMU), a fast integer division unit (FINTDIV), and a cyclic redundancy check unit (VCRC). No changes have been made to existing instructions, pipeline, or memory bus architecture; and programs written for the C28x CPU are completely compatible with these architectural enhancements.

The addition of the Floating-Point Unit (FPU) to the C28x fixed-point CPU core enables support for hardware IEEE-754 single-precision floating-point format operations. The FPU adds a set of floating-point registers (R0H to R7H, STF, RB) and instructions as an extension to the standard C28x architecture, providing seamless integration of floating-point hardware into the CPU. In the pipeline decode stage, the instruction is decoded to determine if it is a standard C28x instruction or a FPU instruction, and is routed accordingly. Since the FPU instructions are extensions of the standard C28x instruction set, most instructions operate in one or two pipeline cycles and some can be done in parallel. Also, the FPU latched overflow and underflow flags are connected to the peripheral interrupt expansion (ePIE) block which assists in debugging overflow and underflow issues.

The Trigonometric Math Unit (TMU) is an extension of the FPU and the C28x instruction set, and it efficiently executes trigonometric and arithmetic operations commonly found in control system applications. Similar to the FPU, the TMU provides hardware support for IEEE-754 single-precision floating-point operations. Seamless code integration is accomplished by built-in compiler support that automatically generates TMU instructions where applicable. This dramatically increases the performance of trigonometric functions, which would otherwise be very cycle intensive. The F28002x TMU includes two additional instructions to support the computation of the floating-point power function "powf". These instructions calculate the inverse binary exponent and the base two logarithm, and can be combined to compute the power of a floating-point number raised to the power of another floating-point number. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. Since the TMU uses the same register set and flags as the FPU, there are no special considerations relating to interrupt context save and restore.

The fast integer division unit (FINTDIV) is an extension of the C28x FPU and it includes an extended instruction set for supporting fast division operations. All instructions execute in a single cycle and three types of integer division are supported (Truncated, Modulus, Euclidean) of varying data type sizes (16/16, 32/16, 32/32, 64/32, 64/64) in unsigned or signed formats. Truncated format is the traditional division performed in C language (where "/" is the integer, and "%" is the remainder); however, the integer value is non-linear around zero. Modulus and Euclidean formats are more appropriate for precise control applications because the integer value is linear around the zero point, and this avoids potential calculation hysteresis. Both the Modulus and Euclidean divisions are supported by C intrinsics, and the C28x compiler supports all three division formats for all data types. Since the FINTDIV uses the existing FPU register set to carry out the FINTDIV operations, there are no special considerations relating to interrupt context save and restore.

The cyclic redundancy check unit (VCRC) is an extension of the C28x CPU and it includes registers and instructions to support CRC algorithms. CRC algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The VCRC can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs, and it is capable of computing the polynomial code checksum for a block length of 10 bytes in 10 cycles (i.e. a byte of data in a single cycle). For custom CRC polynomials the execution time increases to three cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

The C28x CPU, FPU, TMU, FINTDIV, and VCRC architecture and instruction set are documented in the following reference guides:

- *TMS320C28x CPU and Instruction Set Reference Guide*
- *TMS320C28x Extended Instruction Sets Technical Reference Manual*
- *C2000 Real-Time Control Peripherals Reference Guide*
  - This document describes the differences for the above 'unit' types; where a type change represents a major functional feature difference.
- *TMS320F28002x Microcontrollers Technical Reference Manual*

3 Development Tools

The F28002x devices have a new set of bit field header files, a new driver library, and new code examples, which are available in C2000Ware. C2000Ware is the successor to controlSUITE as the centralized repository for software and documentation. It has a new structure and all new content updates will be through C2000Ware and Software Development Kits (SDK) only. Note that C2000Ware, unlike controlSUITE, is versioned at the package level and thus results in a separate directory installation for each revision. C2000Ware can be downloaded from:

- http://www.ti.com/tool/C2000WARE

The SDKs are not included in the base C2000Ware download and needs to be downloaded and installed separately. Each SDK contains the development kit files and collateral related to the specific application solution. The SDKs also include a full version of the C2000Ware package. For additional information, see the *controlSUITE™ to C2000Ware Transition Guide*.

3.1 Driver Library (Driverlib)

The Driver Library (Driverlib) is a set of drivers for accessing the peripherals and device configuration registers. While Driverlib is not drivers in the pure operating system sense (does not have a common interface and does not connect into a global device driver), they do provide a software layer to facilitate a slightly higher level of programming. Driverlib provides a more readable and portable approach to peripheral register programming. This portability allows for an easier migration to future device families since the function calls can remain the same even though the control bits may change within and between registers.

3.2 Migrating Between IQ_Math and Native Floating-Point

The following steps must be taken to convert a project written in IQmath format to native floating point:

1. Select FLOAT_MATH in the IQmath header file. The header file converts all IQmath function calls to their floating-point equivalent.

2. Convert the floating-point number to an integer when writing a floating-point number into a device register. Likewise, when reading a value from a register, it needs to be converted to float. In both cases, this is done by multiplying the number by a conversion factor. For example, to convert a floating-point number to IQ15, multiply by 32768.0 as shown below:

```
#if MATH_TYPE == IQ_MATH
    PwmReg = (int16)_IQtoIQ15(Var1);
#else // MATH_TYPE is FLOAT_MATH
    PwmReg = (int16)(32768.0L*Var1);
#endif
```

To convert from an IQ15 value to a floating-point value, multiply by 1/32768.0 or 0.000030518.

3. Do the following to take advantage of the on-chip floating-point unit:

   a. Use Code Composer Studio with the C28x codegen tools version 19.6.0 or later.

   b. Set the compiler so that it can generate native C28x floating-point code. To do this, use the –v28 --float_support=fpu32 compiler switches. In Code Composer Studio, the float_support switch is under Compiler Options → Processor Options.

   c. Use the correct run-time support library for native 32-bit floating-point. It is recommended to include libc.a rather than directly including the RTS library. Note that libc.a is an index which will automatically select the correct .lib based on the project properties.

   d. Consider using the C28x FPU Fast RTS Library (C2000Ware → libraries → math → FPUfastRTS) to get a performance boost from math functions such as sin, cos, div, sqrt, and atan. The Fast RTS Library should be linked in before the normal run-time support library.

3.3 Embedded Application Binary Interface (EABI) Support

The F28002x is one of the first C2000 device families to migrate from Common Object File Format (COFF) to Embedded Application Binary Interface (EABI). EABI overcomes several limitations of COFF, which includes the symbolic debugging information not being capable of supporting C/C++, and the limit on the maximum number of sections and length of section names and source files. Note that EABI and COFF are not compatible and conversion between the two formats is not possible. The following is a brief summary of EABI differences compared to COFF.

- Direct initialization
  - Uninitialized data is zero by default in EABI.
  - Initialization of RW data is accomplished via linker-generated compressed copy tables in EABI.

- C++ language support
  - C++ inline function semantics: In COFF, inline functions are treated as static inline and this causes issues for functions that cannot be inlined or have static data. In EABI, inline functions without the 'static' qualifier have external linkage.
  - Better template instantiation: COFF uses a method called late template instantiation and EABI uses early template instantiation. Late template instantiation can run into issues with library code and can result in long link times. Early instantiation uses ELF COMDAT to guarantee templates are always instantiated properly and at most one version of each instantiation is present in the final executable.
  - Table-Driven Exception Handling (TDEH): Almost zero impact on code performance as opposed to COFF which uses setjmp/longjmp to implement C++ exceptions Features enabled by EABI.

- Features enabled by EABI
  - Location attribute: Specify the run-time address of a symbol in C-source code.
  - Noinit/persistent attribute: Specify if a symbol should not be initialized during C auto initialization.
  - Weak attribute: Weak symbol definitions are pre-empted by strong definitions. Weak symbol references are not required to be resolved at link time. Unresolved weak symbols resolve to 0.
  - External aliases: In COFF, the compiler will make A an alias to B if all calls to A can be replaced with B. A and B must be defined in the same file. In EABI, the compiler will make A an alias to B even if B is external.
- Calling convention
  - Scalar calling convention is identical between COFF and EABI.
  - Struct calling convention (EABI):
    - Single field structs are passed/returned by value corresponding to the underlying scalar types.
    - For FPU32, homogenous float structs with size less than 128 bits will be passed by value.
    - Passed in R0H-R3H, then by value on the stack.
    - Structs that are passed by value are also candidates for register allocation.
    - For FPU64, the same applies for 64-bit doubles (R0-R3).
- Double memory size
  - In EABI, double is 64-bit size while in COFF, double is still represented as 32-bit size.
  - C/C++ requires that double be able to represent integer types with at least 10 decimal digits, which effectively requires 64-bit double precision.

Table 1 summarizes the compiler-generated section names used by COFF and EABI.

Table 1. Section Names

Description	COFF	EABI
Read-Only Sections		
Const data	.econst	.const
Const data above 22-bits	.farconst	.farconst
Code	.text	.text
Pre-main constructors	.pinit	.init_array
Exception handling	N/A	.c28xabi.exidx/.c28xabi.extab
Read-Write Sections		
Uninitialized data	.ebss	.bss
Initialized data	N/A	.data
Uninitialized data above 22-bits	.farbss	.farbss
Initialized data above 22-bits	N/A	.fardata
Heap	.esysmem	.sysmem
Stack	.stack	.stack
CIO Buffer	.cio	.bss:cio

For more information about EABI and the migration process, see the following reference guides:

- *TMS320C28x Assembly Language Tools User's Guide*
- *TMS320C28x Optimizing C/C++ Compiler User's Guide*
- *C28x Embedded Application Binary Interface*
- C2000 Migration from COFF to EABI https://software-dl.ti.com/ccs/esd/documents/C2000_c28x_migration_from_coff_to_eabi.html

4 Package and Pinout

Both the F2803x and the F280025/F280025C/F280023/F280023C devices are available in an 80-pin low-profile quad flatpack (LQFP) package; however they are not pin-compatible. All other package options for the F2802x/03x and the F28002x devices are neither package nor pin-compatible. Any application being migrated from the F2802x/03x to the F28002x will require a new board layout to accommodate the changes in the pinout and/or the package. For more information, see the *TMS320F28002x Microcontrollers Data Sheet*.

5 Operating Frequency and Power Management

The F28002x devices have a maximum operating frequency of 100 MHz. By comparison, the F2802x devices have a maximum operating frequency of 60 MHz, 50 MHz, or 40 MHz depending upon the specific device family member, and the F2803x devices have a maximum operating frequency of 60 MHz.

The F28002x devices are powered by a 3.3 V supply and use an internal 1.2-V LDO Voltage Regulator (VREG) to supply the required 1.2 V to the core (VDD). The F28002x devices do not have a VREGENZ pin, and therefore the internal VREG is always enabled. The F2802x and F2803x devices are powered by a 3.3 V supply and have the option to power the 1.8 V core (VDD) externally or through the internal LDO Voltage Regulator (VREG). Unlike the F28002x devices, the F2802x and F2803x devices have a VREGENZ pin. The POR and BOR circuits on the F28002x and F2802x/03x devices are functionally the same. For details related to power management, see the *TMS320F28002x Microcontrollers Data Sheet*.

6 Power Sequencing

Before powering the F28002x devices, no voltage larger than 0.3 V above VDDIO can be applied to any digital pin, and no voltage larger than 0.3 V above VDDA can be applied to any analog pin (including VREFHI). The 3.3-V supplies VDDIO and VDDA should be powered up together and kept within 0.3 V of each other during functional operation. The VDD sequencing requirements are handled by the device. The F2802x and F2803x devices do not have specific power sequencing requirements. For information related to any electrical specifications, see the *TMS320F28002x Microcontrollers Data Sheet*.

7 Memory Map

The memory map between the F28002x and F2802x/03x are different and code must be rebuilt accordingly. This section covers the key differences. For specific details about the memory map, see the *TMS320F28002x Microcontrollers Data Sheet*.

7.1 Random Access Memory (RAM)

This section highlights the major differences in the RAM memory. The various memory block addresses and sizes differ between the F28002x devices and F2802x/03x devices, except for memory blocks M0 and M1. Additionally, memory blocks M0 and M1 on the F28002x are ECC protected.

- The F28002x has 12K x 16 words of RAM (ECC or parity-protected). This memory is divided into 10K x 16 words of dedicated (M0 – M1) and local shared (LS4 – LS7) RAM, and 2K x 16 words of global shared (GS0) RAM. By comparison, the F2802x has up to 6K x 16 words of RAM available and the F2803x has up to 10K x 16 words of RAM available.
- The F28002x GS0 RAM block can be used as a source and/or destination for each of the 6 DMA channels. DMA is not available on the F2802x/03x devices.

Table 2 summarizes the F28002x RAM memory blocks by size, address range, access, and protection/security.

Table 2. F28002x RAM Addresses and Memory Block Sizes

Memory	Size	Address Range	HIC Access	DMA Access	ECC/ Parity	Access Protection	Security
M0 RAM	1K x 16	0x0000 0000 - 0x0000 03FF	-	-	ECC	Yes	-
M1 RAM	1K x 16	0x0000 0400 - 0x0000 07FF	-	-	ECC	Yes	-
PIE RAM	512 x 16	0x0000 0D00 - 0x0000 0EFF	-	-	-	-	-
LS4 RAM	2K x 16	0x0000 A000 - 0x0000 A7FF	-	-	ECC	Yes	Yes
LS5 RAM	2K x 16	0x0000 A800 - 0x0000 AFFF	-	-	ECC	Yes	Yes
LS6 RAM	2K x 16	0x0000 B000 - 0x0000 B7FF	-	-	ECC	Yes	Yes
LS7 RAM	2K x 16	0x0000 B800 - 0x0000 BFFF	-	-	ECC	Yes	Yes
GS0 RAM	2K x 16	0x0000 C000 - 0x0000 C7FF	Yes	Yes	Parity	Yes	-
CAN A MSG	2K x 16	0x0004 9000 - 0x0004 97FF	-	-	Parity	-	-

7.2 Flash and OTP

This section highlights the major differences in the flash and OTP memory.

7.2.1 Size and Number of Sectors

The size and number of sectors has changed and code must be rebuilt accordingly. The exact flash size as well as sector configuration varies from device to device. For details, see Table 3. Note that code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress.

Table 3. Flash Sector Configuration by Device

	F280200	F28026 F28022 F28020	F28027 F28023 F28021	F28030	F28033 F28032 F28031	F28035 F28034	F280021	F280023 F280022	F280025 F280024
Sectors	2	4	4	4	8	8	4	8	16
Size	4K x 16	4K x 16	8K x 16	4K x 16	4K x 16	8K x 16	4K x 16	4K x 16	4K x 16
Total	8K x 16	16K x 16	32K x 16	16K x 16	32K x 16	64K x 16	16K x 16	32K x 16	64K x 16

7.2.2 Flash Parameters

The flash parameters differ between the F28002x and F2802x/03x. For details, see the *TMS320F28002x Microcontrollers Data Sheet*.

7.2.3 Entry Point into Flash

The flash entry point can be set to one of four pre-defined address options. Assigning the specific entry address to use is determined by the user-configurable boot definition table BOOTDEF registers Z1-OTP-BOOTDEF-HIGH and Z1-OTP-BOOTDEF-LOW. (Note that BOOTDEF registers Z2-OTP-BOOTDEF-HIGH and Z2-OTP-BOOTDEF-LOW is used when Z2-OTPBOOTPIN-CONFIG is configured). These registers are located in the DCSM OTP. During development and debug, the emulation equivalent BOOTDEF registers EMU-BOOTDEF-HIGH and EMU-BOOTDEF-LOW allow experimenting with different boot mode options without programming the OTP.

Table 4 summarizes the flash entry points.

Table 4. Flash Entry Points

Option	BOOTDEF Value	Flash Entry Point	Flash Sector
0 (default)	0x03	0x0008 0000	Bank0 Sector 0
1	0x23	0x0008 4000	Bank 0 Sector 4
2	0x43	0x0008 8000	Bank 0 Sector 8
3	0x63	0x0008 EFF0	Bank 0, End of Sector 14

7.2.4 Dual Code Security Module (DCSM) and Password Locations

The DCSM offers protection for two zones (zone-1 and zone-2), and is intended to block access and visibility to the various on-chip memory resources with the purpose of preventing duplication and reverse engineering of proprietary code. The options for both zones are identical, and each memory resource can be assigned to either zone. Either zone can protect each sector of flash individually, each LSx memory block individually, User OTP, and secure ROM.

Each zone is secured by its own 128-bit (four 32-bit words) user defined CSM password, which is stored in its dedicated OTP location based on a zone-specific link pointer. The user accessible CSMKEY registers are used to secure and unsecure the device, and a new or un-programmed device will be unlocked by default. Since the OTP cannot be erased, flexibility is provided by using a link pointer to select the location of the active zone region within the OTP block, allowing the user to make multiple modifications to the configuration up to thirty times. This is accomplished by exploiting the fact that each bit in the OTP can be programmed one bit at a time, and a "1" can be programmed to a "0", but not erased back to a "1". The most significant bit position in the link pointer that is programmed to a "0" defines the valid offset base address for the active zone region within the OTP block. This differs from the F2802x/03x devices where the 128-bit (eight 16-bit words) password is stored in the last eight locations in flash.

7.2.5 OTP

The entire OTP is reserved and unlike the F2802x/F2803x it is not available for user code/data (that is, no boot ROM entry point into the OTP). It consists of two 1K x 16 bit error correction code (ECC) protected sectors. The TI OTP sector is reserved for TI internal use only and it contains device calibration/trim data and settings used by the flash state machine for erase and program operations. The DCSM OTP (also known as User OTP) sector contains the user-configurable locations for security and boot process.

7.2.6 Flash Programming

The flash technology used with the F28002x devices is different than that of F2802x/03x devices. The F28002x flash offers faster erase and program operations. It also supports ECC for safety reasons. Since ECC is supported, F28002x flash API allows users to program in four modes – Fapi_DataOnly, Fapi_AutoEccGeneration, Fapi_DataAndEcc, and Fapi_EccOnly. Also, F28002x flash allows programming 128-bits at-a-time, whereas F2802x/03x allows programming only 16-bits at-a-time. F28002x flash API supports all these enhanced features and hence API prototypes are not compatible with that of F2802x/3x. For more details, see the *TMS320F28002x Flash API Reference Guide*.

7.3 Boot ROM

This section highlights the boot ROM enhancements of the F28002x device. The boot ROM has increased in size to 64K x 16 words on the F28002x from 8K x 16 words on the F2802x/03x. The F28002x boot ROM origin address starts at 0x003F 0000 and contains the contents of Table 5.

Table 5. Boot ROM Contents

ROM Signature	FPU32 Twiddle Tables	Boot Checksum	Version
AES Tables	Boot	Flash API Library (ROM)	Vector Table
IQmath Tables [1]	Interrupt Handlers	Flash API Table	
FPU32 Fast Tables	CPU Fast Data [2]	CRC Table	

(1) The memory location of the IQmath tables has changed to origin address 0x003F 1402 and a length of 0x166D words. Be sure to use the new addresses in your linker command file.

(2) To determine if this is available for your device, see the device-specific data manual. If not available, then this section is reserved.

In order to take advantage of the F28002x FPU, the boot ROM contains floating-point math tables which are used by the C28x FPU Fast RTS Library, located in C2000Ware at (C2000Ware → libraries → math → FPUfastRTS). For additional information about the boot ROM, see the *TMS320F28002x Microcontrollers Technical Reference Manual*.

7.3.1 Boot ROM Reserved RAM

On the F28002x devices the boot ROM reserved memory is the first 0x0126 words starting at 0x0002. This section contains the boot status, boot mode, MPOST status, and boot stack. Do not to allocate code or data to these memory locations until bootloading is complete.

7.3.2 Boot Mode Selection

The F28002x device is extremely flexible in its ability to use alternate, reduce, or completely eliminate boot mode selection pins by programming a BOOTPIN_CONFIG register, whereas the F2802x/03x boot mode pins are hard-coded and provides limited boot options and flexibility. Table 6 compares the two boot mode options which are available for the respective device families.

Table 6. Comparison of Boot Mode Options

	F2802x / F2803x	F28002x
Boot mode pins	GPIO37 and GPIO34 are boot pins for this device. Boot mode pins cannot be modified.	GPIO24 and GPIO32 are default boot mode pins for this device. Other GPIOs can be configured to use as boot mode pin by configuring Z1/Z2-OTP-BOOTPIN-CONFIG in stand-alone mode and EMU-BOOTPIN-CONFIG in emulation mode.
Bootloader options	**Stand-alone mode:** OTP_KEY and OTP_BMODE can be configured to select boot modes available below. **Emulation mode:** EMU_KEY and EMU_BMODE can be configured to select boot modes available below.	**Stand-alone mode:** Z1/Z2-OTP-BOOTDEF-LOW and Z1/Z2-OTP-BOOTDEF-HIGH can be configured to select boot modes available below. **Emulation mode:** EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH can be configured to select boot modes available below.

Table 6. Comparison of Boot Mode Options (continued)

	F2802x / F2803x			F28002x	
Bootloader options (cont)	Boot mode	No. of options available		Boot mode	No. of options available
	PARALLEL_BOOT	1		PARALLEL_BOOT	2
	SCI_BOOT	1		SCI_BOOT	5
	SPI_BOOT	1		SPI_BOOT	4
	I2C_BOOT	1		I2C_BOOT	3
	CAN_BOOT	Not available		CAN_BOOT	3
	RAM_BOOT	1		RAM_BOOT	1
	FLASH_BOOT	1		FLASH_BOOT	4
	OTP_BOOT	1		OTP_BOOT	Not available
	WAIT_BOOT	1		WAIT_BOOT	2

For additional information about the boot mode selection, see the *TMS320F28002x Microcontrollers Technical Reference Manual*.

7.3.3 Bootloaders

The F28002x allows for flexible pin selection when using a peripheral boot loader, such as SCI, SPI, I2C, or CAN. Unlike the F2802x/03x, the F28002x does not support the OTP boot mode.

8 Architectural Enhancements

The F28002x devices include many new architectural enhancements. This section briefly describes the architectural changes from F2802x/F2803x to F28002x devices. For more information, see the *TMS320F28002x Microcontrollers Technical Reference Manual*.

8.1 Clock Sources and Domains

There are numerous enhancement and changes to the clock sources and additional clock domains on the F28002x device. These major enhancements and changes include:

- Increase in the number of Peripheral Clock Gating Register to handle the additional and new peripherals
- INTOSC2 is the primary internal clock source and is the default system clock at reset
- INTOSC1 is a backup clock source which normally only clocks the watchdog timers and missing clock detection circuit (MCD)
- External Clock Source (XTAL) can be used as the main system and CAN bit clock source; frequency limits and timing requirements can be found in the *TMS320F28002x Microcontrollers Data Sheet*
- External Clock Output (XCLKOUT) can be connected to either GPIO16 or GPIO18, and the available clock sources are PLLSYSCLK, PLLRAWCLK, SYSCLK, INTOSC1, INTOSC2, and XTAL
- SYSPLL Integer Multiplier (IMULT) can be a value from 1 to 127
- PLLSYSCLK Divide Select (PLLSYSCLKDIV) can be a value of either 1 or an even value up to 126
- XCLKOUT Divide Select (XCLKOUTDIV) has /8 (default on reset) in addition to /1, /2, and /4

8.2 Dual-Clock Comparator (DCC) Module

The F28002x has a dual-clock comparator (DCC) module. The DCC is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

8.3 Watchdog Timer

The F28002x watchdog timer includes a WDCLK divider in addition to the watchdog prescaler and an optional "windowing" feature which is used to set a minimum delay between counter resets. Utilizing the WDCLK divider, the WDCLK derived from INTOSC1 can be divided by 2 to 4096 in powers of 2. This, along with the watchdog prescaler, provides a very wide range of timeout values for safety-critical applications. The WDCLK divider defaults to divide by 512 for backwards compatibility. On the F2802x/03x devices the WDCLK divider was fixed at divide by 512. The minimum window check feature complement the timeout mechanism in helping protect against error conditions that bypass large parts of the normal program flow but still include watchdog handling. A WDWCR register contains the desired minimum watchdog count. Any attempt to service the watchdog when WDCNTR is less than WDWCR will trigger a watchdog interrupt or reset. When WDCNTR is greater than or equal to WDWCR, the watchdog can be serviced normally. At reset, the window minimum is zero, which disables the windowing feature.

8.4 Peripheral Interrupt Expansion (PIE)

The F28002x PIE module multiplexes up to sixteen peripheral interrupts into each of the twelve CPU interrupt group lines, further expanding support for up to 192 peripheral interrupt signals. As a result, the interrupt vector table has expanded, and all 16-bit fields in the PIEIFRx and PIEIERx registers are being utilized. The interrupt vector table addressing is effectively split into two tables, where peripheral group interrupts 1 to 8 ranges from 0x0D40 to 0x0DFF and peripheral group interrupts 9 to 16 ranges from 0x0E00 to 0x0EBF. This provides backwards compatibility for the lower range peripheral interrupt vector addresses. The PIE vector table has been updated to accommodate the interrupts issued by the additional peripherals. By comparison, the F2802x/03x multiplexes up to eight peripheral interrupts into each of the twelve groups for up to 96 peripheral interrupt signals.

8.5 Lock Protection Registers

The F28002x devices utilize "LOCK" protection with several configuration registers to protect from spurious CPU writes. Once these associated LOCK register bits are set the respective locked registers can no longer be modified by software. Table 7 is a summary of the available LOCK registers. For more information, see the *TMS320F28002x Microcontrollers Technical Reference Manual*.

Table 7. LOCK Registers

CLKCFGLOCK1	CPUSYSLOCK2	SYNCSOCLOCK	RX_LOCK_CTRL
CPUSYSLOCK1	DMACHSRCSELLOCK	INPUTSELECTLOCK	TX_LOCK_CTRL

8.6 General-Purpose Input/Output (GPIO)

The F28002x allows up to twelve independent peripheral signals to be multiplexed on a single GPIO-enabled pin in addition to the CPU-controlled I/O capability. Each pin can be controlled by either a peripheral or the CPU. There are two I/O ports; Port A consists of GPIO0-GPIO31, and Port B consists of GPIO32-GPIO46 (where GPIO61/62/63 not bounded out). The analog signals on this device are multiplexed with digital inputs. These analog I/O (AIO) pins do not have digital output capability and they are assigned to a single port: Port H consists of GPIO224-GPIO247. For more information, see the *TMS320F28002x Microcontrollers Technical Reference Manual*.

> **NOTE:** GPIO18/X2 and GPIO19/X1 have different timings due to the load placed on them by the oscillator circuit. For information on using GPIO18/X2 and GPIO19/X1 as GPIOs, see the *TMS320F28002x Microcontrollers Data Sheet*.

8.7 External Interrupts

The F28002x has five external interrupts (two more than the F2802x/03x). Each external interrupt (XINT1-5) can be mapped to any GPIO pin via the Input X-BAR. Like the F2802x/03x, XINT1-3 has a free-running 16-bit counter which can measure the elapsed time between interrupts.

8.8   Crossbar (X-BAR)

The X-BARs provide a flexible means for interconnecting multiple inputs, outputs, and internal resources in various configurations. The F28002x device contains three X-BARs: the Input X-BAR, the Output X-BAR, and the ePWM X-BAR. Additionally, the F28002xC devices have a CLB X-BAR to allow access to the Configurable Logic Block (CLB).

- Input X-BAR – is used to route external GPIO signals into the device. It has access to every GPIO pin where each signal can be routed to any or multiple destinations which include the ADCs, eCAPs, ePWMs, Output X-BAR, and external interrupts. The F28002x Input X-BAR has sixteen inputs (INPUT1 through INPUT16) and any of the sixteen inputs can be selected as an external input to each of the eCAP modules.

> **NOTE:** This differs from the F2802x/03x devices which uses the GPIO multiplexer to select a specific dedicated input pin to access the eCAP module.

- Output X-BAR – is used to route various internal signals out of the device. It contains eight outputs that are routed to the GPIO structure, where each output has one or multiple assigned pin positions, which are labeled as OUTPUTXBARx. Additionally, the Output X-BAR can select a single signal or logically OR up to 32 signals.
- ePWM X-BAR – is used to route signals to the ePWM Digital Compare submodules of each ePWM module for actions such as trip zones and synchronizing. It contains eight outputs that are routed as TRIPx signals to each ePWM module. Likewise, the ePWM X-Bar can select a single signal or logically OR up to 32 signals.

8.9   Host Interface Controller (HIC)

The F28002x device has a Host Interface Controller (HIC) that allows an external host controller to directly access resources of the F28002x device using the ASRAM protocol.

8.10   Background CRC (BGCRC)

The F28002x Background CRC (BGCRC) module computes a CRC-32 on a configurable block of memory to help identify memory faults and corruption. This is accomplished by fetching the specified block of memory during idle cycles when the CPU is not accessing the memory block. The calculated CRC-32 value is compared against a golden CRC-32 value to indicate a pass or fail.

9   Peripherals

New peripherals have been added and most of the existing peripherals have been updated. The Control Law Accelerator is not available on the F28002x devices. This section briefly describes the additions and changes from F2802x/F2803x to F28002x devices. For an overview of the available peripherals, see the *C2000 Real-Time Control Peripherals Reference Guide*.

9.1   New Peripherals

The F28002x devices include new peripherals that are not available on the F2802x/F2803x devices. For more information, see the *TMS320F28002x Microcontrollers Technical Reference Manual*.

9.1.1   Direct Memory Access (DMA)

The direct memory access (DMA) module is an event-based machine that provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, effectively freeing up the CPU for other functions. Using the DMA is ideal when an application requires a significant amount of time spent moving large amounts of data. Additionally, the DMA is capable of orthogonally rearranging the data as it is transferred into blocks, "ping-pong" buffering, and binning for optimal CPU processing.

A DMA transfer is started by a peripheral or software trigger. There are six independent DMA channels, where each channel can be configured individually and each DMA channel has its own unique PIE interrupt for CPU servicing. All six DMA channels operate the same way, except channel 1 can be configured at a higher priority over the other five channels. At its most basic level the DMA is a state machine consisting of two nested loops and tightly coupled address control logic which gives the DMA the capability to rearrange the blocks of data during the transfer for post processing. Major features of the DMA are:

- Six channels with independent PIE interrupts
- Each DMA channel can be triggered from multiple peripheral trigger sources independently
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: 3 cycles/word without arbitration

9.1.2 Analog Subsystem Interconnect

The F28002x utilizes an analog subsystem interconnect which enables a very flexible pin usage, allowing for smaller device packages. The CMPSS inputs and digital inputs are multiplexed with the ADC inputs. This type of interconnect permits a single pin to route a signal to multiple analog modules. The analog pins are organized into analog groups around a CMPSS module, and the routing is defined in an analog pin and internal connections table.

9.1.3 Comparator Subsystem (CMPSS)

The F28002x CMPSS provides substantial enhancements over the simple analog comparator with the integrated 10-bit reference digital-to-analog (DAC) circuits found on the F2802x/03x devices. There are four CMPSS modules available on the F28002x devices. Each module contains two comparators, two reference 12-bit DACs, two digital filters and one ramp generator. The CMPSS modules are useful for implementing peak current mode control and voltage trip monitoring, which are used in applications such as switched-mode power control and power factor correction. The module is designed around a pair of analog comparators which generates a digital output indicating if the voltage on the positive input is greater than the voltage on the negative input. The positive input to the comparator is always driven from an external pin. The negative input can be driven by either an external pin or an internal programmable 12-bit DAC as a reference voltage. Values written to the DAC can take effect immediately or be synchronized with ePWM events. A falling-ramp generator is available to control the internal DAC reference value for one comparator in the module, which enables peak current mode control in digital power applications. Each comparator output is fed through a programmable digital filter to prevent electrical switching noise from causing spurious trip signals. The output of the CMPSS generates trip signals to the ePWM event trigger submodule and GPIO structure. Additionally, the CMPSS features PWM blanking capability to clear-and-reset existing or imminent trip conditions near the ePWM cycle boundaries. Also, by using the analog subsystem interconnect scheme the CMPSS comparator positive and negative input signals are independently selectable.

9.1.4 Power Management Bus (PMBus)

The PMBus module provides an interface for communicating between the MCU and other devices that are compliant with the System Management Interface (SMI) specification. PMBus is an open-standard digital power management protocol that enables communication between components of a power system.

9.1.5 Fast Serial Interface (FSI)

The FSI module is a highly reliable high-speed serial communication peripheral capable of operating at dual data rate providing 200 Mbps transfer using a 50 MHz clock. The FSI consists of independent transmitter and receiver cores that are configured and operated independently. FSI is a point-to-point communication protocol operating in a single-master/single-slave configuration. With this high-speed data rate and low channel count, the FSI can be used to increase the amount of information transmitted and reduce the costs to communicate over an isolation barrier.

9.2 Control Law Accelerator (CLA)

The F28002x devices do not have a CLA. (A Type-0 CLA is available on the F28035 and F28033 devices).

9.3 Control Peripherals

This section describes the changes and additions to the F28002x device control peripherals. For more information, see the following reference guides:

- *TMS320F28002x Microcontrollers Technical Reference Manual*
- *C2000 Real-Time Control Peripherals Reference Guide*

9.3.1 Enhanced Pulse Width Modulator (ePWM)

The ePWM module on the F28002x devices remains functionally the same, and includes many enhancements. As a result, additional registers have been added, and the ePWM address space has been remapped for better alignment and usage. These enhancements include:

- Counter Compare Sub-module – added counter compares CMPC and CMPD to allow Interrupts and ADC SOC events to be generated.
- Action Qualifier Sub-module – added shadow loading of AQCTLA and AQCTLB registers to enable changes that must occur at the end of a period even when the phase changes. Additionally, shadow to active load on SYNC and Global Reload for the Action Qualifier Sub-module is supported.
- Dead-Band Sub-module – added high resolution capability to dead-band RED and FED in half-cycle clocking mode. Includes features to enable both RED and FED on either PWM outputs. Increased dead-band with 14-bit counters. Dead-band/dead-band high-resolution registers are shadowed to allow dynamic configuration changes.
- Event Trigger Sub-module – enhanced pre-scaling logic to issue interrupt requests and ADC SOC expanded up to every 15 events, to allow software initialization of event counters on SYNC event.
- Trip-Zone Sub-module – independent flags have been added to reflect the trip status for each of the TZ sources. Also, changes have been made to the trip zone module to support certain power converter switching techniques, such as valley switching. Trip-zone TZ4 is sourced from an inverted EQEPxERR signal, TZ5 is connected to the system clock fail logic, and TZ6 is sourced from the EMUSTOP output from the CPU.
- Digital Compare Sub-module – the Digital Compare Trip Select logic [DCTRIPSEL] has up to 12 external trip sources that are selected by the Input X-BAR logic. This is in addition to an ability to OR all of them, for up to 14 external and internal sources which are used to create the respective DCxEVTs. Blanking window filter register width is 16 bits, and the DCCAP functionality has been enhanced to provide more programming flexibility.
- High-Resolution PWM – includes the ability to enable high-resolution period and duty cycle control on both ePWMxA and ePWMxB outputs.
- Simultaneous Writes to TBPRD and CMPx Registers – allows writes to TBPRD, CMPA:CMPAHR, CMPB:CMPBHR, CMPC, and CMPD of any ePWM module to be tied to any other ePWM module, and also allows all ePWM modules to be tied to a particular ePWM module, if desired.
- Shadow to Active Load on SYNC of TBPRD and CMP Registers – supports simultaneous writes of TBPRD and CMPA/B/C/D registers.
- Delayed Trip Functionality – changes have been added to achieve dead-band insertion capabilities to support delayed trip functionality, which is needed for peak current mode control type applications. This has been accomplished by allowing comparator events to go into the Action Qualifier Submodule as a trigger event (Events T1 and T2). If comparator T1/T2 events are used to modify the PWM, changes to the PWM waveform will not take place immediately, but instead they will synchronize to the next TBCLK.
- One Shot and Global Reload of Registers – allows one shot and global reload capability from shadow to active registers. This avoids partial reload conditions in, for example, multi-phase applications. It also allows programmable pre-scale of shadow to active reload events. Global Load can simplify ePWM software by removing interrupts and ensuring that all registers are loaded at the same time.

- PWM SYNC Related Enhancements – allows PWM SYNCOUT generation based on CMPC and CMPD events. These events can also be used for PWMSYNC pulse selection.

9.3.2 Enhanced Capture Module (eCAP)

The F28002x devices have three eCAP modules and one has high resolution capture (HRCAP) capability. Enhancements to the eCAP module include:

- Input Multiplexer – selects one of 128 signals, which can be from internal or external sources. Any GPIO pin can be used as an input source via the Input X-BAR. Input source is selected by INPUTSEL bit fields in the ECCTL0 register.

  > **NOTE:** The F2802x/03x devices use the GPIO multiplexer to select a specific dedicated input pin to access the eCAP module.

- Event Filter Reset Bit – CTRFILTRESET bit field in the ECCTL2 register clears the event filter, modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo Counter Status Bits – MODCNTRSTS bit fields in the ECCTL2 register indicate which capture register will be loaded next. It was not possible to know current state of modulo counter with the F2802x/03x eCAP modules.
- DMA Trigger Source – CEVT[1-4] can be configured as the source for eCAPxDMA.
- EALLOW Protection – added to critical registers. To maintain software compatibility with F2802x/03x devices, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.
- ECAPxSYNCINSEL Register – added for each eCAP to select an external SYNCIN. Each eCAP module can have a separate SYNCIN signal.
- High Resolution Capture (HRCAP) – extension of eCAP (i.e. unified) rather than a separate module. All eCAP hardware is accessible when using the HRCAP features. Enhancements include:
  - Simplified calibration scheme and HRCAP is always functional without the need to perform offline calibration.
  - Calibration is always running in the background which drastically reduced the software overhead needed to calibrate.
  - Reduced software overhead to compute fractional bits.
  - Fractional and integer portions are packed into 32 bits.
  - Support for one-shot capture

9.3.3 Enhanced Quadrature Encode Pulse Module (eQEP)

The F28002x devices have two eQEP modules. The F2803x devices have one eQEP module and the eQEP module is not available on the F2802x devices. Enhancements to the F28002x eQEP module include:

- QEP Mode Adapter (QMA) – the QMA evaluates transitions on the external EQEPA and EQEPB signal lines and generates direction and clock signals for supporting industrial drive applications. To use the QMA the eQEP module needs to be configured in the Direction-Count mode.
- Latching Position Counter – on ADCSOCA/ADCSOCB event from ePWM module.
- SinCos – support for decoding signals from SinCos transducers.

9.4 Analog Peripherals

This section describes the changes and additions to the F28002x device analog peripherals. For more information, see the following reference guides:

- *TMS320F28002x Microcontrollers Technical Reference Manual*
- *C2000 Real-Time Control Peripherals Reference Guide*

9.4.1 Analog-to-Digital Converter (ADC)

Unlike the ADC found on the F2802x/03x where a single ADC has two sample-and-hold (S/H) circuits, the F28002x utilizes two independent ADCs and each has a single S/H circuit. This allows the F28002x to efficiently manage multiple analog signals for enhanced overall system throughput. By using multiple ADC modules, simultaneous sampling or independent operation can be achieved. The ADC module is implemented using a successive approximation type ADC with a resolution of 12-bits and it provides a throughput of 3.45 MSPS.

Like the F2802x/03x, ADC triggering and conversion sequencing is managed by a series of start-of-conversion (SOCx) configuration registers. However, the F28002x adds burst priority mode, in addition to the round robin and high priority modes. Burst mode allows a single trigger to convert one or more than one SOCx sequentially at a time. This mode uses a separate Burst Control register to select the burst size and trigger source. Also, the F28002x has four flexible PIE interrupts rather than nine found on the F2802x/03x.

To further enhance the capabilities of the F28002x ADC, each ADC module incorporates four post-processing blocks (PPB), and each PPB can be linked to any of the ADC result registers. The PPBs can be used for offset correction, calculating an error from a set-point, detecting a limit and zero-crossing, and capturing a trigger-to-sample delay:

- Offset correction can simultaneously remove an offset associated with an ADCIN channel that was possibly caused by external sensors or signal sources with zero-overhead, thereby saving processor cycles.
- Error calculation can automatically subtract out a computed error from a set-point or expected result register value, reducing the sample to output latency and software overhead.
- Limit and zero-crossing detection automatically performs a check against a high/low limit or zero-crossing and can generate a trip to the ePWM and/or generate an interrupt. This lowers the sample to ePWM latency and reduces software overhead. Also, it can trip the ePWM based on an out-of-range ADC conversion without any CPU intervention, which is useful for safety conscious applications.
- Sample delay capture records the delay between when the SOCx is triggered and when it begins to be sampled. This can enable software techniques to be used for reducing the delay error.

9.5 Communication Peripherals

This section describes the changes and additions to the F28002x device communication peripherals. For more information, see the following reference guides:

- *TMS320F28002x Microcontrollers Technical Reference Manual*
- *C2000 Real-Time Control Peripherals Reference Guide*

9.5.1 SPI

The F28002x SPI includes the following enhancements:

- Transmit and receive FIFOs have increased from 4-levels to 16-levels
- High-speed mode
- Delayed transmit control
- DMA support

Also included is the STEINV inversion bit for digital audio interface receive mode on devices with two SPI modules (which is available on F2803x, but not F2802x). The F28002x has two SPI modules, whereas the F2803x has up to two SPI modules depending on the device package and the F2802x has only one SPI module.

9.5.2 SCI

The F28002x SCI module remains functionally the same as the F2802x/03x except transmit and receive FIFOs have increased from 4-levels to 16-levels.

9.5.3 LIN

The F28002x has two LIN modules that are compliant to the LIN 2.1 protocol specifications. The F2803x has one LIN module that is compliant to LIN 1.3 and 2.0 protocol specifications. The LIN module is not available on the F2802x.

9.5.4 I2C

The F28002x has two I2C modules. Transmit and receive FIFOs have increased from 4-levels to 16-levels, and the bug related to the timing of the XRDY transmit interrupt has been fixed. The F2802x/03x has one I2C module.

9.5.5 CAN

The F28002x DCAN has a different register structure compared to F2802x/03x eCAN and therefore code written for one module cannot be migrated to another.

The following features are available in F28002x DCAN and are not available in F2802x/3x eCAN:

- Parity check mechanism for all RAM modules
- Automatic Retransmission (upon loss of arbitration) can be disabled
- Silent mode (Node listens passively)
- Mailbox RAM may be combined to form FIFO buffers
- Data can be monitored on CANTX pin in self-test mode

The following are the features that are available in F2802x/03x eCAN and are not available in F28002x DCAN:

- Timestamping of messages
- Transmission priority configuration (TPL)
- Data-byte order configuration (DBO)

For more information, see the following application report:

- *Programming Examples and Debug Strategies for the DCAN Module.*

10 Configurable Logic Block (CLB)

The F28002xC devices are specially enabled device variants that have access to the Configurable Logic Block (CLB). The CLB is a collection of configurable blocks that can be inter-connected using software to implement custom digital logic functions. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals, such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as simple PWM generators, or to implement custom serial data exchange protocols.

11 Embedded Real-Time Analysis and Diagnostic (ERAD)

A standard C28x CPU includes two analysis units, where the first analysis unit counts events or monitors address buses, and the second analysis unit monitors address and data buses. The two analysis units can be configured for hardware breakpoints or hardware watch points, and additionally the first analysis unit can be configured as a benchmark counter or event counter. The F28002x expands these capabilities with the Embedded Real-Time Analysis and Diagnostic (ERAD) module. This module is external to the C28x CPU and provides additional hardware breakpoints, hardware watch points, and counters for profiling, as well as other advanced features. With the ERAD it is now possible to have up to ten hardware breakpoints.

Typically, the ERAD module is used by the debug software. However, the user application software can also be configured to use the ERAD module. This is especially useful for real-time systems where it is not possible to connect a debug probe for intrusive debug. In this case, the user software can control the ERAD module for non-intrusive debug and profiling of the system.

For more information, see the *TMS320F28002x Microcontrollers Technical Reference Manual*.

12 Emulation – JTAG Port

The F28002x devices support two JTAG modes:

- IEEE 1149.1 Standard JTAG mode using TCK, TMS, TDI and TDO pins; note that there is no TRSTn pin on F28002x devices
- IEEE 1149.7 Compact JTAG (cJTAG) using TCK and TMS pins; in this mode the TMS pin is bi-directional and carries TDI, TMS, and TDO information

For more information, see the *TMS320F28002x Microcontrollers Data Sheet*.

13 Silicon Errata

For the most current known exceptions to the functional specifications (advisories) and usage notes (where the device's behavior may not match presumed or documented behavior), see the following document:

- *TMS320F28002x MCUs Silicon Errata*

14 Device Comparison Summary

In this section, Table 8 provides a general feature comparison between the F28002x, F2803x, and the F2802x device families. For specific details about device features, maximum clock frequency, memory sizes, and peripheral availability and quantity, see the device-specific data sheet.

Table 8. Device Comparison Matrix

	F28002x	F2803x	F2802x
Clock	100 MHz	60 MHz	60 MHz
FPU	√ [1]	-	-
TMU	√	-	-
FINTDIV	√	-	-
VCRC	√	-	-
CLA	-	√ (Type 0)	-
6-Channel DMA	√ (Type 0)	-	-
Flash / RAM	64K x 16 / 12K x 16	64K x 16 / 10K x 16	32K x 16 / 6K x 16
32-bit CPU Timers	√	√	√
Watchdog Timer	√	√	√
On-chip Oscillators	√	√	√
ADC	Two 12-bit (Type 5)	One 12-bit (Type 3)	One 12-bit (Type 3)
CMPSS w/ 2 DACs	√	-	-
CMP w/DAC	-	√	√
ePWM / HRPWM	√ / √ (Type 4)	√ / √ (Type 1)	√ / √ (Type 1)
eCAP / HRCAP	√ / √ (Type 1)	√ / √ (Type 0)	√ / - (Type 0)
eQEP	√ (Type 1)	√ (Type 0)	-
HIC	√	-	-
CAN [2]	√ (DCAN)	√ (eCAN)	√ (eCAN)
I2C	√ (Type 1)	√ (Type 0)	√ (Type 0)
SCI	√	√	√
SPI	√ (Type 2)	√ (Type 1)	√ (Type 1)
LIN	√ (Type 1)	√ (Type 0)	-
PMBus	√	-	-
FSI	√	-	-
X-BARs	√	-	-

Table 8. Device Comparison Matrix (continued)

	F28002x	F2803x	F2802x
CLB	√	-	-
ERAD	√	-	-

(1) √ indicates available. For details, check the specific device.

(2) DCAN and eCAN are not software compatible.

For more detailed device information, see the following data sheets:

- *TMS320F28002x Microcontrollers Data Sheet*
- *TMS320F2803x Microcontrollers Data Sheet*
- *TMS320F2802x Microcontrollers Data Sheet*

15 References

- Texas Instruments: *TMS320F28002x Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F28002x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28002x MCUs Silicon Errata*
- Texas Instruments: *TMS320F2803x Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F2803x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F2803x MCUs Silicon Errata*
- Texas Instruments: *TMS320F2802x Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F2802x,TMS320F2802xx Technical Reference Manual*
- Texas Instruments: *TMS320F2802x, TMS320F2802xx MCUs Silicon Errata*
- Texas Instruments: *TMS320C28x CPU and Instruction Set Reference Guide*
- Texas Instruments: *TMS320C28x Extended Instruction Sets Technical Reference Manual*
- Texas Instruments: *C2000 Real-Time Control Peripherals Reference Guide*
- Texas Instruments: *TMS320C28x Assembly Language Tools User's Guide*
- Texas Instruments: *TMS320C28x Optimizing C/C++ Compiler User's Guide*
- Texas Instruments: *controlSUITE™ to C2000Ware Transition Guide*
- http://www.ti.com/tool/C2000WARE
- Texas Instruments: *C28x Embedded Application Binary Interface*
- C2000 Migration from COFF to EABI https://software-dl.ti.com/ccs/esd/documents/C2000_c28x_migration_from_coff_to_eabi.html
- Texas Instruments: *TMS320F28002x Flash API Reference Guide*
- Texas Instruments: *Programming Examples and Debug Strategies for the DCAN Module*