Application Note

Hardware Design Guide for AM65x Devices

TEXAS INSTRUMENTS

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Trademarks

1 Introduction

The Hardware Design Guide for AM65x family of Devices Application Report provides a starting point for the engineers designing with AM65x processors. It provides an overview of the flow, design efforts and highlights important areas that must be addressed. Note that this document does not contain all the information needed to complete the system design. In many cases, it refers to the device-specific data manual or to various other user guides as sources for specific information.

The document is organized in a sequential manner. It starts from decisions that must be made during the initial planning stages of the design, through the selection of key devices, electrical, and thermal requirements. For ensuring design success, issues discussed in each of the section should be resolved before moving to the next section.

Note

This guide may not cover every aspect of the system design.

Note

The AM65x device has capabilities to help system designers address safety requirements.

This guide is focused on non-safety applications.

1.1 Before Getting Started

The AM65x processors includes wide variety of capabilities, not all of which will be used in every design. Consequently, the requirements for different designs using the same device can vary widely depending on the target application. Designers must understand the requirements before determining the details of the design. In addition, the design may require additional circuitry to operate correctly in the target environment. For the selected device and determine the following, see latest device-specific collaterals on TI.com like the data sheet, Errata, TRM and EVM User's guides:

- What are the expected environmental conditions for the device operation, target boot mode, storage type and interfaces used
- How much processing will each of the cores in the selected device be performing
- What is the DDR memory type, speed and interface that will be used
- Peripherals attached to the processor

1.2 Device (Processor) Selection

Selection of device is the most important step during the system design process. For selecting the device variant, device density, features, package (ACD), and speed grade that is applicable, see the *Functional Block Diagram* and *Device Comparison* section in device-specific data sheet.

1.3 Technical Documentation

A number of documents relevant to the selected device are provided on the product folder page. Read through relevant documents before the start of design.

1.4 Design Documentation

Throughout this guide, TI recommends generating a design document periodically. Generating and storing this information provides you with the foundation for the documentation package, and this design document is needed when seeking external review support.

2 System Block Diagram

A detailed System Block Diagram, covering all the functional blocks and required interfaces is key to a successful design.

2.1 Creating the System Block Diagram

The first step during the system design is to create a detailed System Block Diagram. The System Block Diagram includes all major functional blocks, associated devices, interfaces and illustrates the I/Os (ports) used for interconnecting the devices.

The following is a collection of resources to support the System Block Diagram creation process:

- The TMDX654GPEVM (AM65x evaluation module (EVM)), TMDX654IDKEVM (AM65x industrial development kit (IDK)) and any other available EVMs are a good source to start with the design.
- The TI.com links referred to below provide Device Functional Block Diagrams, Device device-specific Data sheet, User's Guide, Errata, application notes, design considerations, and other related information for various applications. Design and development section include EVM information, Design tools, simulation models and software. As part of support and training, links to commonly applicable E2E threads are available.
  - AM6526 Product Folder
  - AM6528 Product Folder
  - AM6546 Product Folder
  - AM6548 Product Folder

2.2 Selecting the Boot Mode

The System Block Diagram should indicate the interface used for booting.

The AM65x device contains multiple peripheral interfaces that support boot mode. Examples include: QSPI, OSPI, PCIe, GPMC NOR, Hyperflash, Ethernet, USB, eMMC, MMCSD, I2C, SPI and UART. The AM65x device supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, the ROM moves on to the backup mode.

The boot mode pins and the associated resistor configurations provide inputs on the boot mode setting to be used by the ROM code for boot. These pins are sampled at power-on-reset, and must be properly set up before releasing (deassertion) the reset. The BOOTMODE[06:00] pins are used to select the primary and backup interfaces used for booting. Additionally, each boot mode has different configuration options, controlled by the other boot mode pins (BOOTMODE[18:07] and MCU_BOOTMODE[09:00]).

Key considerations for boot mode configuration:

- TI recommends including provision to configure boot modes used during development, such as UART boot or No-boot mode for JTAG debug.
- Boot pins have other functions after reset. Ensure the board design takes this into account when choosing pullup/pulldown resistors for the boot pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the device is reset (indicated by the PORz_OUT pin) to enable it to boot properly.
- The functionality of some boot mode pins are reserved. These pins should not be left floating and must be terminated (pullup or pulldown). For details regarding termination of reserved boot mode pins, see the *Boot Mode Pins* section of the *Initialization* chapter of the device-specific TRM.

For details regarding boot modes, see the *Initialization* chapter of the device-specific TRM.

Note

It is the user responsibility to set the boot mode pins (via pullups or pulldowns, and optionally jumpers/ switches) depending on the desired boot scenario.

2.3 Confirming Pin Multiplexing Compatibility

The processor contains a number of peripheral interfaces. To optimize size, pin count, package cost while maintaining maximum functionality, many of the device pads (pins) can multiplex up to eight signal functions. Thus, not all peripheral interface instances can be used simultaneously.

Texas Instruments has developed SysConfig-PinMux Tool that helps a system designer select the appropriate function using pin-multiplexing configuration too for their AM65x based system design.

Note

The pinmux configuration generated using SysConfig-PinMux Tool for the design should be saved along with other design documentation.

3 Power Supply

After completing the device selection and system block diagram, next design process is to determine the power supply needs for the selected processor.

3.1 Power (Supply) Rails

For the full list of processor power rails and recommended operating range, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details about select power rails.

3.1.1 Internal LDOs for IO groups

The processor includes seventeen internal LDOs, with the output of each connected to a pin (named "CAP_VDD*") on the processor. A capacitor must be connected to each of these LDO output pins. For guidance on the capacitor selection and connection, see the *Power Supply* section in the *Signal Descriptions* chapter of the device-specific data sheet.

3.1.2 Dual-Voltage LVCMOS I/Os

The processor includes twelve dual-voltage I/O domains (VDDSHV[0:8] and VDDSHV[0:2]_WKUP), where each domain provides power to a fixed set of I/Os. Each I/O power domain can be configured for 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of I/Os powered by the respective I/O power domain.

Each of these supplies has a corresponding I/O bias supply (VDDS[0:8] and VDDS[0:2]_WKUP). If any of the VDDSHV[0:8] or VDDSHV[0:2]_WKUP are configured for 3.3-V operation, the corresponding VDDS[0:8] or VDDSHV[0:2]_WKUP should be sourced from the internal I/O Bias LDO (CAP_VDDA_1P8_IOLDO[0:1] and CAP_VDDA_1P8_IOLDO_WKUP). When any of the VDDSHV[0:8] or VDDSHV[0:2]_WKUP are configured for 1.8-V operation, both VDDS[0:8] and VDDSHV[0:8] or VDDS[0:2]_WKUP and VDDSHV[0:2]_WKUP should be supplied from the same source.

For more information, see the *External Capacitors* section in the *Applications, Implementation, and Layout* chapter of the device-specific data sheet.

3.1.3 Dual-Voltage Switching SDIO I/Os

The processor includes one integrated 1.8-V SDIO LDO to support SD card I/O voltage switching from card initialization to high-speed data modes. Only one MMCSD port (selectable through the MCU_BOOTMODE09 pin) can be connected to the SDIO LDO in a given system.

For information about how to connect and configure the SDIO LDO, see:

- The *External Capacitors* section in the *Applications, Implementation, and Layout* chapter of the device-specific data sheet.
- The *Power Supply* section in the *Signal Descriptions* chapter of the device-specific data sheet.

3.2 Determining System Power Requirements

The maximum and minimum current requirements for each of these voltage rails are not available in the device-specific data sheet. These requirements are highly application-dependent and must be calculated for a specific use case.

3.3 Power Supply Filters

The processor contains multiple analog supply pins that provide power to sensitive analog circuitry such as PLLs, DLLs, and SERDES buffers and terminations. These must be attached to filtered supply sources.

3.4 Power Supply Decoupling and Bulk Capacitors

To properly decouple the supply planes from system noise, decoupling and bulk capacitors are required. For general information about decoupling capacitors, see the device-specific data sheet.

For guidance on optimizing the selection and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis*.

3.5 Power Supply Sequencing

A detailed diagram of the power supply sequencing (Power-Up/Power-Down) for the processor can be found in the device-specific data sheet. All power supplies associated with the processor should allow for controlled sequencing using on-board logic when using discrete power solution or a PMIC based power supply.

4 Clocking

The next design step is proper clocking, and providing appropriate clocks to all connected devices in the system. These clocks can be generated by pairing external crystals with an internal oscillator or they can be generated externally by a clock generator or oscillator. This section describes the clocks available in the processor and the requirements for these clocks.

4.1 System Clock Inputs

The processor clock inputs and recommended oscillator connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet. WKUP_OSC0 is a required clock for proper operation of the processor.

OSC1 and WKUP_LFOSC are optional, depending on the system requirements.

4.2 Single-Ended Clock Sources

The WKUP_OSC0, WKUP_LFOSC0 and OSC1 internal oscillators can be sourced from a crystal or an LVCMOS square-wave digital clock source. For more details, see the *Input Clocks / Oscillators* section in the *Specifications* chapter of the device-specific data sheet.

Note

Be sure to terminate the XO pin as per the data sheet recommendation when using an external clock.

4.3 Unused Clock Inputs

For guidance on the recommended connections for unused clock inputs, see the *Connections for Unused Pins* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

5 JTAG

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. Although JTAG is not required for operation, TI strongly recommends that a JTAG connection be included in the designs.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates, see the device-specific TRM.

5.1.2 System Implementation of JTAG / Emulation

The JTAG and Emulation pins on this processor are split across different power domains. The TDI, TDO, and TMS I/Os are powered by the VDDSHV0 domain. The TCK, TRSTz, EMU0, and EMU1 I/Os are powered by the VDDSHV0_WKUP domain. For proper operation of most emulators, these signals must be operating at the same voltage level. VDDSHV0 and VDDSHV0_WKUP can be configured either 1.8 V or 3.3 V.

For most other system-level implementation details, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 JTAG Termination

For terminating the JTAG interface signal, see the *Connections for Unused Pins* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

6 Device Configurations and Initialization

When the voltage rails and the required clocks are present and stable, the processor reset may be deasserted (released) to start the processor initialization.

6.1 Device Reset

The processor can be reset in several ways. The methods are described in detail in the device-specific data sheet and TRM.

The device includes four external reset pins (MCU_PORz, MCU_RESETz, PORz, and RESETz) and four reset status pins (MCU_PORz_OUT, MCU_RESETSTATz, PORz_OUT, and RESETSTATz). Be sure to provide the terminations recommended in the data sheet.

Additional reset modes are available through internal registers and emulation.

The device integrates an on-chip Power-on-Reset (POR) generator. Additionally, this device supports an external POR generation through a PORz and MCU_PORz input pin. The MCU_BYPASS_POR pin selects the POR source. When the MCU_BYPASS_POR pin is set high at power-up, on-chip POR generation will be completely bypassed and the external POR used. When it is low, the POR is generated internally. However, the four external reset inputs must all be pulled high to enable this internal POR generation.

Note that TI recommends implementing RESET logic using AND gate for on-board Media and Data Storage devices and other peripherals as applicable. One of the AND gate input shall be controlled by processor GPIO pin with provision to isolate. Other AND gate input shall be the Main Domain POR status output (PORz_OUT) Signal. Ensure the reset outputs are terminated as per the device recommendations.

The 3.3 V power source for the SD Card needs to be routed through an external power switch that can be controlled. This controlled power switch is required to reset the SD Card since cycling power to the card is the only way to reset the card back to its default state.

For more information, see the *TMDX654GPEVM (AM65x evaluation module (EVM))* and *TMDX654IDKEVM (AM65x industrial development kit (IDK))* schematics.

6.2 Boot Modes

For more details about the processor boot mode options, see Section 2.2.

Boot modes and certain device configuration selections are latched at the rising edge of MCU_PORz and PORz. The configuration and boot mode inputs are multiplexed with GPIO pins or pins with other functions. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for their primary function. The PORZ_OUT pin indicates latching of boot mode configuration.

6.3 Watchdog Timer

Consider using external or internal watchdog timer based on the application requirement.

7 Peripherals

This section covers the device peripherals and modules, and is intended to be used in addition to the information provided in the device-specific data sheet, TRM, and relevant application reports. The three types of documents should be used as follows:

- Data Sheet: AC Timings, Used pin guidance
- TRM: Functional Description, Programming Guide, Register offsets
- Application Reports: System-level understanding and issues

7.1 Selecting Peripherals Across Functional Domains

The processor is partitioned into three functional domains, each containing specific processing cores and peripherals:

- MAIN domain
- Microcontroller (MCU) domain
- Wake-up (WKUP) domain

For most use cases, peripherals from any of the domain can be used. All peripherals, regardless of their domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access all peripherals in the MCU and WKUP domains.

7.2 Ethernet Interface

AM65x provides an Integrated Ethernet switch. An Integrated Ethernet switch supporting one external Ethernet ports RMII (10/100) or RGMII (10/100/1000) using CPSW2G subsystem. For configuring RMII interface, see the *MCU_CPSW0 RMII Interface* section of the device-specific TRM for the recommended configuration.

For more details on the Ethernet interface, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.3 Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU-ICSSG)

AM65x provides three instances of PRU-ICSSG subsystems and supports Ethernet, UART0, eCAP0, PWM, IEP0 and IEP1 peripheral modules.

Each PRU_ICSSG contains 2 x Ethernet ports (MII/ RGMII). SGMII mode is supported only for PRU_ICSSG2 instance.

For more details, see the *Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG) (SR1.0)* and *Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG) (SR2.0)* sections in the *Processors and Accelerators* chapter of the device-specific TRM.

7.4 Universal Serial Bus (USB) Subsystem

AM65x processor provides two USB subsystems, one SuperSpeed (USB3.0) and one HighSpeed (USB2.0) subsystems with integrated PHY. These ports can be independently configurable as USB host, USB peripheral, or USB DRD.

Follow USB VBUS Design Guidelines for scaling the VBUS voltage connected to the processor.

For more information, see the device-specific TRM for USB connection and On-The-Go feature support.

For more details, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

8 I/O Buffers and Termination

An important task in the hardware design, before beginning schematic capture, is to confirm both DC and AC electrical compatibility between the processor and interfaced devices.

- The device-specific data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, run IBIS simulations using IBIS models provided for the processor to confirm signal integrity.
  - AM654x IBIS Model

For more information on terminations, see the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

9 Power Consumption and Thermal Solutions

The Processor power consumption can vary depending on usage, implementation, topology, component selection, and process variation.

9.1 Power Consumption

Contact TI over E2E and start a new thread for support related to Power Estimation Tool.

9.2 Power Savings Modes

The device supports multiple power saving modes. For more details, see the *Device Power States* section in the *Device Configuration* chapter of the device-specific TRM.

9.3 Guidance on Thermal Solution

The *Thermal Design Guide for DSP and Arm Application Processors* application report provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

For more information, see AM654x Thermal Model.

10 Schematic Recommendations

At this stage of the design, schematic capture can be started. To support in creating the schematics, see the below collection of information.

10.1 Selection of Component and Values

Be sure to use the passive component values recommended in the data sheet when ever applicable .

10.2 Schematics Development

The Schematics can be drawn newly or reused. For examples during the schematic's capture phase, see the *TMDX654GPEVM (AM65x evaluation module (EVM))* and *TMDX654IDKEVM (AM65x industrial development kit (IDK))* schematics.

During schematic capture, follow *AM65x Schematic Checklist* and Errata (*AM65x Processors Silicon Revision*).

Note

When the EVM schematics is reused, ensure the functionality is reviewed and review change in net name before reuse.

When schematics is reused, the DNI setting are reset. Make sure the DNIs are reconfigured (populating DNIs could affect the functionality).

10.3 Reviewing the Schematics

After completing the schematic capture, check the design against the *AM65x Schematic Checklist*.

Plan an internal schematic review to review the schematics with reference to the schematic checklist and inspect other key areas of the schematic for errors, inaccuracies, missing net connections, and so forth.

10.4 Floor planning of the PCB

After schematic capture, TI recommends floor planning of the board to determine the interconnect distances between the various devices, board size and outline.

11 Layout and Routing Guidelines

After completing schematic capture and reviews, the next design step is the PCB layout. For information supporting the board layout, see the following section.

11.1 Escape Routing Guidelines

The *AM654x BGA Escape Routing* application report provides a sample PCB escape routing for the AM65x processor.

11.2 DDR Board Design and Layout Guidelines

The goal of the *AM65x DDR Board Design and Layout Guidelines* application report is to make the DDR4 system implementation straight forward for all designers. Requirements have been captured as a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4 memory that follow the guidelines in this document.

11.3 High-Speed Differential Signal Routing Guidance

The *High-Speed Interface Layout Guidelines* application report provides guidance for successful routing of the high-speed differential signals. This includes PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. TI supports only designs that follow the board design guidelines contained in the application report.

Note

Consider using the *TMDX654GPEVM (AM65x evaluation module (EVM))* and *TMDX654IDKEVM (AM65x industrial development kit (IDK))* layouts as reference.

12 Terminology

CPSW2G – Common Platform Ethernet Switch 2-port Gigabit

DRD – Dual-Role-Device

E2E – Engineer to Engineer

ECAP – Enhanced Capture

eMMC – embedded Multi-Media Card

EMU – Emulation Control

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

HS-RTDX – High Speed Real Time Data eXchange

I2C – Inter-Integrated Circuit Interface

IBIS – Input/Output Buffer Information Specification

IDK – Industrial Development Kit

IEP – Industrial Ethernet Peripheral

JTAG – Joint Test Action Group

LDO – Low Dropout

LVCMOS – Low voltage complementary metal oxide semiconductor

MII – Media Independent Interface

MMC – Multi-Media Card

OSPI – Octal Serial Peripheral Interface

PCB – Printed Circuit Board

PMIC – Power management integrated circuit

POR – Power-on Reset

PRU-ICSSG – Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit

POR – Power-on Reset

PWM – Pulse-Width Modulator

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

SD – Secure Digital

SDIO – Secure Digital Input Output

SGMII – Serial Gigabit Media Independent Interface

SPI – Serial Peripheral Interface

TCK – JTAG Test Clock Input

TDI – JTAG Test Data Input

TDO – JTAG Test Data Output

TMS – JTAG Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – JTAG Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

13 References

- Texas Instruments: *AM654x, AM652x Sitara™ Processors Data Sheet*
- Texas Instruments: *AM65x/DRA80xM Processors Technical Reference Manual*
- Texas Instruments: *AM65x Silicon Errata*
- Texas Instruments: *TMDX654GPEVM (AM65x evaluation module (EVM))*
- Texas Instruments: *TMDX654IDKEVM (AM65x industrial development kit (IDK))*
- Texas Instruments: *TMDX654HSEVM (AM65x high security (HS) evaluation module (EVM))*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors Application Report*
- Texas Instruments: *PRU-ICSS Feature Comparison*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *AM65x/DRA80x Schematic Checklist*
- Texas Instruments: *AM654x/DRA80xM BGA Escape Routing*
- Texas Instruments: *AM65x/DRA80xM DDR Board Design and Layout Guidelines*
- Texas Instruments: *High-Speed Interface Layout Guidelines*

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2018) to Revision A (December 2022)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Added Section 1.2	2
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