Application Report
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AM43xx EMIF Tools

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ABSTRACT

At the center of every application is the need for memory. With limited on-chip processor memory, external memory serves as a solution for large software systems and data storage, and an unstable external memory interface can result in system failures or hinder software development. To prevent potential system level anomalies and ensure robust systems, hardware must be configured correctly and tested thoroughly.

The AM43xx EMIF Tools application focuses on post layout activities, including configuring the Texas Instrument processors for accessing external double data rate (DDR) memories, optimizing delay locked loop (DLL) ratios to compensate for board routing skew. This application report provides a detailed description on how to use the associated application files. The document overview provides a complete list of processors and memory types supported by the AM43xx EMIF Tools application.

The spreadsheet discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/sprac70.

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1 Overview

This document provides detailed steps outlining the procedure to initialize Texas Instruments' processors to access external DDR memories using the accompanying tools included in the AM43xx EMIF Tools application.

1.1 Supported Features of AM43xx EMIF Tools

The AM43xx EMIF Tools application supports the following features:

- TI SOCs: AM437x, AM438x
- DDR Types: DDR3/DDR3L/LPDDR2
- Basic EMIF configuration topics including:
  - Initializing the EMIF and DDR for basic read/write functionality
  - Compensating for signal skew

The source code included in the AM43xx EMIF Tools application is supported by the CPU targets listed in Table 1.

Table 1. Supported CPU Targets

CPU	TI SoC
Cortex-A9	AM437x and AM438x

2 EMIF Configuration

The following section describes how to use the supporting application files to configure the EMIF controller for DDR memory accesses.

2.1 Preliminary Requirements

Before using the supporting application files, ensure that you have access to the following system application information:

- The data sheet of the selected DDR memory
- PCB trace lengths of the DDR clock and strobe signals (required for deriving the right settings for leveling)

2.2 Generating EMIF Register Values

To assist you in defining the EMIF configuration register values, the AM43xx EMIF Tools application provides an EMIF register configuration workbook. The workbook is divided into seven worksheets, and requires specific information pertaining to the system application environment. The first worksheet should be reviewed. The next three worksheets require your input; their tabs are yellow. The fifth worksheet provides the requirement of invert clock. The sixth worksheet calculates the register values based on the provided inputs. The last worksheet provides final register values to be updated on the GEL file.

Table 2. EMIF Register Configuration Worksheets

Worksheet	Description
Title-README	Informative
Step1-SystemDetails	User input: system information
Step2-DDR Timings	User input: timing requirements from DDR data sheet
Step3-Board Details	User input: trace lengths of clock / strobe
Invert Clock Output	Selects between invert_clock setting of 1 or 0 based on the trace lengths
EMIF Tool	Output: calculate register values
Registers	Output: register values

The following sections outline the procedure to complete the various required input parameters of the EMIF configuration workbook.

2.2.1 Step1 – System Details

The first worksheet requires you to input both high level system application details, as well as specific I/O settings for the DDR pins of the TI application processor and DDR memory.

Step 1A seeks system level details and is shown in Table 3 with populated example values.

Table 3. System Application Details

Detail	Description	Value	Units
1	DDR Memory Type	DDR3	–
2	DDR Memory Frequency	400	MHz
3	DDR Data Bus Width	32	Bits
4	DDR DQS	Differential	–
5	DDR Rank	Single Rank	–

The table parameters are defined in detail in the bulleted list below:

- Detail 1 – DDR Memory Type: This value should be selected based on the DDR memory type connected to the TI processor. Pre-defined values are provided in a drop-down menu list based on the supported memory types.
- Detail 2 – DDR Memory Frequency: This value should be selected for the entered DDR clock frequency.
- Detail 3 – DDR Data Bus Width: This value should be selected based on the bus width between the TI processor and the DDR memory. This value represents the bus width per EMIF channel. Pre-defined values are provided in a drop-down menu list.
- Detail 4 – DDR DQS: This value should be selected to match the type of DQS lines. Pre-defined values are provided in a drop-down menu list.
- Detail 5 – DDR Rank: This value should be selected to match DDR rank. Typically, this is the number of chip-selects on the DDR memory

Care should be taken to provide details in order throughout the workbook. As the parameter values are selected, the drop-down menu lists of other parameters may change. In some instances, a previous selected value may no longer be available. In this case, the cell location turns red. Providing the details in order should avoid the necessity to re-select a parameter value.

Step 1B requests specific details pertaining to the DDR memory utilized in the system application. These details are required for the workbook to determine the size and speed bin of the DDR memory. Table 4 shows an example.

Table 4. DDR Memory Specifications

Detail	Description	Value	Units
6	Speed Bin: Data Rate	800	MT/s
7	Density	4	Gb
8	Number of Rows	16	–
9	Number of Columns	10	–
10	Number of Banks	8	–
11 (1)	Speed Bin: CAS Latency @ 800MT/s data rate	5	ntCK
12	Width	16	Bits
13	Average Periodic Refresh Interval	7800	ns

(1) Detail 11 is only used to determine the 'JEDEC" value defined in the worksheet. 'Step2–DDR Timings'. Detail 11 does not correspoind to the actual CAS latency programmed to the EMIF.

The table parameters are defined in detail in the bulleted list below:

- Detail 6 – Speed Bin (Data Rate): This value should be selected to match the rated speed grade of the DDR memory connected to the TI processor.
- Detail 7 – Density: This value should be selected to match the density of a single DDR memory connected to the TI processor. If using 4 x8 DDR memory parts, this value should reflect the density of 1 x8 DDR memory.
- Detail 8 – Number of Rows: This value should be selected to match the number of rows of the DDR memory connected to the TI processor.
- Detail 9 – Number of Columns: This value should be selected to match the number of columns of the DDR memory connected to the TI processor.
- Detail 10 – Number of Banks: This value should be selected to match the number of banks of the DDR memory.
- Detail 11 – Speed Bin (CAS Latency): This value should be selected to match the required CAS latency to ensure functional operation of the DDR memory at the rated speed grade specified by the “Speed Bin: Data Rate” parameter. This is only used to determine the "JEDEC" timing values defined in worksheet "Step2-DDR Timings". It does not correspond to the actual CAS latency programmed to the EMIF. If using a DDR3-1333 speed bin with CL of 9, this parameter should be set to 9.
- Detail 12 – Width: This value should be selected to match the width of a single DDR memory connected to the TI processor. If using 4 x8 DDR memory parts, this value should be set to x8.
- Detail 13 – Average Periodic Refresh Interval: This value should be entered to set the right periodic refresh interval based on the operating conditions of the DDR memory.

Step 1C requires the user to provide the desired I/O settings for the DDR memory termination and output driver impedance. Table 6 illustrates an example configuration for DDR3.

Table 5. DDR Memory I/O Settings (termination/output driver impedance)

Detail	Description	Value	Units	TI Recommendation (1)
14	ODT / Rtt_Nom	RZQ/4	Ω	RZQ/4
15	Dynamic ODT / Rtt_Wr	RZQ/4	Ω	RZQ/4
16	Output Driver Impedance	RZQ/6	Ω	RZQ/6

(1) TI provides default recommendations based on the DDR board routing rules specified in the device-specific data sheet. It is recommended to perform board level signal integrity simulations to validate these settings for optimal performance.

The table parameters are defined in detail in the bulleted list below:

- Detail 14 – ODT/Rtt_Nom: This value applies to the on-die termination of the DDR memory I/O pins. For more information, see the DDR memory data sheet. The DDR memory data sheet specifies these parameters as per the JEDEC DDR standard [1], [2].
- Detail 15 – Dynamic ODT / Rtt_Wr: This value applies to on-die termination during DDR writes when the dynamic ODT mode is enabled. For more information, see the DDR memory data sheet. The DDR memory data sheet specifies these parameters as per the JEDEC DDR standard [1], [2].
- Detail 16 – Output Driver Impedance: This value applies to the output driver impedance of the DDR memory I/O pins. For more information, see the DDR memory data sheet. The DDR memory data sheet specifies these parameters as per the JEDEC DDR standard [1], [2].

Step 1D determines the ZQ calibration and temperature sensitivity settings for the output drive of the DDR memory. For more information on setting these values, see the device-specific DDR memory data sheet. Table 6 illustrates these settings

Table 6. ZQ Calibration Settings

Detail	Description	Value	Units	TI Recommendation (1)
17	ZQCL on Self Refresh	1	–	1
18	Temperature Sensitivity	1.5	%/ºC	0 to 1.5
19	Voltage Sensitivity	0.15	%/mV	0 to 0.15
20	Temperature Drift Rate	1	ºC/Sec	0 to 1
21	Voltage Drift Rate	10	mV/Sec	0 to 15

(1) For more information on setting these values, see the DDR memory data sheet. The DDR memory data sheet specifies these parameters as per the JEDEC DDR standard [1], [2]

The table parameters are defined in detail in the bulleted list below:

- Detail 17 – ZQCL on self refresh: This value if set to 1 enables ZQ calibration long cycle upon self-refresh exit.
- Detail 18 – Temperature sensitivity: This value is the percentage sensitivity of the temperature.
- Detail 19 – Voltage Sensitivity: This value is the percentage sensitivity of the voltage.
- Detail 20 – Temperature Drift Rate: This value is the temperature variation rate with respect to time.
- Detail 21 – Voltage Drift Rate: This value is the voltage variation rate with respect to time.

Step 1E allows you to modify the I/O settings for the DDR pins of the TI application processor. Table 7 illustrates the required input details.

Table 7. DDR IO Configuration (SoC Side)

Detail	Description	Value	Units	TI Recommendations (1)
22	ODT	Full Thevenin	Ω	Full Thevenin
23	Slew Rate: Addr/Ctrl/Clk	Fastest: SR[4:3] = 0b000	–	Fastest: SR[4:3] = 0b000
24	Slew Rate: Data/Strobe	Fastest: SR[4:3] = 0b000	–	Fastest: SR[4:3] = 0b000
25	Output Driver Impedance: Addr/Ctrl/Clk	44	Ω	44
26	Output Driver Impedance: Data/Strobe	44	Ω	44

(1) TI provides default recommendations based on the DDR board routing rules specified in the Data sheet. It is recommended to perform board level signal integrity simulations to validate these settings for optimal performance.

The table parameters are defined in detail in the bulleted list below:

- Detail 22 – ODT: This value applies to the on-die termination of the EMIF I/O pins on the Texas Instruments application processor.
- Detail 23 – Slew Rate (Addr/Ctrl/Clk): This value applies to the slew rate of the EMIF address, control, and clock I/O pins on the Texas Instruments application processor.
- Detail 24 – Slew Rate (Data/Strobe): This value applies to the slew rate of the EMIF data and strobe I/O pins on the Texas Instruments application processor.
- Detail 25 – Output Driver Impedance (Addr/Ctrl/Clk): This value applies to the output driver impedance of the EMIF address, control, and clock I/O pins on the Texas Instruments application processor.
- Detail 26 – Output Driver Impedance (Data/Strobe): This value applies to the output driver impedance of the EMIF data and strobe I/O pins on the Texas Instruments application processor.

2.2.2 Step 2 – DDR Timings

The second worksheet requires you to input DDR timing values that can be found in the DDR memory data sheet. Figure 1 portrays the required timing values required and is populated assuming a DDR3-800 memory operating at 400 MHz.

Parameter	Description	Datasheet Values		Final Bit Field Values		JEDEC Bit Field Values
		tCK	ns	Value	Units	(DDR3-800 @ 400 MHz)
CAS Latency	Delay between internal READ command and data ready	5		5	tCK	
CWL Latency	Delay between internal WRITE command and data ready	5		5	tCK	
tRTW	Read to write	11		7	tCK	
tRP	Precharge command period		13.125	5	tCK	5
tRCD	Active to read or write delay		13.125	5	tCK	5
tWR	Write recovery time		15	5	tCK	6
tRAS	Active to Precharge command period		37.5	14	tCK	15
tRC	Active to Active/Refresh command period		50	19	tCK	20
tFAW	Four Activate Window		50	19	tCK	20
tRRD	Active Bank to Active Bank command period	4	10	1	tCK	2
tWTR	Internal Write to Read command delay	4	10	3	tCK	4
tXP	Exit power down mode to first valid command	3	6	2	tCK	3
tXSNR/tXS	Exit self refresh to commands not requiring a locked DLL	5	270	107	tCK	108
tXSRD/tXSDLL	Exit self refresh to commands requiring a locked DLL	512		511	tCK	512
tRTP	Internal Read to Precharge command delay	4	7.5	3	tCK	4
tCKE	CKE minimum pulse width	3	5	2	tCK	3
tCSTA	Turnaround time	1		0	tCK	
tCKESR	Minimum CKE low width for Self Refresh entry to exit	4	15	3	tCK	4
tZQCS	ZQ short calibration time	64	80	63	tCK	64
tDQSCKmax	Maximum time interval between clock and DQS (For LPDDR2)		5.5	--	tCK	
tRFC	Refresh to Active/Refresh command period		260	103	tCK	104
tRAS (max)	Active to Precharge command period (Max Value)		70200	8	tREFI intervals	9
tREFI	Average periodic refresh interval		7800	3120	tCK	3120

Figure 1. DDR Timings

The following list describes the different columns in Figure 1:

- Parameter: The timing parameter name found in the DDR data sheet. All listed parameters require minimum timing values, except tRAS(max) and tREFI.
- Description: A description of the DDR timing parameter.
- Data Sheet Values: The corresponding DDR timing value found in the DDR data sheet. This value can either be defined in units tCK, ns, or the maximum of either a tCK or ns value. As illustrated in Figure 1, the worksheet calculates the bit field value based off of the maximum of either the tCK or ns value.
- Final Bit Field Value: The final bit field value programmed to the EMIF register. This value is typically in units of clock cycles.
- JEDEC Bit Field Values: This column's intended purpose is for reference only and is dynamically updated based off of the user's input from Section 2.2.1.

The workbook attempts to warn you if an input timing value is tighter than expected (based off of the JEDEC values populated for the memory device detailed in Section 2.2.1). In Figure 2, the timing parameters tWR and tREFI have been changed from that shown in Figure 1. However, a typical minimum write recovery time and average refresh interval for a DDR3 memory is 15 ns and 7.8 µs, respectively. The timing parameter tWR is flagged because the new tWR user input of 10 ns is less than a typical minimum value of 15 ns. In this case, the memory row may be pre-charged too early. The timing parameter tREFI is flagged because the new tREFI user input of 8 µs is larger than a typical average value of 7.8 µs. In this case, the memory may not be refreshed as often as necessary.

Parameter	Description	Datasheet Values tCK	Datasheet Values ns	Final Bit Field Values Value	Final Bit Field Values Units	JEDEC Bit Field Values (DDR3-800 @ 400 MHz)
CAS Latency	Delay between internal READ command and data ready	5		5	tCK	
CWL Latency	Delay between internal WRITE command and data ready	5		5	tCK	
tRTW	Read to write	11		7	tCK	
tRP	Precharge command period		13.125	5	tCK	5
tRCD	Active to read or write delay		13.125	5	tCK	5
tWR	Write recovery time		10	3	tCK	6
tRAS	Active to Precharge command period		37.5	14	tCK	15
tRC	Active to Active/Refresh command period		50	19	tCK	20
tFAW	Four Activate Window		50	19	tCK	20
tRRD	Active Bank to Active Bank command period	4	10	1	tCK	2
tWTR	Internal Write to Read command delay	4	10	3	tCK	4
tXP	Exit power down mode to first valid command	3	6	2	tCK	3
tXSNR/tXS	Exit self refresh to commands not requiring a locked DLL	5	270	107	tCK	108
tXSRD/tXSDLL	Exit self refresh to commands requiring a locked DLL	512		511	tCK	512
tRTP	Internal Read to Precharge command delay	4	7.5	3	tCK	4
tCKE	CKE minimum pulse width	3	5	2	tCK	3
tCSTA	Turnaround time	1		0	tCK	
tCKESR	Minimum CKE low width for Self Refresh entry to exit	4	15	3	tCK	4
tZQCS	ZQ short calibration time	64	80	63	tCK	64
tDQSCKmax	Maximum time interval between clock and DQS (For LPDDR2)		5.5	--	tCK	
tRFC	Refresh to Active/Refresh command period		260	103	tCK	104
tRAS (max)	Active to Precharge command period (Max Value)		70200	8	tREFI intervals	9
tREFI	Average periodic refresh interval		8000	3200	tCK	3120

Figure 2. DDR Timings (Warning)

Although the warnings may serve as a quick sanity check in the event that a timing parameter is accidentally input incorrectly, you should ultimately ensure the final bit field values comply with the timing values specified in their DDR data sheet.

2.2.3 Step 3 – Board Details

The third worksheet requests you to enter the microstrip and stripline PCB delay per inch, PCB trace lengths of the DDR clock and strobe signals from the TI application processor to the DDR memories for each byte lane. This information is pertinent for systems utilizing a fly-by topology to interface to DDR3/L memories. The PCB trace lengths are required to determine an approximation of the PCB flight skew of the signals, and identifies the requirement of an invert clock.

Table 8, Figure 3 and Figure 4 illustrate the format for which the PCB trace lengths should be provided. Because a particular trace may be routed on more than one layer of the PCB, you should identify which portions of the trace are routed on the outer layers of the PCB (Microstrip) and which portions are routed on the inner PCB layers between two planes (Stripline).

Table 8. PCB DDR Trace Lengths

DRAMs Connected to EMIF								
	PCB Trace Length in Inches							
	Byte 0		Byte 1		Byte 2		Byte 3	
Signal	Microstrip	Stripline	Microstrip	Stripline	Microstrip	Stripline	Microstrip	Stripline
CLK	0.000	2.500	0.000	2.500	0.000	2.500	0.000	2.500
DQSn	0.000	2.500	0.000	0.100	0.000	0.100	0.000	4.000

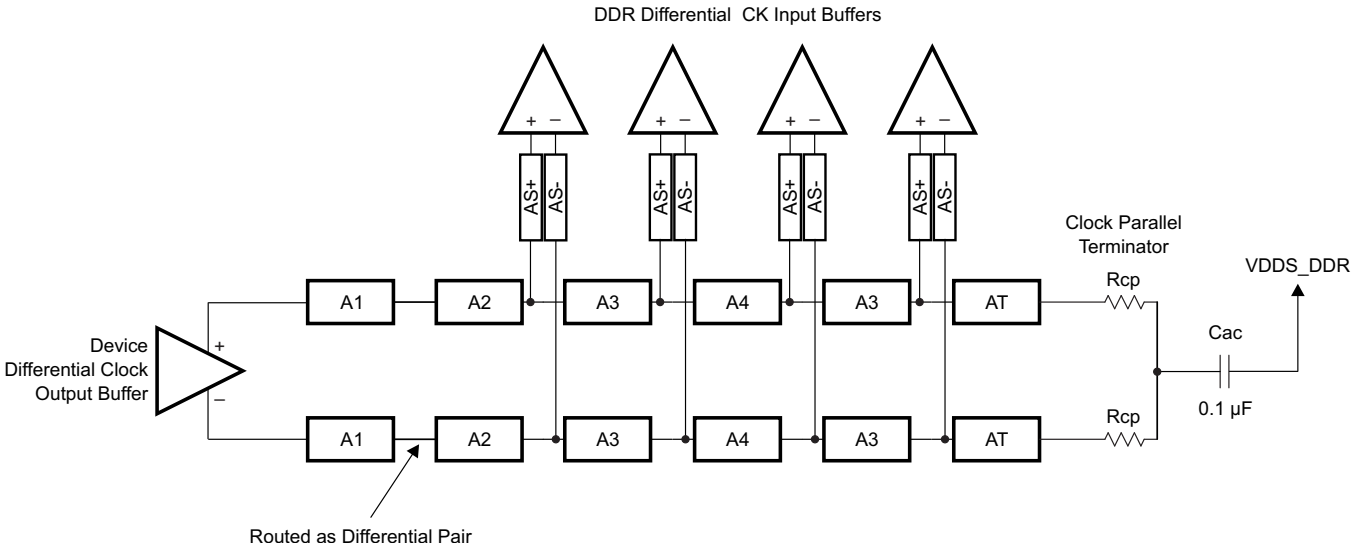

Figure 3. CK Topology for Four DDR3 Devices

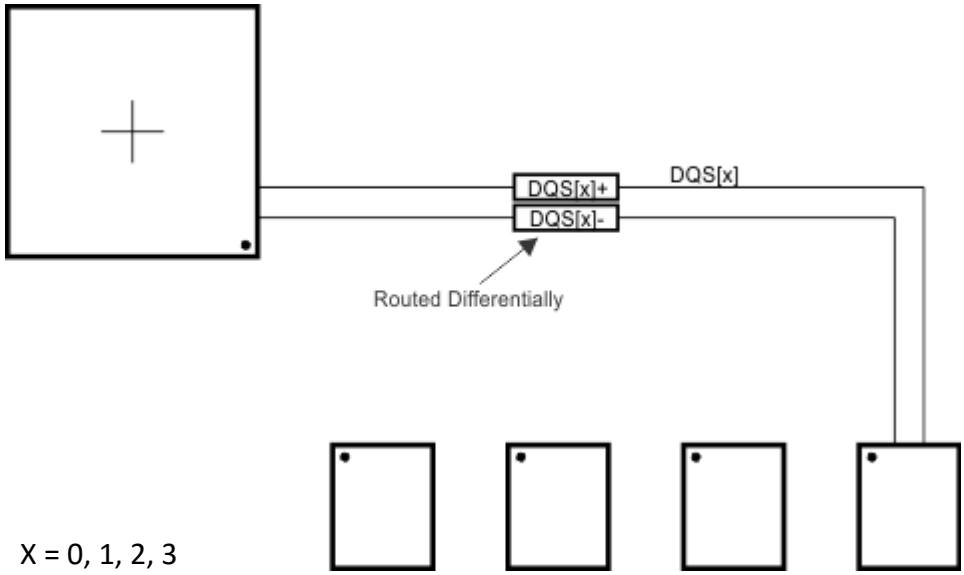

Figure 4. DQS[x] Routing With Any Number of Allowed DDR3 Devices

2.2.4 Invert Clock

After the system level, board level, and DDR timing details have been populated in their corresponding worksheets, you can access the fifth worksheet, “Invert Clock", to obtain the invert clock value.

This worksheet computes the requirement of an invert clock based on the information provided in the board details worksheet. It would compare the lengths of clock and DQS signals and identify the invert clock necessity.

2.2.5 EMIF Tool

In sixth worksheet, various EMIF configuration register values are computed based on the information given in step 1, 2 and 3 worksheets.

2.2.6 Registers

In this worksheet, you could get the consolidated list of EMIF Registers, DDR PHY registers, IO Control Registers and LPDDR2 DDR memory-specific mode register values to be programmed in the GEL file or registers that need to be programmed in the EMIF configuration code.

3 References

1. DDR3 SDRAM Standard, JESD79-3F, 2012
2. LPDDR2 SDRAM Standard, JESD209-2F, 2013
3. AM4372, AM4376, AM4377, AM4378, AM4379 Sitara™ Processors Data Manual

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2017) to A Revision	Page
• The associated zip file was updated from v20 to v21.	1

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