Calculator for CAN Bit Timing Parameters

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ABSTRACT

Controller Area Network (CAN) nodes use user-specified timing parameters to sample the asynchronous bitstream and recover the clock. These parameters are typically based on the frequency of the available reference oscillator. There may be several options available for a given frequency, and some of them will allow a looser oscillator tolerance than others. This application report details the creation of a bit timing calculator to maximize the oscillator tolerance for the CAN modules on TI microcontrollers.

Project collateral discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/sprac35.

Contents

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1 Introduction

Calculation of the bit timing parameters requires at least three inputs:

- The desired bit rate, which is common across the entire bus.
- An estimate of the propagation delay between the most distant nodes on the bus
- The CAN module clock frequency, which is used to derive the bitstream sampling clock

The propagation delay comes from two main sources: the speed of electromagnetic propagation along the bus wiring and extra delay due to transceivers, isolation, or other interface circuitry.

A bit timing calculator must provide at least five outputs:

- The baud rate prescaler (BRP), which determines the sampling clock period. A single period is referred to as a time quantum (Tq).
- The propagation delay expressed as a number of time quanta.
- The length of phase segment 1 (PhSeg1) in time quanta. In addition to determining the bit rate, phase segment 1 acts as a buffer that can be lengthened to resynchronize with the bitstream.
- The length of phase sergment 2 (PhSeg2) in time quanta. Phase segment 2 is like phase segment 1, but it occurs after the sampling point instead of before. Phase segment 2 can be shortened to resynchronize with the bit stream.
- The synchronization jump width (SJW) in time quanta. This is the maximum time by which the bit sampling period may be lengthened or shortened during each cycle to adjust for oscillator mismatch between nodes.

The calculator described in this document also outputs the number of time quanta per bit, the oscillator tolerance, the sampling point, and timing register values for the eCAN and D_CAN modules used on the TMS320C2000™ series of microcontrollers.

2 Implementation

The calculator first computes the propagation time as a fraction of the bit period. Either the bus length, a physical propagation delay, or both may be specified. The bus propagation speed is assumed to be two thirds of the speed of light, the standard value for twisted pair cable. The resulting delay time is doubled to give a round trip delay.

The number of time quanta per bit (known as the bit time) can range from 8 to 25. There is no analytic formula for determining the optimum bit time in advance, so the calculator tries all of them. The closest integral baud rate prescaler is calculated for each value. The BRP and Tq/bit values are then used to calculate the actual sampling bit rate. Any difference from the desired value is added to the total tolerance later.

The propagation segment is determined from the fraction computed above, rounded up. The remaining time is split between phase segments 1 and 2, with PhSeg2 rounded up and PhSeg1 rounded down.

The synchronization jump width is limited to 4 Tq at most, and cannot be longer than PhSeg1 or PhSeg2. Thus, the SJW is the minimum of these three values.

Oscillator tolerance is derived from two formulas. The first gives the condition for correct evaluation of 13 dominant bits in a row during an error condition, where there is no re-synchronization:

$$df \leq = \frac{\min(PhSeg1, PhSeg2)}{(2 \times (13 \times bit\_time - PhSeg2))} \quad (1)$$

The second formula gives the condition for full re-synchronization after 10 consecutive bits:

$$df \leq = \frac{SJW}{(2 \times 10 \times bit\_time)} \quad (2)$$

The factor of 2 in each formula comes from considering two oscillators on different nodes, each having the worst-case frequency error in opposite directions. The final oscillator tolerance is the minimum of these two values minus any error in the nominal frequency.

Once the tolerances for all possible values of Tq/bit have been calculated, the settings with the best tolerance are chosen. These are reported in the output section of the calculator. The settings are then converted into eCAN and D_CAN register values, which are also reported.

The calculator can report errors based on several conditions:

- The CAN clock frequency must be at least 8 times the bit rate to give the minimum 8 Tq/bit.
- The propagation delay must be short enough to allow reasonable values for the phase segments.
- The ratio between the CAN clock and the bit rate must be close enough to an integer to produce a usable BRP.

The calculator reports a warning when the exact bit rate cannot be derived from the CAN clock frequency. It also reports a warning when the propagation time is more than half the bit time, since this implies that the bus length is too long for the desired bit rate.

3 References

- *Introduction to the Controller Area Network (CAN)* (SLOA101)
- *Controller Area Network Physical Layer Requirements* (SLLA270)
- *Bosch CAN Specification* (www.kvaser.com/software/7330130980914/V1/can2spec.pdf)

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