Application Report

SPRAC24–January 2016

ADC as Voltage Monitoring in TDA3x

Vivek Dhande and Sivaraj R

ABSTRACT

The analog-to-digital conversion (ADC) module in TDA3x can be used as voltage monitoring. This application note describes how the ADC module can be used for monitoring the input core voltages coming from the PMIC on the board/EVM.

Contents

1 ADC Module Overview

The continuous mode of operation can be used along with the high and low range check feature of ADC to continuously monitor the ADC input channels.

1.1 Continuous Mode

In case of continuous mode, the ADC continuously converts each channel input in a round robin fashion at the ADC clock rate of 10 MHz.

Each channel conversion takes minimum 18 ADC clock cycles to > 300 ADC cycles depending up on the various delays and averaging mode selected.

Based on this rate, the ADC FIFO (of size 64 words) will get filled up with converted data and can overflow if the FIFO is not read out - either by CPU or DMA.

So, when using continuous mode, it is recommended that you should configure DMA to pull the data out from the FIFO. For details, see the *ADC Functional Description* section of the *TDA3x SoC for Advanced Driver Assistance Systems (ADAS) Silicon Revision 1.0 Technical Reference Manual* (SPRUHQ7).

1.2 Range Check

When this feature is enabled, the ADC module can generate a separate event interrupt to the CPU when the converted channel data crosses a particular range (> high or < low).

Then the CPU/driver can use this interrupt event to detect "bad" voltage and take appropriate action.

This range check feature is independent of continuous or single shot mode of operation. But this is effective to be used in continuous DMA mode as there is no CPU intervention for data range check as explained in continuous DMA mode.

For details, see the *ADC Functional Description* section; for register settings, see the *ADC Register Description* section of the *TDA3x SoC for Advanced Driver Assistance Systems (ADAS) Silicon Revision 1.0 Technical Reference Manual* (SPRUHQ7).

2 Voltage Monitoring

Continuous voltage monitoring can be achieved in two different ways as explained in the following sections.

2.1 Continuous Mode With CPU

If CPU is used to read out the ADC FIFO, then interrupts are generated for every round of conversion. Then, the CPU can read out the FIFO content and does the necessary voltage check.

In this case, the CPU utilization might be high depending on the rate at which the conversion is performed.

NOTE: The range check feature is not very effective as the CPU is always reading the data from the FIFO. Adding the range check manually is not going to use more CPU cycles compared to reading FIFO data and ISR handling.

2.2 Continuous Mode With DMA and Range Check Enabled

In this mode, the DMA is programmed to read out the FIFO and write the conversion results in a circular buffer. Since range check is enabled, the CPU can rely on the range check interrupt to decide if the voltage has gone out of range. Based on that information, it can read and check the buffer. Checking of each and every data is not required unlike CPU mode. This mode consumes the least amount of CPU cycles.

NOTE:

- Follow the software sequences to recover from FIFO overflow error. FIFO overflow, as such, is not a catastrophic failure except that you will lose the ADC input data until the ADC conversion is restarted.
- The range check feature can be enabled or disabled selectively per channel. But, the high and low range value is common for all channels. Therefore, you can not have a different voltage range check for different channels; all channels need to use the same range. For instance, if supply voltage DSP_EVE and VDD_CORE of TDA3x are being monitored, the range should be based on the minimum of the two as based on the value provided in the *TDA3x SoC for Advanced Driver Assistance Systems (ADAS) 15mm Package (ABF) Data Manual* (SPRS916). If this is not acceptable, the CPU mode of monitoring will be more flexible.

2.3 Deciding CPU Vs DMA Mode

Continuous monitoring using the CPU is more flexible but requires high CPU cycles, whereas, DMA uses less CPU cycles but with limited range check across channels.

Apart from this limitation, consider the sampling rate at which the voltage needs to be monitored. The choice of sampling rate should be based on the rate at which voltage can change in the power supply circuitry.

Therefore, it is not always necessary to sample the input at the maximum possible clock of 10 MHz and use up the CPU cycles.

Instead, the ADC clock can be further divided using prescalar as per the required sampling rate; hence, you could still use CPU mode that provides maximum flexibility with minimum CPU cycles.

For example, based on the EVM layout, if it is decided that each channel voltage needs to be sampled for every 1ms, then each channel sampling is 1 KSPS (kilo sample per second).

If there are 8 channels, this turns up to 8 KSPS. If you use 16 sample average and minimum open/sampling delays, then each sample will take 273 ADC clock cycles.

Therefore, the ADC clock can be reduced to 8x273 KHz = 2.184 MHz and the corresponding CPU utilization might be under and acceptable number.

3 References

1. *ADC* chapter of the *TDA3x SoC for Advanced Driver Assistance Systems (ADAS) Silicon Revision 1.0 Technical Reference Manual* (SPRUHQ7)
2. *TDA3x SoC for Advanced Driver Assistance Systems (ADAS) 15mm Package (ABF) Data Manual* (SPRS916)

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