Application Report
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C5000 DSP-Based Low-Power System Design

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ABSTRACT

Low-power consumption is one of the most important requirements for the embedded system. The C5000™ ultra low-power DSP family is ideal for portable devices (audio, voice and vision) and other applications that require analytics with low power.

To take advantage of this feature in system design, good practices need to be carried out. This application report focuses on the Texas Instruments' C5000 DSP family. Low-power related features are highlighted on the architecture level and keynotes are presented for the C5000-based system design.

The term "C5000" mentioned in this document represents the latest C55x5, C55x4 and C5517 family devices, including devices like C5505/15/35 and C5504/34, and so forth.

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1 Introduction

The main factors for the power consumption of CMOS devices are discussed in the following sections.

1.1 Dynamic Power Consumption

Two main factors affect the dynamic power consumption of CMOS devices: switching frequency (f) and operation voltage (V). The dynamic power dissipation of a CMOS circuitry can be calculated according to Equation 1:

$$Pa = CV^2 f \quad (1)$$

- C is the capacitance load
- V is the operation voltage
- f is the operation frequency

Based on Equation 1, the dynamic (or active) power is proportional to the square-of-the-V, and frequency and capacitance. So, an optimized system design means to set the DSP working at a state in which the active frequency and voltage meets the application performance requirements (while not over clocking the devices or applying a higher voltage than it needs).

Since the C5000 is targeting the low-power applications, the architecture has numerous features and flexibility that can manipulate the core-voltages and set various operation frequencies based on different applications.

1.2 Static Power Consumption

The static power consumption consists of the leakage of a CMOS device (the I/O configuration of the device).

The following sections discuss the related features of C5000 and describe how to use them to achieve the optimized power consumption on system-level design and development.

2 Power Domain and Operation Voltage Control

C5000 has several power domains that supply power to various modules inside the DSP. Table 1 lists all the power domains in C5000. It also indicates the power supply source and whether or not it can be turned off.

Table 1. Power Domains Inside C5000 DSP

Domains	Ranges (V)	Supply sources	Can-be-off?	Description
Digital core	1.05/1.3/1.4	DPS_LDO or External	Yes	If the DSP_LDO is turned off by DSP software, the only way to wake it up is by using WAKE_UP pin or pre-set RTC alarm.
I/O1	1.8/2.5/2.75/3.3	External	Yes	This power domain is for all the digital I/Os, except EMIF
I/O2 (EMIF) (1)	1.8/2.5/2.75/3.3	External	Yes	This power domain is for EMIF interface only
USB_3.3	3.3	External	Yes	USB_PLL and line transceiver
USB_1.3	1.3	USB_LDO or External	Yes	USB core
Analog	1.3	ANA_LDO or External	Yes	Analog module: PLL, SAR
DVDDRTC	1.8/2.5/2.75/3.3	External	No	WAKE_UP, RTC CLKOUT
CVDDRTC	1.05/1.3	External	No	RTC core, RTC CLOCK
LDOI	1.8/3.3	External	No	LDOs, bandgap, and I/O supply for some input pins

(1) Some of the c55x family of device do not have external memory interface (EMIF). For information on the available peripherals, see device-specific data manual.

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To provide a flexibility of the system power consumption for different applications, the EMIF, USB_1.3, and USB3.3 power domains can be turned off permanently turned off when these specific peripherals are not used. C5000 has the "voltage scaling" feature for CPU core power domain, this means that the software can lower or raise the core supply's voltage on-the-fly.

The internal DSP-LDO can be used to implement the voltage scaling of the DSP core.

- First, one can enable the internal LDO by connecting the DSP_LDO_EN pin to ground.
- After reset, once the trim updates are performed by the bootloader, the output voltage of DSP-LDO will be set at 1.3 V.
- The software can adjust the output voltage to 1.05 V by setting the DSP_LDO_V bit (bit-1) in the LDOCNTL register to "1". Before accessing LDOCNTL, either the ANA or SAR clock gating register should be off to allow CPU to write and read to the LDOCNTL register (0x7004).
- Attention must be paid to the clock frequency when lowering the voltage. The clock frequency should be adjusted first according to the operation range, before lowering the voltage. Otherwise, the device might become unstable. Table 2 provides details on operating voltage and corresponding frequencies.

Table 2. C5000 CPU Operation Frequency vs Voltage

Core Voltages (V)	Core Operating Frequency (MHz)	I/O Voltages (V)
1.05	60 MHz or 75 MHz	1.8 2.5 2.75 3.3
1.3	100 MHz or 120 MHz	1.8 2.5 2.75 3.3
1.4	150 MHz	1.8 2.5 2.75 3.3

3 Clock Control of C5000

Another important factor for dynamic power consumption is frequency/clock.

C5000 provides multiple ways to configure the system clock and to control the clocks that are distributed to CPU core and peripherals. Depending on the source of the system clock, the clock generation can be configured in three modes: PLL bypassed and system running, PLL bypassed and system running, and PLL engaged and system running.

3.1 C55x5 Device

- ***PLL bypassed and system running at RTC clock***: If the first clock mux is selecting the RTC as its input, and the PLL is bypassed, then the 32.768 KHz RTC clock will be used as the system clock. Since the RTC clock is running at very slow frequency, with the DSP core idling and peripherals gated (will cover these later), this will be the most power-conserved mode.
- ***PLL bypassed and system running at external input clock***: If the first clock mux is selecting CLKIN (an external clock) as its input, and the PLL is bypassed, then an external clock will be used as the system clock. The nominal frequency of the external clock is 12 MHz.
- ***PLL engaged and system running at PLL output***: If the PLL is selected as the source for the system clock, the system will run at the output frequency of the PLL. Usually, this mode should be used as the normal active mode. Benefits from the programmability of PLL, system can operate at wide frequency range in this mode. Depend on the version of the device; the PLL can go up to 150 MHz.

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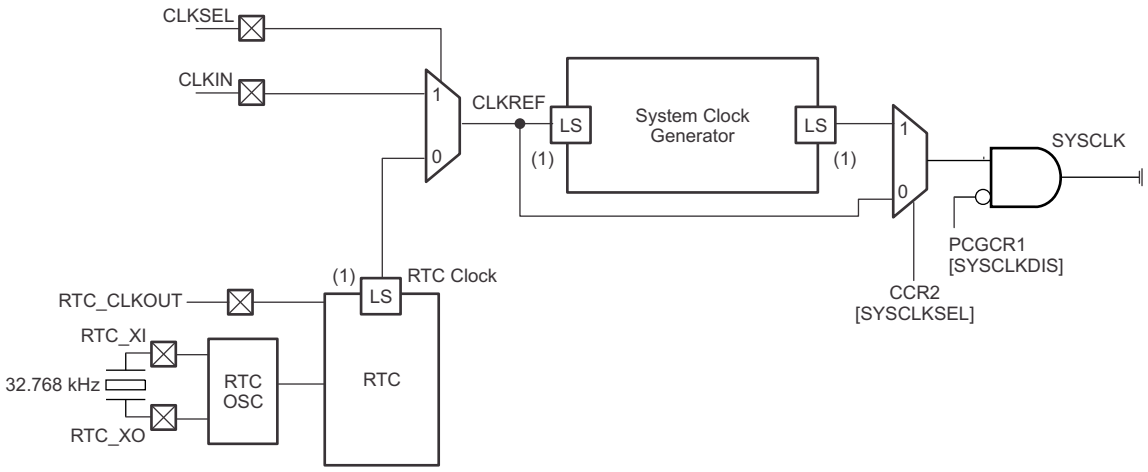

Figure 1. System Clock Generation - C55x5

3.2 C5517 Device

- ***PLL bypassed and system running at 12 MHz USB Reference Clock***: The system clock generator can be fully bypassed and the input reference clock can be passed directly to the DSP system clock. The USB reference clock is generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB_MXI and USB_MXO pins. This crystal is not required if the USB oscillator is not used as input to the system reference clock and the USB peripheral is not being used.
- ***PLL bypassed and system running at external input clock***: If the first clock mux is selecting CLKIN (an external clock) as its input, and the PLL is bypassed, then an external clock will be used as the system clock. The frequency of the external clock is expected to be CLKIN frequency is expected to be 11.2896 MHz, 12.0 MHz, 12.288 MHz, 16.8 MHz, or 19.2 MHz
- ***PLL engaged and system running at PLL output***: If the PLL is selected as the source for the system clock, the system will run at the output frequency of the PLL. Usually, this mode should be used as the normal active mode. Benefits from the programmability of PLL, system can operate at wide frequency range in this mode. Depend on the version of the device; the PLL can go up to 200 MHz.

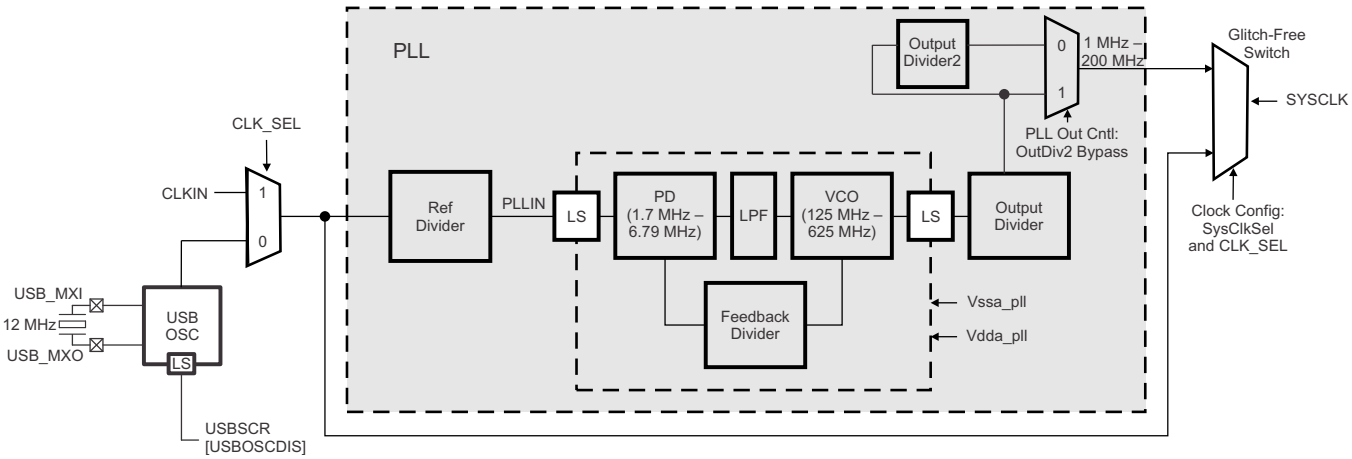

Figure 2. System Clock Generation – C5517

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Based on these three modes, system clock control can be elaborated further:

- The PLL is not used and can be turned off to save power shown in the first and second mode in Section 3.2.
- The PLL is engaged, so the system level programmer and designer can set the output PLL running at an optimized frequency for the specified application as shown in the third mode in Section 3.2.
- The system can switch between the first, second and third modes on-the-fly. In other words, the system PLL can be turned ON or OFF based on the need.

System clock will provide operation clocks for DSP but and the peripherals. This clock will be distributed to each individual module. If modules will not be used for a specific application, the distribution of the clock to these modules can be turned OFF (gated) to save power.

There are two types of clock gating in C5000: one is for CPU core and the other is for peripherals. These two types are highlighted in the following:

- The CPU core: clock can be gated by setting the idle configuration register (ICR) and the Idle Status Register (ISTR), and then issuing idle instruction.
- The peripherals: clock can be gated by setting the corresponding bits of the Peripheral Clock Gating Configuration Registers (PCGRC1 (0x1C02) and PCGCR2 (0x1C03)); no instruction is needed. However, two peripherals, EMIF and universal asynchronous receiver/transmitter (UART), need to be treated differently. For these two peripherals, a gating request must first be submitted. After the request is acknowledged, the clock can be turned OFF safely.

The following three example codes illustrate how to implement the clock control and configuration in system software.

The example code to gate CPU core and put it into "idle":

```
#define ICR 0x0001
.
.
.
*(ioport volatile unsigned int *)ICR = 0x03EF; // Request to disable ports & C55x CPU

//add 6 "nop" clearing pipeline
asm (" nop");
asm (" nop");
asm (" nop");
asm (" nop");
asm (" nop");
asm (" nop");

asm (" idle"); //idle the CPU

//DSP will go to sleep until a wake-up event occurs
//DSP will wake up and start from here
.
.
.

The example code to gate the peripherals (including EMIF and UART)


#define PCGCR1 0x1c02
#define PCGCR2 0x1c03
#define CLKCFGMSW 0x1c1f
#define CLKSTOP 0x1C3A
#define PLL_CNTL1 0x1c20
.
.
.
Uint16 i;
Uint16 temp;
Uint16 clk_stop_ack = 0;
.
```


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```
.
.
//Request to stop the UART and EMIF clock
temp = *(ioport volatile unsigned int *)CLKSTOP;
*(ioport volatile unsigned int *)CLKSTOP = temp | 0x0011;

//Check if the two STOPPING requests have been granted by reading the CLKSTOP register
while (clk_stop_ack != 0x0022){
temp = *(ioport volatile unsigned int *)CLKSTOP;
clk_stop_ack = temp & 0x0022;
}

//leave the system-clock on (bit-15), but gated all peripherals' clocks
*(ioport volatile unsigned int *)PCGCR1 = 0x7FFF;
*(ioport volatile unsigned int *)PCGCR2 = 0x007F;

//bypass the PLL (bit0 = 0), now the system clock is from the RTC clock
*(ioport volatile unsigned int *)CLKCFGMSW = 0x0;

for (i=0; i&lt;50; i++); //add extra software delay

//power down the PLL
temp = *(ioport volatile unsigned int *)PLL_CNTL1;
*(ioport volatile unsigned int *)PLL_CNTL1 = temp | 0x1000 ;

*( volatile unsigned *)IFR0 =0xFFFF; //clear all interrupt flags
*( volatile unsigned *)IFR1 =0xFFFF; //clear all interrupt flags
```

The example code to set the system PLL running at certain frequency in active mode; set to 100 MHz case is used in the example.

```
#include <stdio.h>
#include <tistdtypes.h>
#define IDLE_CTRL0 0x1c02
#define IDLE_CTRL1 0x1c03
#define CLKCFGMSW 0x1c1f
#define PLL_CNTL1 0x1c20
#define PLL_CNTL2 0x1c21
#define PLL_CNTL3 0x1c22
#define PLL_CNTL4 0x1c23
#define CCSSR *((volatile ioport unsigned *)(0x1c24)) //CLKOUT selection register
#define ST3_55 *((volatile unsigned *)(0x0004)) //CPU register ST3_55

void ProgramPLL_100MHz_clksel0()
{
:Uint16 regVal;
:Uint16 i;
Uint16 st3_55_rd;

:for (i=0; i<30000; i++);

// Enable clocks to all peripherals
*(ioport volatile unsigned int *)IDLE_CTRL0 = 0x0;
*(ioport volatile unsigned int *)IDLE_CTRL1 = 0x0;

// bypass PLL
*(ioport volatile unsigned int *)CLKCFGMSW = 0x0;

*(ioport volatile unsigned int *)PLL_CNTL1 = 0x8BE8;
*(ioport volatile unsigned int *)PLL_CNTL2 = 0x8000;
*(ioport volatile unsigned int *)PLL_CNTL3 = 0x0806;
*(ioport volatile unsigned int *)PLL_CNTL4 = 0x0000;

// Busy wait until TESTLOCKMON is high or timeout
:do
:{
regVal = *(ioport volatile unsigned int *)PLL_CNTL3;
```


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```
:} while ((regVal & 8) == 0) ;

// Switch to PLL clk
*(ioport volatile unsigned int *)CLKCFGMSW = 0x1;
for (i=0; i<30000; i++);

//following part route the DSP clock to CLK_OUT pin
CCSSR = 0x000B; //CCSSR, CLOCKOUT pin setting: 0xF=USB_PHY_CLK; 0xB=DSP_CLK
st3_55_rd = ST3_55; //read ST3_55 register ST3_55 = st3_55_rd & 0xFFFB; //enable CLKOUT pin for
debug only
}
```

The above three examples are extracted from the application programs; they illustrate typical cases in real applications.

Table 3 summarizes C5000 clock structure. This information helps to create a clock control scheme and write control program for a specific application.

Table 3. Clock Domains Inside C5000

Domains	Can-be-Gated?	Registers	Descriptions
RTC	No		RTC clock should always be on.
PLL	Yes	CCR2 (b0)	PLL can be turn off, in this case the internal clock generator block is bypassed.
USB	Yes	PCGCR2 (b2)	Clock source for USB PLL and USB digital core
SYS_CLOCK	Yes	PCGCR1 (b15)	This is the clock that is distributed to CPU cores and the peripherals (except the USB-PHY). Set the WAKEUP pin high to re-enable system clock
FFT	Yes	ICR (b9)	FFT co-processor; issue idle instruction to gate clock
MPORT	Yes	ICR (b7)	MPORT of core; issue idle instruction to gate clock
XPORT	Yes	ICR (b6)	XPORT of core; issue idle instruction to gate clock
IPORT	Yes	ICR (b8)	IPORT of core; issue idle instruction to gate clock
DPORT	Yes	ICR (b5)	DPORT of core; issue idle instruction to gate clock
CPU	Yes	ICR (b0)	CPU core; issue idle instruction to gate clock
EMIF	Yes	PCGCR1 (b11)	Request gating first, then set the corresponding register bit to gate clock
SPI	Yes	PCGCR1 (b1)	Set the corresponding register bit to gate clock
I2S0	Yes	PCGCR1 (b8)	Set the corresponding register bit to gate clock
I2S1	Yes	PCGCR1 (b9)	Set the corresponding register bit to gate clock
I2S2	Yes	PCGCR1 (b14)	Set the corresponding register bit to gate clock
I2S3	Yes	PCGCR1 (b0)	Set the corresponding register bit to gate clock
SAR	Yes	PCGCR2 (b1)	Set the corresponding register bit to gate clock
LCD	Yes	PCGCR2 (b0)	Set the corresponding register bit to gate clock
MMC/SD0	Yes	PCGCR1 (b4)	Set the corresponding register bit to gate clock
Ana. Reg.	Yes	PCGCR2 (b6)	Set the corresponding register bit to gate clock
MMC/SD1	Yes	PCGCR1 (b7)	Set the corresponding register bit to gate clock
Timer0	Yes	PCGCR1 (b10)	Set the corresponding register bit to gate clock
Timer1	Yes	PCGCR1 (b12)	Set the corresponding register bit to gate clock
Timer2	Yes	PCGCR1 (b13)	Set the corresponding register bit to gate clock
UART	Yes	PCGCR1 (b2)	Request gating first, then set the corresponding register bit to gate clock
I2C	Yes	PCGCR1 (b6)	Set the corresponding register bit to gate clock
DMA0	Yes	PCGCR1 (b3)	Set the corresponding register bit to gate clock
DMA1	Yes	PCGCR2 (b3)	Set the corresponding register bit to gate clock
DMA2	Yes	PCGCR2 (b4)	Set the corresponding register bit to gate clock
DMA3	Yes	PCGCR2 (b5)	Set the corresponding register bit to gate clock
McBSP	Yes	PCGCR1 (b5)	Set the corresponding register bit to gate clock - (C5517 only)

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Table 3. Clock Domains Inside C5000 (continued)

Domains	Can-be-Gated?	Registers	Descriptions
McSPI	Yes	PCGCR1 (b9)	Set the corresponding register bit to gate clock - (C5517 only)
McSPISPIREF	Yes	PCGCR2 (b7)	Set the corresponding register bit to gate clock - (C5517 only)
UHPI	Yes	PCGCR2 (b1)	Set the corresponding register bit to gate clock - (C5517 only)

Figure 3 is an illustration of the clock diagram for the C55xx devices. The same information can be found in the *TMS320C5515 DSP System User's Guide* (SPRUFX5).

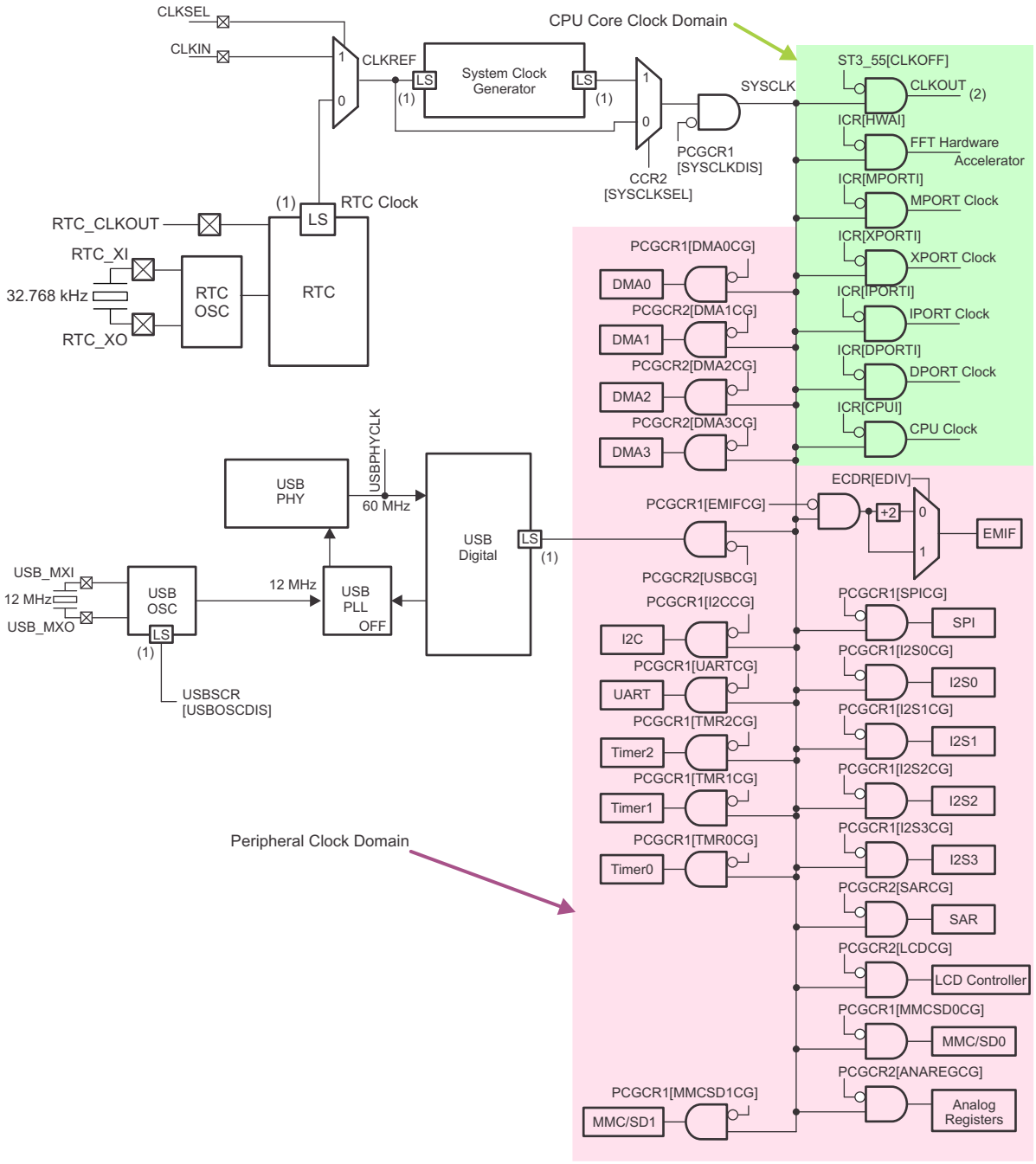

Figure 3. C55x5 Clock Diagram

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Figure 4 also illustrates the clock diagram for the C55xx devices.

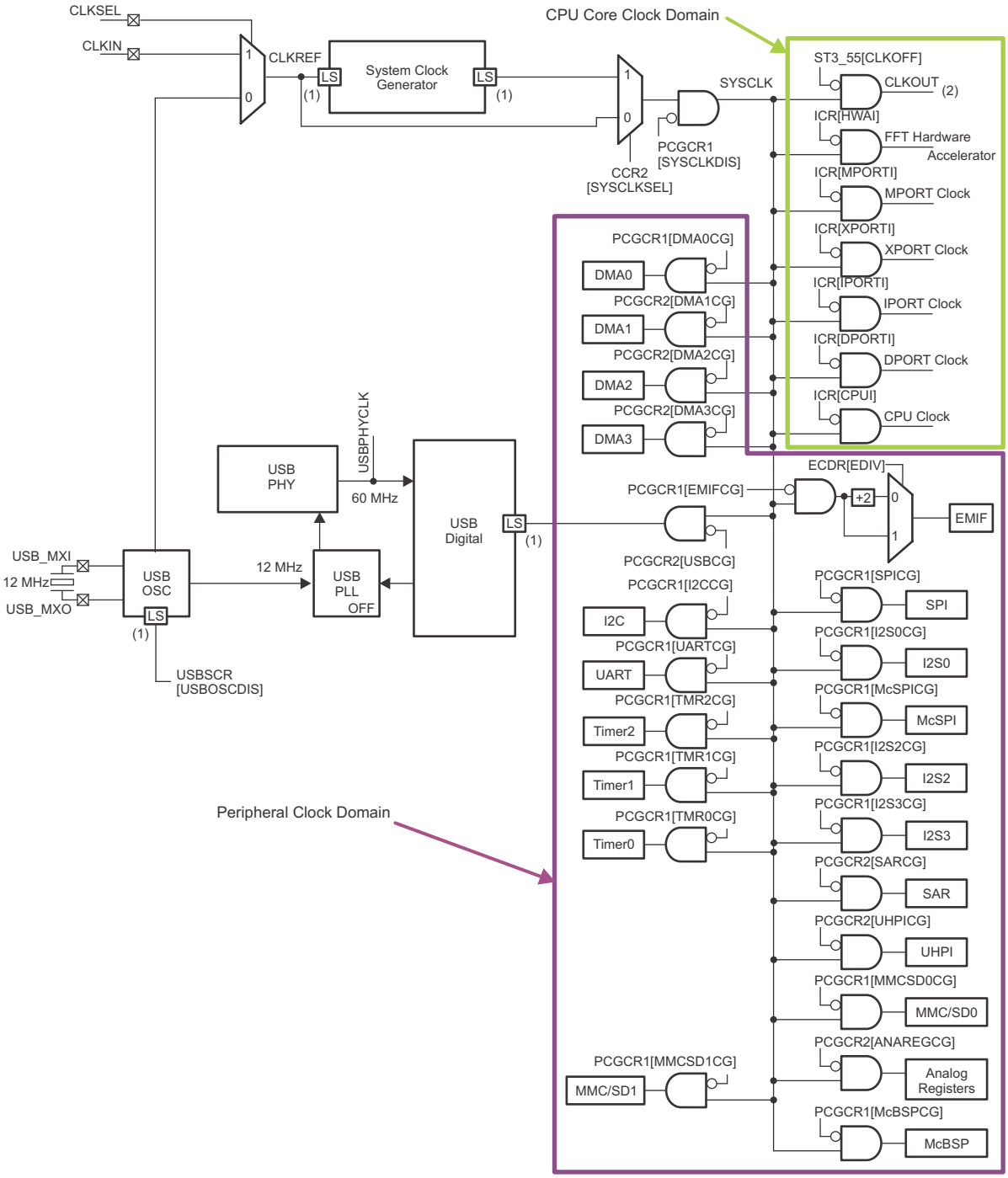

Figure 4. C5517 Clock Diagram

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4 I/O Configuration and Static Power Consumption

4.1 Overview of CMOS I/O

The two important factors that affect the device power consumption were discussed in previous sections. They are critical for reducing the dynamic (active) power. The factors that affect the static power consumption are presented in this section.

Static power refers to the power consumption that is not functionally related. For example, part of the static power consumption is caused by the leakage of the device and the other aspect is, device not being configured correctly at the system level, this will cause addition power consumption and it could be quite significant too.

In this section, focus is on the I/O pin configuration.

In general, a basic CMOS input cell circuitry is illustrated as shown in Figure 5.

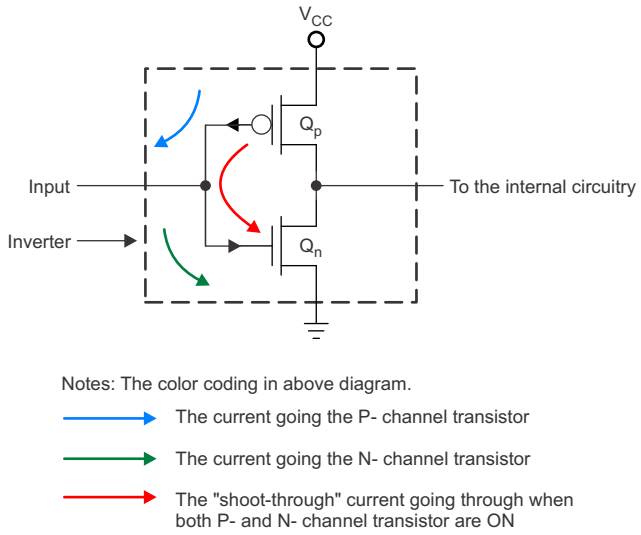

Figure 5. CMOS I/O

During a normal operation, depend on the input is at "High" or at "Low", one of the two transistors will be turned ON at a time. The current flow will take either the "Green" path or the "Blue" path as depicted in the diagram. These are the normal-amount current.

But when the input node is floating, the input node could be at the "threshold" region for a long period of time. At some point in this "threshold" region, both transistors will be ON (or partial ON); when this condition occurs, a significant amount of current will flow through from the VCC (power supply) to the ground. The current flow will now take the "red" path as depicted in the above diagram; sometime this current is called "shoot-through" current. This current will increase the power consumption dramatically.

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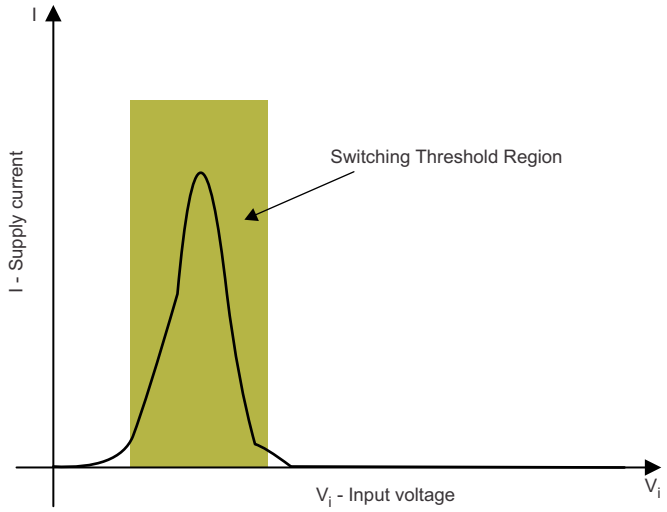

Figure 6. Switching Threshold Region

It is very likely, that the floating inputs could be in the "threshold region". As presented in Figure 6, the high current flow is in that region.

The floating-input condition makes the system behavior "un-predictable". For example, with the same system configuration that is running hardware with the same software, but while in standby mode, power consumption can vary drastically between the units.

Figure 7 shows the two potential "problematic" input pins.

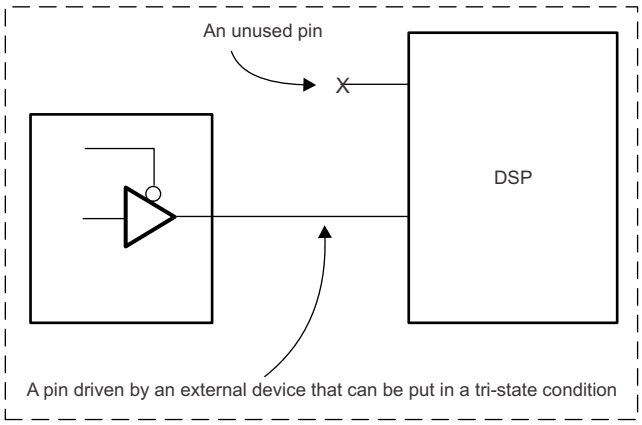

Figure 7. Unused Pins

Conceptually, to avoid the floating input pins, it is easy to just add pull-up or pull-down resistors to the unused input pins. But in real applications, there are some features and techniques that have been integrated into the I/Os of the devices.Section 5 presents the details about the C5000 DSP I/O features and how to use them.

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5 C5000 I/O Pin Functions and Features

In today's applications, high-pin-count devices are often dealt with. The external resistors will increase the area of PCB, and make the PCB design and manufacturing more difficult. More importantly, today's low-power systems are extremely power sensitive; external resistors themselves consume power. To overcome these difficulties and make system design easier, certain features have been added into the device I/O cells.

Two main features that have been integrated into the I/O cells are:

- Internal pull-up or pull-down circuitry: these pull-ups an pull-downs can be controlled by software settings
- Internal bus-holder: this type of circuitry holds a current state of an I/O circuit, either "1" or "0". The current state is determined by the previous driven state.

A typical I/O cell used in C5000 is illustrated in Figure 8.

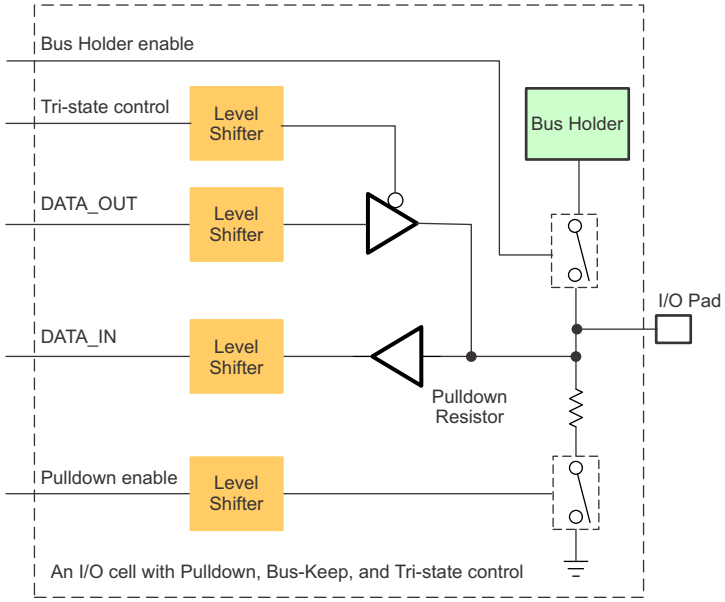

Figure 8. Typical I/O Cell

NOTE:

- Bus-Holder enable signal is controlled by hardware. Only when the C5000 DSP-core is turned OFF, the Bus-Holder will be engaged.
- Tri-state control signal can be controlled by software.
- Pull-down enable signal can be controlled by software.

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To see whether a specific pin has been implemented, see Table 4 and Table 5. These tables list all of the pull-up, pull-down, and bus-holder information for I/O pins of C5000.

Table 4. C55X5 I/Os

Pin Names	PD (1)	PU (1)	BH (1)	Power Domain	Type
EM_CS[0:5]			Y (2)	DVDDEMIF	I/O/Z
EM_D[0:15]			Y (2)	DVDDEMIF	I/O/Z
EM_A[0:14]			Y (2)	DVDDEMIF	I/O/Z
EM_A[15:20]	Y		Y (2)	DVDDEMIF	I/O/Z
EM_BA[0:1]			Y (2)	DVDDEMIF	I/O/Z
EM_OE			Y (2)	DVDDEMIF	I/O/Z
EM_WAIT[2:5]			Y (2)	DVDDEMIF	I/O/Z
EM_WE			Y (2)	DVDDEMIF	I/O/Z
EM_SDCLK			Y (2)	DVDDEMIF	I/O/Z
EM_SDCKE			Y (2)	DVDDEMIF	I/O/Z
EM_DQM1			Y (2)	DVDDEMIF	I/O/Z
EM_R/W			Y(2)	DVDDEMIF	I/O/Z
$\overline{\text{EM\_SDRAS}}$			Y (2)	DVDDEMIF	I/O/Z
EM_DQM0			Y (2)	DVDDEMIF	I/O/Z
$\overline{\text{EM\_SDCAS}}$			Y (2)	DVDDEMIF	I/O/Z
LCD_EN_RDB/SPI_CLK			Y (2)	DVDDIO	O/Z
LCD_CS1_E1/SPI_CS1			Y (2)	DVDDIO	I/O/Z
LCD_CS0_E0/SPI_CS0			Y (2)	DVDDIO	I/O/Z
LCD_RS/SPI_CS3			Y (2)	DVDDIO	I/O/Z
LCD_RW_WRB/SPI_CS2			Y (2)	DVDDIO	I/O/Z
LCD_D[0]/SPI_RX			Y (2)	DVDDIO	I/O/Z
LCD_D[1]/SPI_TX			Y (2)	DVDDIO	I/O/Z
LCD_D[2]/GP[12]	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[3]/GP[13]	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[4]/GP[14]	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[5]/GP[15]	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[6]/GP[16]	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[7]/GP[17]	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[10]/I2S2_RX/GP[20]/SPI_RX	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[11]/I2S2_DX/GP[27]/SPI_TX	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[13]/UART_CTS/GP[29]/I2S3_FS	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[14]/UART_RXD/GP[30]/I2S3_RX	Y		Y (2)	DVDDIO	I/O/Z
LCD_D[15]/UART_TXD/GP[31]/I2S3_DX	Y		Y (2)	DVDDIO	I/O/Z
EMU1		Y	Y (2)	DVDDIO	I/O/Z
EMU0		Y	Y (2)	DVDDIO	I/O/Z
TCK		Y		DVDDIO	I
TDI		Y		DVDDIO	I
TDO (2)			Y (2)	DVDDIO	O/Z
TMS		Y		DVDDIO	I
$\overline{\text{TRST}}$	Y# (2)			DVDDIO	I
XF			Y (2)	DVDDIO	O/Z
MMC0_D0/I2S0_DX/GP[2]	Y		Y (2)	DVDDIO	I/O/Z

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Table 4. C55X5 I/Os (continued)

Pin Names	PD (1)	PU (1)	BH (1)	Power Domain	Type
MMC0_CLK/I2S0_CLK/GP[0]	Y		Y (2)	DVDDIO	I/O/Z
MMC0_D1/I2S0_RX/GP[3]	Y		Y (2)	DVDDIO	I/O/Z
MMC0_D3/GP[5]	Y		Y (2)	DVDDIO	I/O/Z
MMC0_CMD/I2S0_FS/GP[1]	Y		Y (2)	DVDDIO	I/O/Z
MMC1_D1/I2S1_RX/GP[9]	Y		Y (2)	DVDDIO	I/O/Z
MMC1_CLK/I2S1_CLK/GP[6]	Y		Y (2)	DVDDIO	I/O/Z
MMC1_D0/I2S1_DX/GP[8]	Y		Y (2)	DVDDIO	I/O/Z
MMC0_D2/GP[4]	Y		Y (2)	DVDDIO	I/O/Z
MMC1_D3/GP[11]	Y		Y (2)	DVDDIO	I/O/Z
MMC1_CMD/I2S1_FS/GP[7]	Y		Y (2)	DVDDIO	I/O/Z
MMC1_D2/GP[10]	Y		Y (2)	DVDDIO	I/O/Z
GPAIN3				VDD_ANA	Ain/O/Z
GPAIN2				VDD_ANA	Ain/O/Z
GPAIN1				VDD_ANA	Ain/O/Z
GPAIN0				VDD_ANA	Ain/O/Z
RTC_XI				VDD_RTC	AI
RTC_XO				VDD_RTC	AI
WAKEUP				VDD_IO4	I/O/Z
RTC_CLKOUT				VDD_IO4	I/O/Z
SDA				DVDDIO	I/O/Z
CLKIN				DVDDIO	I
$\overline{\text{INT1}}$		Y		DVDDIO	I
CLK_SEL				DVDDIO	I
SCL				DVDDIO	I/O/Z
CLKOUT			Y (2)	DVDDIO	O/Z
$\overline{\text{RESET}}$		Y		DVDDIO	I
$\overline{\text{INT0}}$		Y		DVDDIO	I

(1) PD = Software controllable pull-down integrated; PU = Software controllable pull-up integrated; BH = with bus holder circuit; Y# = means the internal pull-down of $\overline{\text{TRST}}$ pin is always enabled by hardware.

(2) Some of the C55x family of devices do not have EMIF. For information on the available peripherals, see your device-specific data manual.

Table 5. C5517 I/O

Pin Names	PD (1)	PU (1)	BH (1)	Power Domain	Type
EM_CS[0:2]	Y		Y (3)	DVDDEMIF	I/O/Z
EM_D[0:15]	Y		Y (3)	DVDDEMIF	I/O/Z
EM_A[0:14]	Y		Y (3)	DVDDEMIF	I/O/Z
EM_A[15:20] / GP[26:21]	Y		Y (3)	DVDDEMIF	I/O/Z
EM_BA[0:1]	Y		Y (3)	DVDDEMIF	O/Z
EM_OE	Y		Y (3)	DVDDEMIF	I/O/Z
EM_WAIT[2:5]	Y		Y (3)	DVDDEMIF	I
EM_WE	Y		Y (3)	DVDDEMIF	I/O/Z
EM_SDCLK	Y		Y (3)	DVDDEMIF	O/Z
EM_SDCKE/UHPI_HHWIL	Y		Y (3)	DVDDEMIF	I/O/Z
EM_DQM1 /UHPI_HBE1	Y		Y (3)	DVDDEMIF	I/O/Z
EM_R/W	Y		Y (3)	DVDDEMIF	O/Z
EM_SDRAS/UHPI_HAS	Y		Y (3)	DVDDEMIF	I/O/Z

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Table 5. C5517 I/O (continued)

Pin Names	PD (1)	PU (1)	BH (1)	Power Domain	Type
EM_DQM0 /UHPI_HBE0	Y		Y (3)	DVDDEMIF	I/O/Z
EM_SDCAS/UHPI_HCS	Y		Y (3)	DVDDEMIF	I/O/Z
SPI_CLK/UHPI_HINT	Y		Y (3)	DVDDIO	O/Z
SPI_CS1/UHPI_HCNTL1	Y		Y (3)	DVDDIO	I/O/Z
SPI_CS0/UHPI_HCNL0	Y		Y (3)	DVDDIO	I/O/Z
SPI_CS3/UHPI_HRDY	Y		Y (3)	DVDDIO	I/O/Z
SPI_CS2/UHPI_HR_NW	Y		Y (3)	DVDDIO	I/O/Z
SPI_RX /UHPI_HD[0]	Y		Y (3)	DVDDIO	I/O/Z
SPI_TX /UHPI_HD[1]	Y		Y (3)	DVDDIO	I/O/Z
UHPI_HD[2]/GP[12]	Y		Y (3)	DVDDIO	I/O/Z
UHPI_HD[3]/GP[13]	Y		Y (3)	DVDDIO	I/O/Z
UHPI_HD[4]/GP[14]	Y		Y (3)	DVDDIO	I/O/Z
UHPI_HD[5]/GP[15]	Y		Y (3)	DVDDIO	I/O/Z
UHPI_HD[6]/GP[16]	Y		Y (3)	DVDDIO	I/O/Z
UHPI_HD[7]/GP[17]	Y		Y (3)	DVDDIO	I/O/Z
I2S2_CLK/GP[18]/SPI_CLK /UHPI_HD[8]	Y		Y (3)	DVDDIO	I/O/Z
I2S2_FS/GP[19]/SPI_CS0 /UHPI_HD[9]	Y		Y (3)	DVDDIO	I/O/Z
I2S2_RX/GP[20]/SPI_RX /UHPI_HD[10]	Y		Y (3)	DVDDIO	I/O/Z
I2S2_DX/GP[27]/SPI_TX /UHPI_HD[11]	Y		Y (3)	DVDDIO	I/O/Z
UART_RTS/GP[28]/I2S3_CLK/UHPI_HD[12]	Y		Y (3)	DVDDIO	I/O/Z
UART_CTS/GP[29]/I2S3_FS/UHPI_HD[13]	Y		Y (3)	DVDDIO	I/O/Z
UART_RXD/GP[30]/I2S3_RX/UHPI_HD[14]	Y		Y (3)	DVDDIO	I/O/Z
UART_TXD/GP[31]/I2S3_DX/UHPI_HD[9]	Y		Y (3)	DVDDIO	I/O/Z
EMU1		Y	Y (3)	DVDDIO	I/O/Z
EMU0		Y	Y (3)	DVDDIO	I/O/Z
TCK		Y		DVDDIO	I
TDI		Y		DVDDIO	I
TDO (3)		Y		DVDDIO	O/Z
TMS		Y		DVDDIO	I
TRST	Y (2)			DVDDIO	I
XF		Y	Y (3)	DVDDIO	O/Z
MMC0_D0/I2S0_DX/GP[2]/McBSP_DX	Y		Y (3)	DVDDIO	I/O/Z
MMC0_CLK/I2S0_CLK/GP[0]/McBSP_CLKX	Y		Y (3)	DVDDIO	I/O/Z
MMC0_D1/I2S0_RX/GP[3]/McBSP_DR	Y		Y (3)	DVDDIO	I/O/Z
MMC0_D3/GP[5] /McBSP_CLKR_CLKS	Y		Y (3)	DVDDIO	I/O/Z
MMC0_CMD/I2S0_FS/GP[1]/McBSP_FSX	Y		Y (3)	DVDDIO	I/O/Z
MMC1_D1/McSPI_SIMO/GP[9]	Y		Y (3)	DVDDIO	I/O/Z
MMC1_CLK/McSPI_CLK/GP[6]	Y		Y (3)	DVDDIO	I/O/Z
MMC1_D0/McSPI_SIMO/GP[8]	Y		Y (3)	DVDDIO	I/O/Z
MMC0_D2/GP[4] /McBSP_FSR	Y		Y (3)	DVDDIO	I/O/Z
MMC1_D3/GP[11]/McSPI_CS2	Y		Y (3)	DVDDIO	I/O/Z
MMC1_CMD/McSPI_CS0//GP[7]	Y		Y (3)	DVDDIO	I/O/Z
MMC1_D2/GP[10]/McSPI_CS1	Y		Y (3)	DVDDIO	I/O/Z
GPAIN3				VDD_ANA	Ain/O/Z
GPAIN2				VDD_ANA	Ain/O/Z
GPAIN1				VDD_ANA	Ain/O/Z
GPAIN0				VDD_ANA	Ain/O/Z

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Table 5. C5517 I/O (continued)

Pin Names	PD (1)	PU (1)	BH (1)	Power Domain	Type
RTC_XI				VDD_RTC	AI
RTC_XO				VDD_RTC	AI
WAKEUP				VDD_IO4	I/O/Z
RTC_CLKOUT				VDD_IO4	O/Z
SDA				DVDDIO	I/O/Z
CLKIN	Y			DVDDIO	I
$\overline{\text{INT1}}$		Y		DVDDIO	I
CLK_SEL				DVDDIO	I
SCL				DVDDIO	I/O/Z
CLKOUT	Y			DVDDIO	O/Z
$\overline{\text{RESET}}$		Y		DVDDIO	I
$\overline{\text{INT0}}$		Y		DVDDIO	I
EM_CS1/UHPI_HDS2		Y	Y (3)	DVDDEMIF	I/O/Z
EM_CS0/UHPI_HDS1		Y	Y (3)	DVDDEMIF	I/O/Z

(1) PD = Software controllable pull-down integrated; PU = Software controllable pull-up integrated; BH = with bus holder circuit

(2) The internal pull-down of $\overline{\text{TRST}}$ pin is always enabled by hardware.

(3) The bus-holder is enabled only when the DSP core is turned off.

The following sections describe how to use these I/O features in a C5000-based system.

The following procedures detail how to use the I/O feature of a C5000-based system. The goal to prevent the undefined I/Os is:

- If the unused pins are bi-directional I/O pins and they can be configured as outputs, configure them as output and set the corresponding output state to "0" or "1".
- If the unused pins are bi-directional I/O pins and have internal pull-down or pull-up circuitries that can be controlled by software, configure them as input and enable the internal pull-up or pull-down by software.
- If the unused pins are input only and do not have integrated pull-up or pull-down circuitries that can be controlled by software. Then, external pull-up/pull-down resistors are required.

Following are the examples that cover different sceneries on system level.

Case 1: assuming a system only use the low 8-bit LCD interface. Therefore, the pin LCD [8:15] are not used in a system and system level has no external devices to drive them at certain states.

In this case, set the eight pins as inputs and enable internal pull-downs.

```
#define GPIO_DIR1 0x1C07
#define EBSR 0x1C00
#define PDINHIBR3 0x1C19
.
.
.
//set PPmode(EBSR[14:12])="010"LCD, LCD[8:15] become GP[18:20] and GP[27:31]
*(ioport volatile unsigned *)EBSR |= 0x2A00;
//Set the corresponding GPIO as input; 0-input 1-output
*(ioport volatile unsigned int *)GPIO_DIR1 = 0x07E3;
//enable the internal pull-down
*(ioport volatile unsigned *)PDINHIBR3 &= 0x00FF;
```


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Case 2: After the system software has been developed and debugged, usually the JTAG port will not have been used. Yet, some of the JTAG pins may be floating without external drivers; this could cause higher power-consumption or inconsistency in power-consumption across the devices. The example below illustrates how to set the unused JTAG port in a defined state.

```
#define PDINHIBR2 0x1C18
.
.
.
//set EMU0/EMU1/TDI/TMS/TCK, EMU0 and EMU1 share the same enable bit
*(ioport volatile unsigned *)PDINHIBR2 &= 0xF0FF;
```

For the TDO pin, although it is an output pin, in C5000 when it is not being used, it will be in tristate mode and the I/O cell could become a floating input pin. Also, since there is no software controllable pull-up/down circuit for the TDO pin, the last option: an external resistor should be used to pull this pin "High".

6 Summary

To summarize the low-power design best practices for C5000 that has been discussed in this document.

- Choose the right device voltage for your system; change them through software based on the application.
- Choose the right frequency for the active mode of your application
- Run the device at very low frequency, such as RTC frequency, while in non-active mode. By doing this, you can also turn OFF the PLL completely.
- Configure all the I/O pins to the correct states, no input and hi-z pins should be left floating.
- Utilize internal pull-up/pull-down to reduce external components and to save power.

7 References

- *TMS320C5515 DSP System User's Guide* (SPRUFX5)
- *TMS320C5517 Fixed-Point Digital Signal Processor Data Manual* (SPRS727)
- *TMS320C5517 Digital Signal Processor Technical Reference Manual* (SPRUH16)

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