# Peak Current Control Realization for Boost Circuit Based On C2000™ MCU

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# 1 Introduction

The peak current mode is widely used in a switching power supply application. Peak current mode can be easily implemented by analog controllers, such as UC3845. This type of control shows good performance not only in stability, but also in dynamic response. However, this control is seldom realized by the digital controllers. Additionally, peak current mode requires a mechanism to implement the slope compensation; the majority of the MCUs on the market do not meet this demand.

The Piccolo series microcontroller (MCU) from TI has embedded analog comparators that can be connected to its on-chip ePWM module. Also, the slope compensation unit is on-chip. This makes the Piccolo MCU a suitable digital controller to realize peak current mode control without any external component. This application report discusses the implementation of peak current control mode for the boost circuit using the TMS320F28027 MCU.

# 2 The Peak Current Mode Principle

## 2.1 The PWM Duty Generation in Peak Current Mode

In voltage control mode or the average current mode, the MCU calculates the PWM duty. But in peak current control mode, the PWM trip result generates the duty cycle.
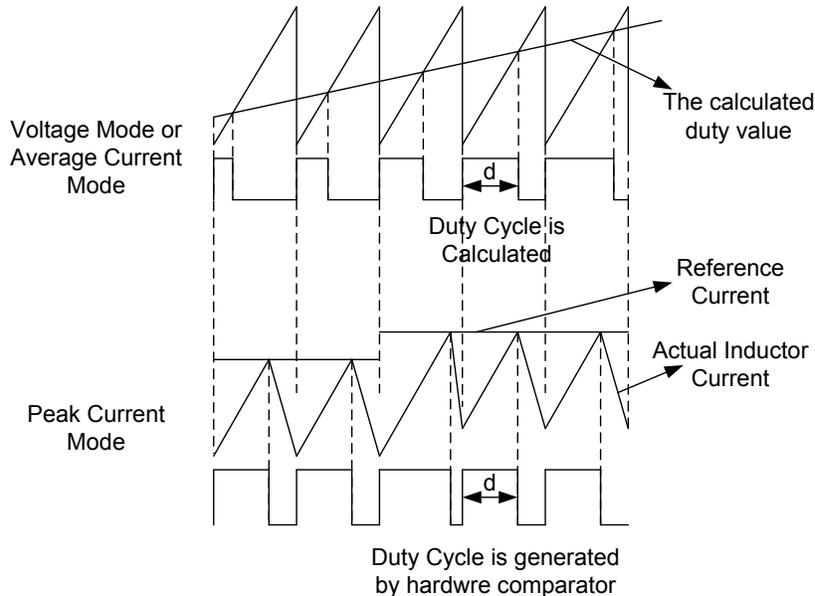


**Figure 1. PWM Generation in Peak Current Mode**

At the beginning of each PWM cycle of the peak current mode, the PWM turns on, and the inductor current increases. A reference inductor current occurs when the inductor current increases to the reference current. The PWM trips off, which is usually done by the analog comparator, then the PWM duty cycle is generated. To regulate the duty cycle, the reference current must be calculated.

## 2.2 The Slope Compensation

To resist the noise or the load disturbance, the slope compensation must be used in the application when the duty cycle exceeds 50%. Figure 2 shows the reason.
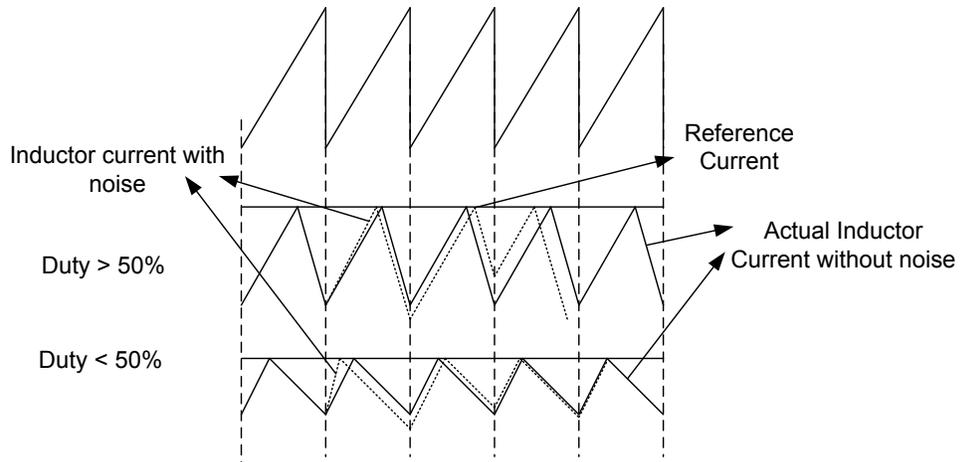


**Figure 2.    Noise Changes in Different Duty Cycle**

When the duty cycle exceeds 50%, a disturbance in the inductor current causes a change in the PWM duty cycle. The effect becomes increasingly larger until the entire system is unstable.

To increase the immunity to the disturbance of the control system, the slope compensation is used (see Figure 3).
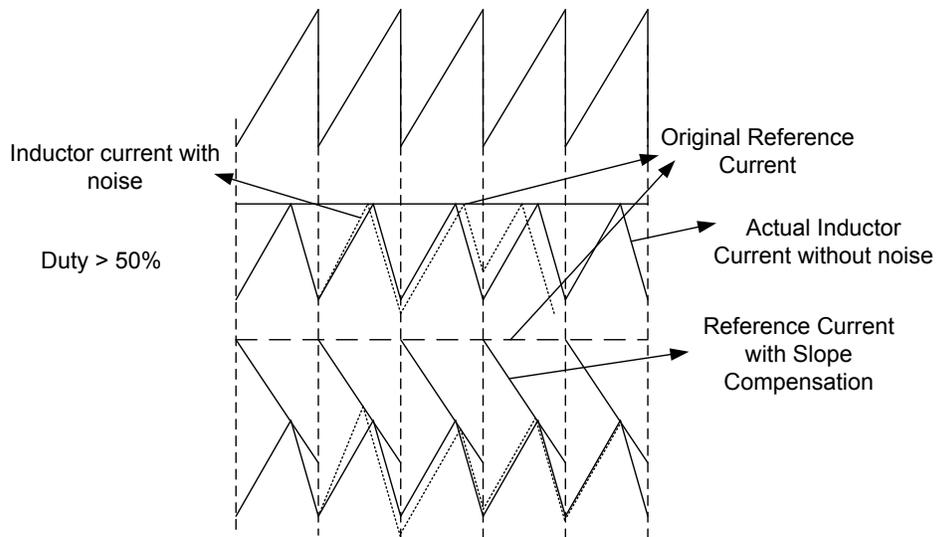


**Figure 3.    Noise Changes After Slope Compensation**

After the slope compensation in every cycle, the noise effect can be eliminated after several cycles. Assume the slope is $k_{slope\_comp}$, the inductor increase slope is $k_1$, and the decrease slope is $k_2$. According to the experience, if the slope must satisfy the following equations to stabilize the system.

$$| k_{slope\_comp} | > 0.5 | k_2 | \tag{1}$$

For the boost topology

$$| k_2 | = \frac{V_o - V_{in}}{L} \tag{2}$$

So

$$| k_{slope\_comp} | > \frac{V_o - V_{in}}{2L} \tag{3}$$

From Equation (3) we can get the slope compensation ratio, which ensures the stability of the peak current control when the duty cycle exceeds 50%.

# 3    Peak Current Mode by Using C2000

## 3.1    On-chip Comparator

In the Piccolo series MCU in the C2000 family, there is an analog comparator with an internal 10-bit digital-to-analog converter (DAC).  One input of the comparator is connected to the ADC input pin, and the other inverting input of the comparator can be set to be connected to the ADC input pin or to the internal 10-bit DAC. Most importantly, the output of the comparator can be input to the ePWM module as a trip source, which can simulate the PWM generation action of the peak current mode.
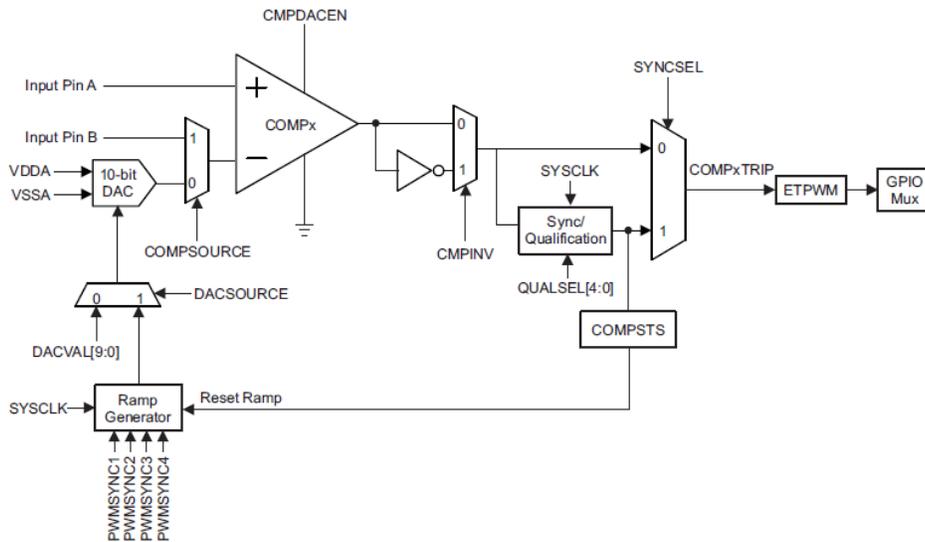


**Figure 4.    Block Diagram of the Internal Comparator**

Aside from the basic comparator, a ramp generator is connected to the 10-bit DAC. The ramp renerator is a count-down counter; the step and the start time can be set by software. So, the value of the 10-bit DAC will be affected by both the DACVAL register and the ramp generator.

## 3.2 Build Up the Peak Current Mode Mechanism

### 3.2.1 Setting the MCU

To realize the peak current mode, the ePWM in the C2000 must be set up to cooperate with the internal comparator. The following key points of the setup must be pay attention to.

- The PWM output mode must be the asymmetrical mode.

- The Digital Compare in ePWM must be enabled.

- The DCxEVT2(x = A,B) must be used due to the CBC event can be effective only for DCxEVT2.

- The clock of the internal comparator must be enabled.

- If the duty cycle exceeds 50%, the RAMP unit must be enabled.

- The inverting input of the internal comparator must be set to the internal DAC.

### 3.2.2 The Voltage Loop Controller

The control block diagram of peak current control is the same as that of average current mode (see Figure 5). The difference is that the internal comparator does the internal loop of peak current mode.
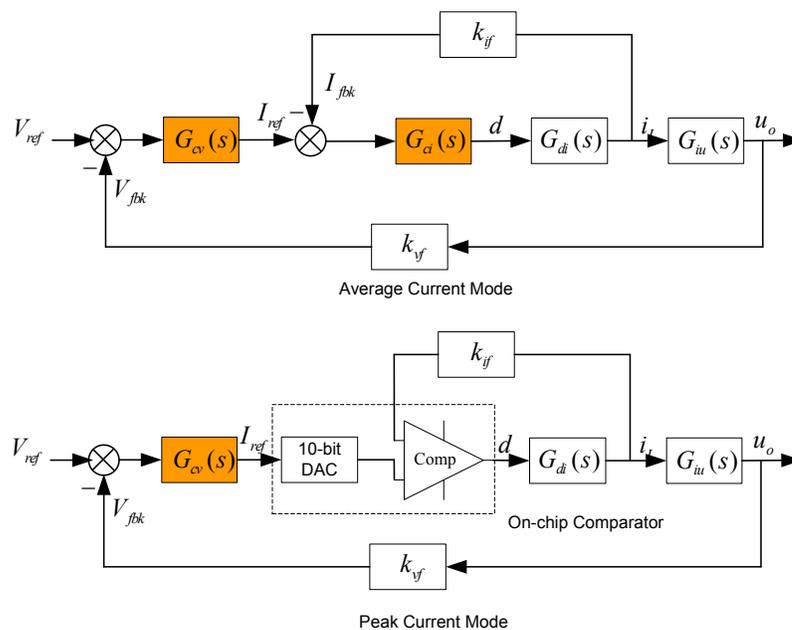


**Figure 5. Control Block Diagram**

For peak current mode control, only the voltage loop controller must be designed.

### 3.3 Implementation for the Boost

This application note uses the following boost circuit parameter:

$$L = 32uH , C = 140uF , V_{in} = 24V , u_o = 50V , R = 25\Omega , f_{sw} = 300kHz , k_{yf} = 0.0144$$
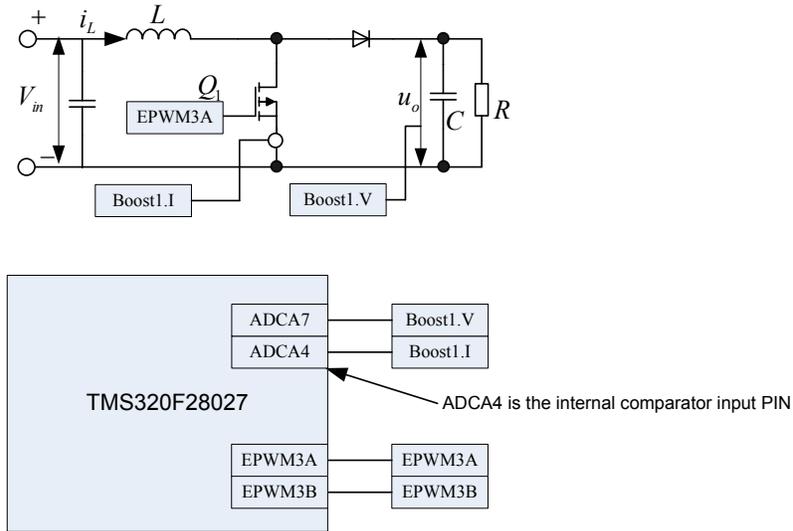


**Figure 6.  Block Diagram of the Implementation**

Using the Piccolo A MCU as the main controller, the EPWM3A is the PWM output pin and the IGBT current is sampled as the inductor current. Also, output voltage is also sampled to design the voltage loop.

In peak current mode, software only needs to calculate the voltage loop, after which the reference current is determined. The reference current is written to the internal 10-bit DAC to let the comparator finish the current loop process. At the same time, the RAMP ratio must be updated when the reference current is changed.

The voltage loop and the slope compensation are executed every three cycles in ISR.
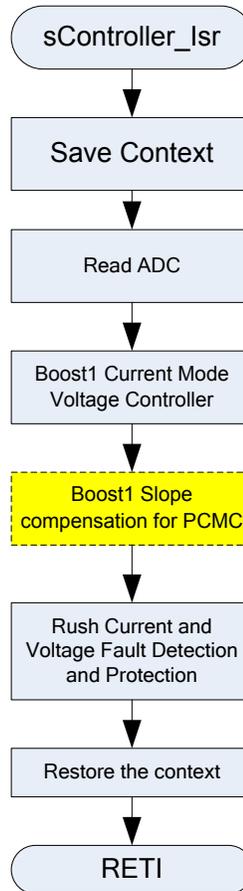
**Figure 7.    Software Flow Chart in ISR**

# 4    Test Result

The test result indicates that using the C2000 MCU helps peak current mode attain a very good performance. In addition, peak current mode is realized easily for boost and buck circuits or for some equivalent topologies.
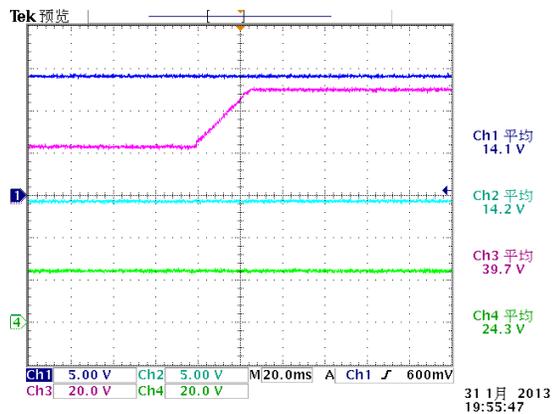


**Figure 8.    Output Voltage Soft Start Test**
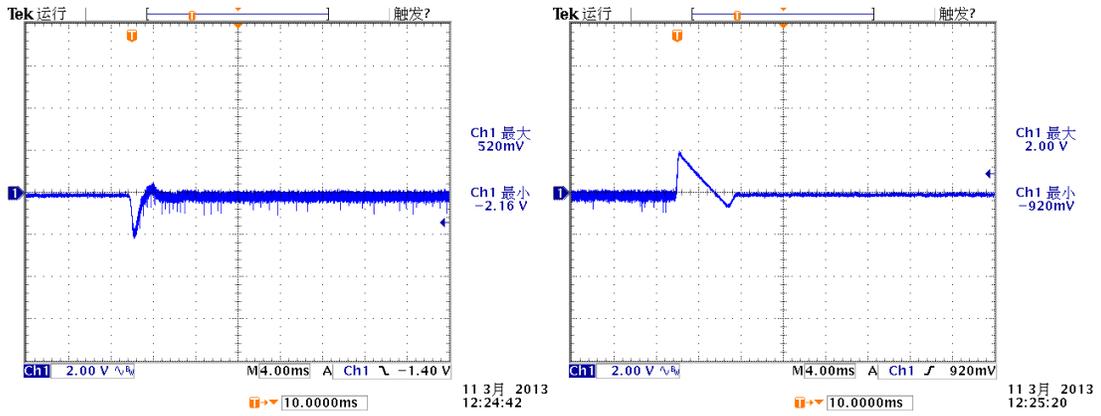
**Figure 9.    Load Step Transient Test (Full Load)**

# Appendix A. Reference Code

## A.1 ePWM Initialization Code

```
if((n == 1) || (n == 3))

 {

        EALLOW;

        if(n == 1) //For buck

        {

          //Config the digital compare unit

          // Define an event (DCAEVT2) based on DC_COMP1OUT

            (*ePWM[n]).DCTRIPSEL.bit.DCAHCOMPSEL = DC_COMP1OUT;       // DCAL = Comparator 1 output

        }

        else //For boost

        {

            (*ePWM[n]).DCTRIPSEL.bit.DCAHCOMPSEL = DC_COMP2OUT;       // DCAL = Comparator 2 output


        }



        (*ePWM[n]).TZDCSEL.bit.DCAEVT2 = TZ_DCAH_HI;           // DCAEVT2 =  DCAH high(will become active as
Comparator output goes high)

        (*ePWM[n]).DCACTL.bit.EVT2SRCSEL = DC_EVT2;             // DCAEVT2 = DCAEVT2(not filtered)

        (*ePWM[n]).DCACTL.bit.EVT2FRCSYNCSEL = DC_EVT_ASYNC;       // Take async path



        // Enable DCAEVT2 is CBC trip sources

        // Note: DCxEVT1 events can be defined as one-shot.

        // DCxEVT2 events can be defined as cycle-by-cycle.

        (*ePWM[n]).TZSEL.bit.DCAEVT2 = 1;

         EDIS;

 }
```

## A.2 Comparator Code

```
Comp2Regs.COMPCTL.bit.COMPDACEN = 1;    //The comparator is powered up

Comp2Regs.COMPCTL.bit.SYNCSEL = 0x1;  //Synchronous version

Comp2Regs.COMPCTL.bit.QUALSEL = 0x2;  //3 clocks

Comp2Regs.COMPCTL.bit.CMPINV = 0x0;   //pass through

Comp2Regs.COMPCTL.bit.COMPSOURCE = 0x0; //The inverting input is internal DAC


Comp2Regs.DACCTL.bit.DACSOURCE = 1;    //Internal ramp

Comp2Regs.DACCTL.bit.RAMPSOURCE = 3;   //EPWM3 is the ramp source

Comp2Regs.RAMPDECVAL_SHDW = 0;        //Initial slope

EPwm4Regs.HRPCTL.bit.PWMSYNCSEL = 1;   //The PWMSYNC is CTR = 0;

Comp2Regs.DACVAL.bit.DACVAL= 1000;           //3.3A

Comp2Regs.RAMPMAXREF_SHDW = (UINT16)(1024<<6);
```

## A.3 Slope Compensation Code

```
;-------------------------------------------------------------------------

;Macro Name: mSlope_Com

;Description: The slope compensation of the PCMC

;Parameter:

;       n: The comparator number

;       _Ref: The reference current Q24

;       _Com_Ratio: The slope compensation ratio

;-------------------------------------------------------------------------

mSlope_Com          .macro    n,_Ref,_Com_Ratio

;=========================

; Set up address pointers
```

```
MOVL    XAR0,#_Ref                              ; Net pointer for InA (XAR0)

MOVL    XAR1,#_Comp:n:Regs.RAMPMAXREF_SHDW      ; pointer to Comparator Ramp Max Ref (XAR1)

MOVL    XAR2,#_Comp:n:Regs.DACVAL                      ; pointer to Comparator Ramp Dac Val (XAR2)

MOVL    XAR3,#_Comp:n:Regs.RAMPDECVAL_SHDW; Output for DACn

MOVL    XT,*XAR0

MOVW    DP,#_Com_Ratio

QMPYL   ACC,XT,@_Com_Ratio      ;ACC = upper16(Q24*Q24) = Q16

MOVL    *XAR3,ACC        ;_Comp:n:Regs.RAMPDECVAL_SHDW = ACC


MOVL    ACC,*XAR0              ; Q24

SFR     ACC,#8                 ; Q16 because Maximum RAMPMAXREF = 0xFFFF

MOV     *XAR1,AL        ; Output value to RAMPMAXREF

LSR     AL, #6          ; Q10 to be written to DACVAL

MOV     *XAR2,AL        ; Output value to DACVAL


.endm
```

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