Application Report
SPRABT6 – August 2013

Different Control Mode for Synchronization Buck or Boost Topology by Using C2000™ MCU

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1 Introduction

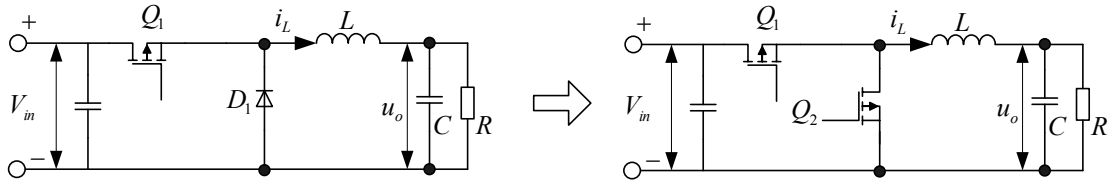
The buck and the boost circuits are the most commonly used topology in nonisolated DC-DC application. The buck circuit is used as step-down converter, while the boost is used as step-up converter. While the buck and boost circuits are critical for the simple DC-DC conversion field, they are also highly important to other power electronics topologies. The reason is that most power converter topologies can be considered as the equivalent circuit consisting of buck and boost converters. Therefore, the analysis and the controller design for these two circuits are very typical. By improving the efficiency of conversion, the synchronized buck and boost have become increasingly popular.

This document discusses the closed-loop controller design for synchronized buck and boost circuit, both in voltage mode and the average current mode. A Piccolo MCU named TMS320F28027 in the C2000 family is used as the digital controller. To realize a high PWM frequency (300 kHz), the application of HRPWM in TMS320F28027 is also shown.

2 The Mathematical Model

The first step in designing the closed-loop controller for the synchronization buck or boost topology is to build up the mathematical model. The synchronization buck or boost topologies are derived from the traditional buck and boost circuit by replacing the diode with a MOSFET. This replacement reduces the conduction loss of the switches.

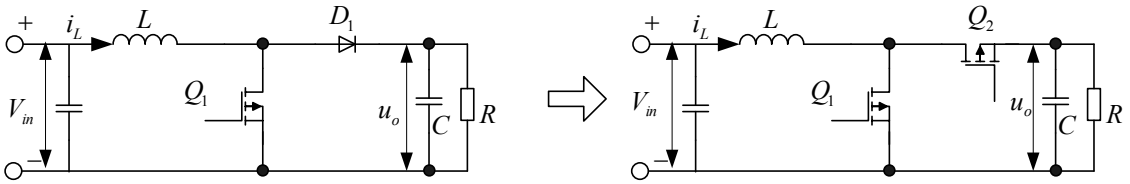
As shown in Figure 1 and Figure 2, the control for the synchronization circuits requires a pair of complementary PWMs. To avoid the short circuit of the two switches, the dead time between the two switches is necessary.



(a) Traditional Buck

(b) Synchronization Buck

Figure 1. Buck Circuit



(a) Traditional Boost

(b) Synchronization Boost

Figure 2. Boost Circuit

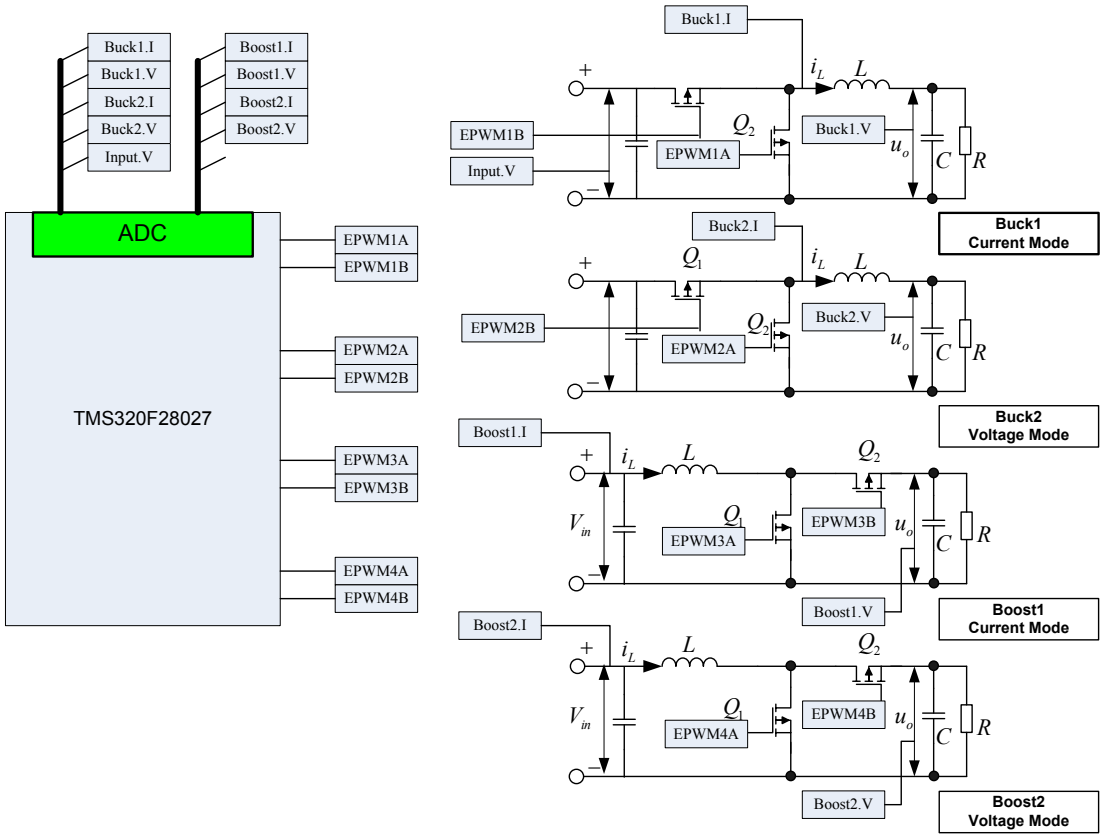


Figure 3. Block Diagram of the System

In this paper, we use one microcontroller unit (MCU) to control four converters, which is two bucks and two boosts (see Figure 3). One buck is controlled in voltage mode, and the other in current control mode. The boost control mode is the same as that of the buck.

Before building up the model, the following parameters should be assumed:

1. The input voltage is V_{in}, and the output voltage is u_o.
2. The inductor current is i_L, and the resistor load is R .
3. The inductance is L, and the output capacitance is C.
4. The duty cycle is d .

2.1 The Small Signal Model for Buck

When the Q1 is on, we can get equation (1).

$$\begin{cases} L\dfrac{di_L}{dt} = V_{in} - u_o \\ C\dfrac{du_o}{dt} = i_L - \dfrac{u_o}{R} \end{cases} \tag{1}$$

When the Q1 is off, we can get equation (2)

$$\begin{cases} L\dfrac{di_L}{dt} = -u_o \\ C\dfrac{du_o}{dt} = i_L - \dfrac{u_o}{R} \end{cases} \tag{2}$$

In each switching cycle, by combining equations (1) and (2) with the average space principle, equation (3) is derived.

$$\begin{cases} L\dfrac{di_L}{dt} = dV_{in} - u_o \\ C\dfrac{du_o}{dt} = i_L - \dfrac{u_o}{R} \end{cases} \tag{3}$$

So, equation (4) shows the average duty cycle of the buck circuit in stable status.

$$d_{avg} = \frac{u_o}{V_{in}} \tag{4}$$

In a very short time range, considering the d , i_L and the u_o as the fixed value, by adding the small signal $\hat{d}$, $\hat{i}_L$ and $\hat{u}_o$ to equation (3), we can get equation (5), which is the small signal function of the buck.

$$\begin{cases} L\dfrac{d\hat{i}_L}{dt} = (d+\hat{d})V_{in} - (u_o + \hat{u}_o) \\ C\dfrac{d\hat{u}_o}{dt} = (i_L + \hat{i}_L) - \dfrac{(u_o + \hat{u}_o)}{R} \end{cases} \tag{5}$$

Assume $\hat{u}_o$ = 0 and $\hat{d}$ = 0, respectively.

$$\begin{cases} L\dfrac{d\hat{i}_L}{dt} = \hat{d}V_{in} \\ C\dfrac{d\hat{u}_o}{dt} = \hat{i}_L - \dfrac{\hat{u}_o}{R} \end{cases} \tag{6}$$

So, equation (7) shows the small signal model transfer function from duty cycle d to the inductor current i_L .

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{in}}{Ls} \tag{7}$$

Equation (8) shows the transfer function from the duty cycle d to output voltage u_o .

$$G_{du}(s) = \frac{\hat{u}_o}{\hat{d}(s)} = \frac{RV_{in}}{Ls(RCs+1)} \quad (8)$$

Equation (7) can be used in current loop design in current mode, and equation (8) can be used in voltage mode controller design.

2.2 The Small Signal Model for Boost

From the same method that used in Section 2.1, we can get the small signal model of the boost.

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_o}{Ls} \quad (9)$$

$$G_{du}(s) = \frac{\hat{u}_o}{\hat{d}(s)} = \frac{(1-d_{avg})RV_o}{Ls(RCs+1)} \quad (10)$$

$$d_{avg} = \frac{u_o - V_{in}}{u_o}$$

3 The Voltage Mode Controller Design

Voltage mode control controls the output voltage by a single output voltage loop, and the controller simply regulates the duty cycle in different running conditions. For example, consider the buck topology (see Figure 4 for the voltage mode closed-loop block diagram):

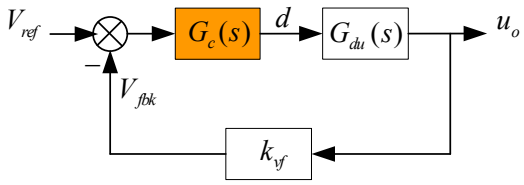


Figure 4. The Voltage Mode Control Block Diagram

Equation (11) shows the open-loop transfer function:

$$G_{open} = G_c(s)G_{du}(s)k_{vf} \quad (11)$$

The $G_c(s)$ is the closed-loop controller, and the k_{vf} is the voltage sampling ratio.

From equation (8) we can see that $G_{du}(s)$ has a low-frequency pole that greatly affects the frequency response of the system by slowing down the bandwidth and reducing the phase margin. To reduce the effect of this pole, it must be a zero to offset it.

So it is better to choose a controller as follows:

$$G_c(s) = \frac{K(s+a)(s+b)}{s(s+c)} \tag{12}$$

$a = \frac{1}{RC}$ is an offset zero to the pole of the $G_{du}(s)$.

b is a high-frequency zero to compensate the phase, and c is a high-frequency pole to reduce the high-frequency noise. Besides, we need an integral element to reduce the static difference of the controller.

In practice, the buck circuit parameter follows:

$L = 32uH$, $C = 460uF$, $V_{in} = 24V$, $u_o = 14V$, $R = 7\Omega$, $f_{sw} = 300kHz$, $k_{vf} = 0.0532$

If equation (13) shows the closed-loop controller:

$$G_c(s) = \frac{5(s+\frac{1}{RC})(s+4500)}{s(s+35000)} = \frac{5(s+322)(s+4500)}{s(s+35000)} \tag{13}$$

Figure 5 shows the frequency response of the open-loop system.

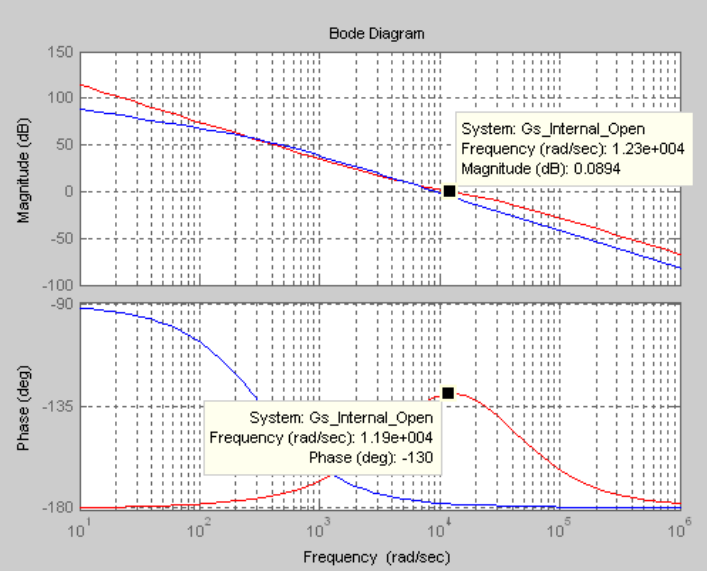


Figure 5. Voltage Mode Open-Loop Response for Buck

In Figure 5, the blue line is the $G_{du}(s)$ frequency response, and the red line is the open loop frequency response after it is controlled. The system is stable because the phase margin is approximately 50 degrees. Besides, the bandwidth is about 12300 rad/s, so the dynamic response can be ensured.

Equation (14) is the continuous function of the voltage loop controller. For the digital controller, we need to make it discrete to the z-domain with a sampling time of 20 µs.

$$G_{cz}(z) = \frac{5 - 9.652z^{-1} + 4.654z^{-2}}{1 - 1.497z^{-1} + 0.497z^{-2}} \quad (14)$$

By using the same method, we can also design the voltage mode controller for boost. In practice, the boost circuit parameter follows:

$L = 32uH$, $C = 140uF$, $V_{in} = 24V$, $u_o = 50V$, $R = 25\Omega$, $f_{sw} = 300kHz$, $k_{vf} = 0.0144$

If equation (15) and equation (16) show the closed-loop controller:

$$G_c(s) = \frac{8(s + \frac{1}{RC})(s + 8000)}{s(s + 45000)} = \frac{8(s + 286)(s + 8000)}{s(s + 45000)} \quad (15)$$

$$G_{cz}(z) = \frac{8 + 15.123z^{-1} + 7.128z^{-2}}{1 - 1.407z^{-1} + 0.407z^{-2}} \quad (16)$$

Figure 6 shows the frequency response of the open-loop system.

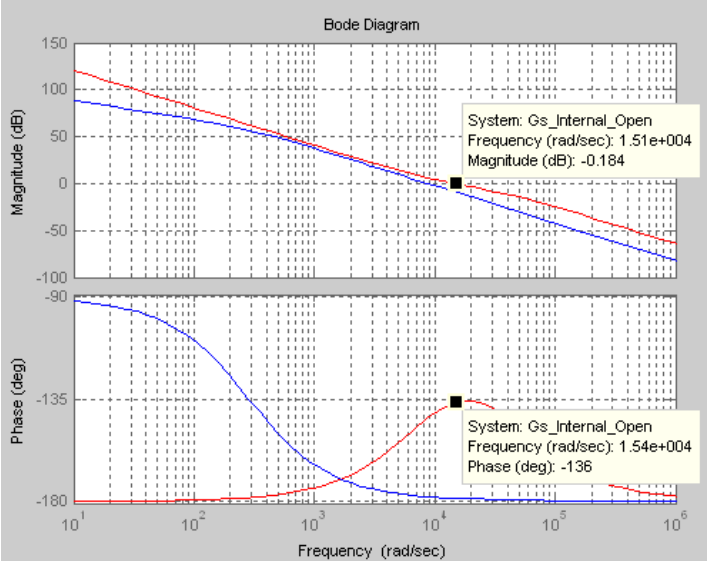


Figure 6. Voltage Mode Open-Loop Response for Boost

4 The Current Mode Controller Design

Current mode control means to regulate the output voltage by internal current loop and an external voltage loop controller. The inductor current and the output voltage are controllable in an external voltage loop controller. Figure 7 shows the current mode control block diagram.

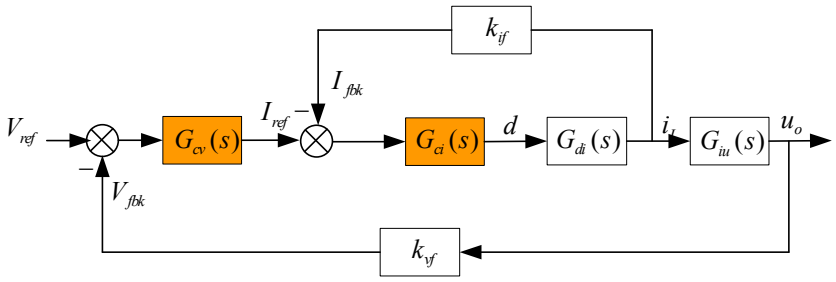


Figure 7. Current Mode Control Block Diagram

When designing the multiloop system, the most important factor is the design of the current loop controller for the system. Also, the internal loop must be designed first. From Figure 7, we can get the internal open-loop transfer function is:

$$G_{open\_i} = G_{ci}(s)G_{di}(s)k_{if} \tag{17}$$

The internal loop object is the transfer function from the duty cycle to the inductor current $G_{di}(s)$. From the preceding analysis, this object is integral. To regulate this kind of object, the PI controller can be used.

$$G_{ci}(s) = \frac{K(s+b)}{s(s+a)} \tag{18}$$

Equation (18) reflects a PI controller that adds a high-frequency pole, which can reduce the high-frequency noise of the system.

If the designed internal loop is fast enough, the internal loop of the system can be considered as a gain, so the external loop object is similar to the integral, and the PI controller can be used for the external loop.

$$G_{cv}(s) = \frac{K(s+b)}{s(s+a)} \tag{19}$$

To ensure the stability of the system, the internal loop must be much faster than the external loop. Therefore, it is necessary to choose the proper bandwidth for both current loop and voltage loop. In the 300-kHz switching frequency application, a 60-MHz MCU cannot execute a 1-cycle controller algorithm because the CPU speed is not fast enough to finish the calculation for the controller in 3.3 µs. In addition, the sampling delay in the closed loop, which greatly reduces the phase margin of the system, cannot be neglected. So, we must reduce the sampling rate and the controller execution rate to reduce the CPU load and the effect of the sampling delay.

In practice, we use a 100-kHz sampling frequency to execute the controller algorithm to update the duty cycle every 10 µs for the internal loop. Considering the delay by the CPU calculation and sampling delay, a bandwidth less than 10 kHz is proper and safe for the internal loop, and a bandwidth less than 2 kHz is proper and safe for the external loop.

Given the same parameters for buck mentioned in the previous section, if we choose the following current loop and voltage loop, the internal open-loop frequency response and the external open-loop frequency can be gained (see Figure 8 and Figure 9, respectively).

$$G_{ci}(s) = \frac{20000(s+20000)}{s(s+140000)} \tag{20}$$

$$G_{cv}(s) = \frac{200000(s+2500)}{s(s+15000)} \tag{21}$$

The discretion for equations (20) and (21) with the sampling time of 10 µs is:

$$G_{ciz}(z) = \frac{0.06471 + 0.01176z^{-1} - 0.05294z^{-2}}{1 - 1.1765z^{-1} + 0.1765z^{-2}} \tag{22}$$

$$G_{cvz}(z) = \frac{3.546z^{-1} - 3.347z^{-2}}{1 - 1.741z^{-1} + 0.741z^{-2}} \tag{23}$$

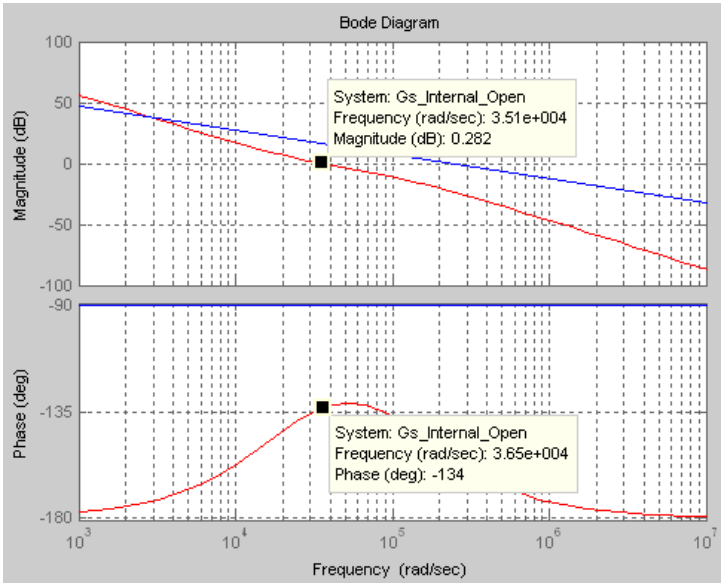


Figure 8. Internal Open-Loop Frequency Response

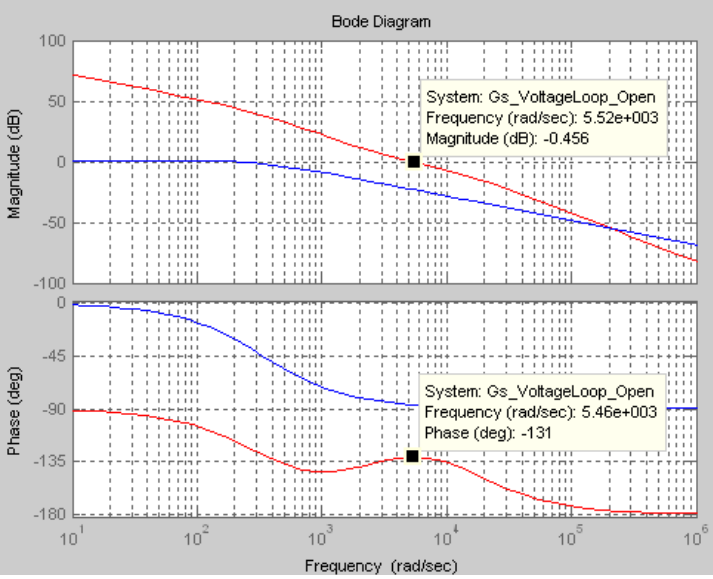


Figure 9. External Open-Loop Frequency Response

Using the same method, the similar result can be attained for current control mode for the boost circuit. In this paper, the current mode controller design is not shown, and the controller for boost is shown below:

$$G_{ci}(s) = \frac{24000(s+20000)}{s(s+140000)} \tag{24}$$

$$G_{cv}(s) = \frac{240000(s+3000)}{s(s+21000)} \tag{25}$$

5 The HRPWM Application Notes

In this paper, the 300-kHz switching frequency is applied for both buck and boost circuit. For a 60-MHz CPU, the PWM duty step for a CPU clock is 0.5%. If the input voltage is 24 V, the voltage regulation step of the controller will be 0.12 V, which is too rough to get fine control for the output voltage. So the HRPWM is needed in a high-switching frequency field.

5.1 The Principle of the HRPWM Module

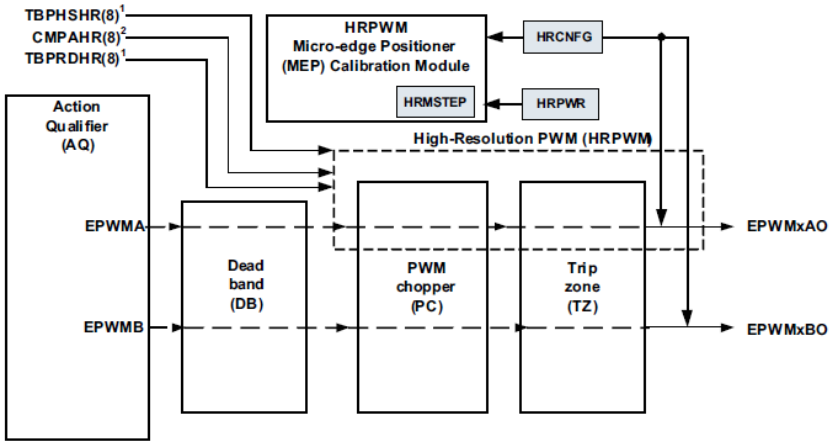


Figure 10. The Block Diagram of HRPWM

The HRPWM uses the TBPHSHR, CMPAHR, and TBPRDHR to fine-tune PWM edge in a single CPU clock cycle. The single CPU clock time can then be divided into several MEP steps. For a 60-MHz MCU, the typical MEP step is 150 ps. In this paper, the CMPAHR is used to generate the high-resolution duty cycle. However, from Figure 10, we cannot realize the high-resolution dead-time.

In the EPWM module, CMPA contains traditional PWM, 16-bit CMPA, and an 8-bit high-resolution CMPAHR.

5.2 CMPAHR Calculation

For a given duty cycle d, two methods can be used to calculate the value of CMPAHR.

1. Calculate the CMPAHR by the following equations:

CMPA = d × TBPRD;

CMPAHR = (frac(d × TBPRD) × MEP_ScaleFactor + 0.5) << 8;

The MEP_ScaleFactor must be updated in the background by calling the SFO() function. All the steps are performed by software.

2. Set the HRPWM running in auto-conversion mode: then software calculates the fraction of the duty cycle, and hardware finishes the other process automatically. MEP_ScaleFactor must update in the background by calling the SFO function. In this mode:

CMPA = d × TBPRD;

CMPAHR = frac(d × TBPRD<<8);

In this paper, the auto-conversion mode is used.

6 Test Result and Conclusion

6.1 The Voltage Mode Test

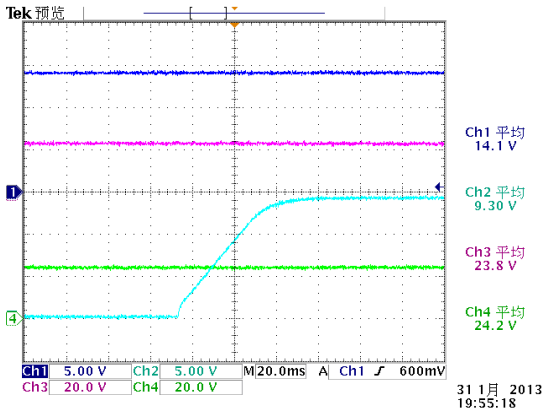


Figure 11. Buck Voltage Mode Soft Start Test

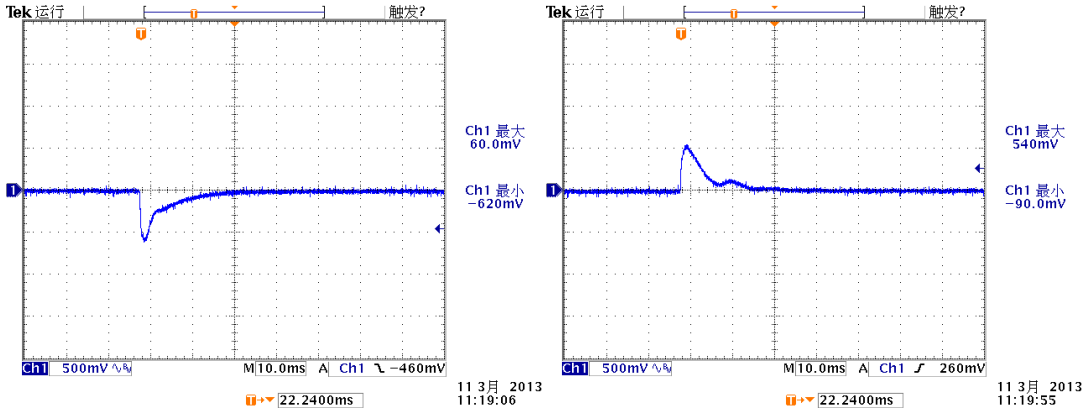


Figure 12. Buck Voltage Mode Load Step Test

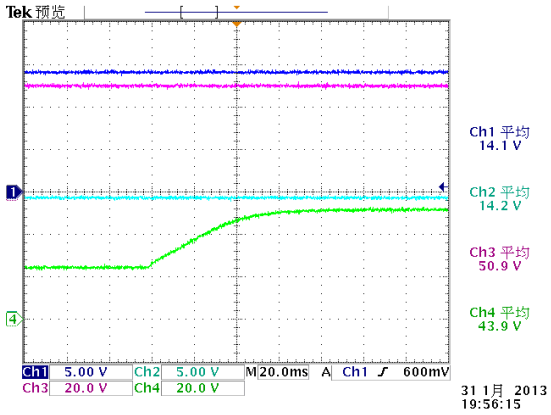


Figure 13. Boost Voltage Mode Soft Start Test

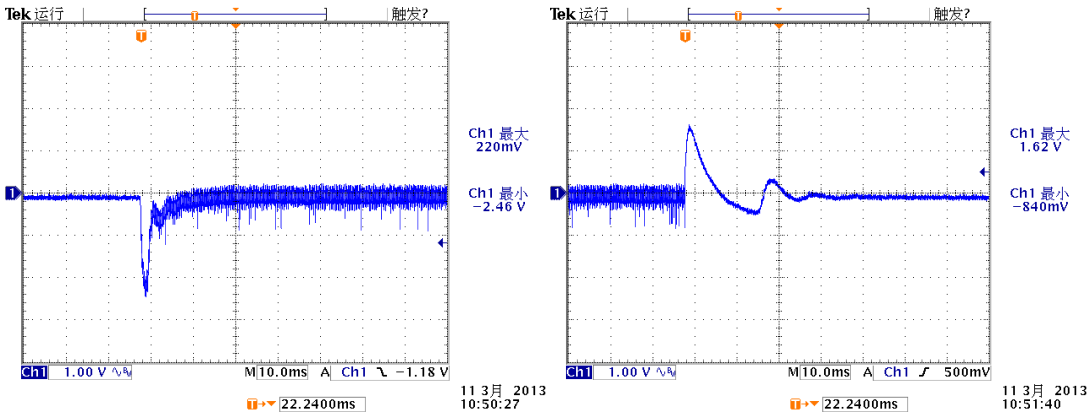


Figure 14. Boost Voltage Mode Load Step Test

6.2 The Current Mode Test

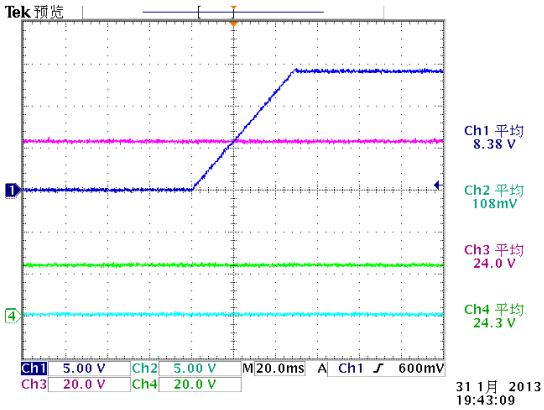


Figure 15. Buck Current Mode Soft Start Test

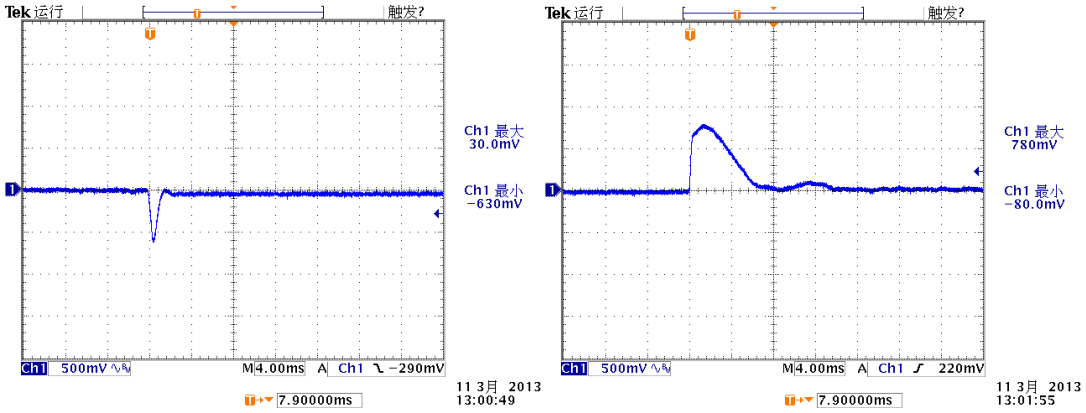


Figure 16. Buck Current Mode Load Step Test

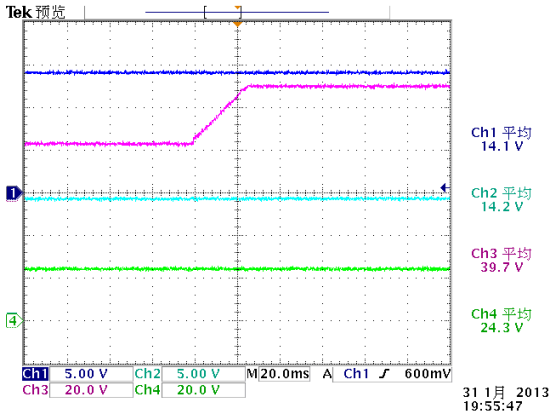


Figure 17. Boost Current Mode Soft Start Test

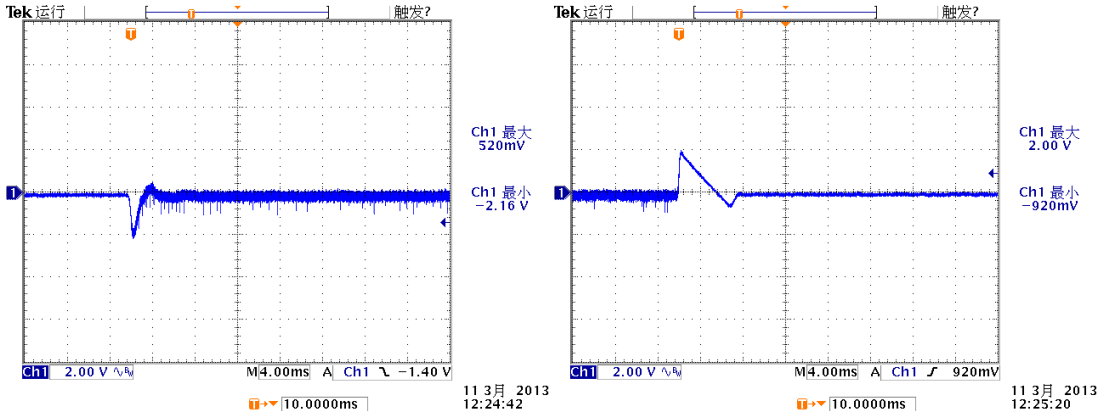


Figure 18. Boost Current Mode Load Step Test

6.3 Conclusion

In this paper, four channels of buck and boost circuit are controlled by only one Piccolo A MCU. The Piccolo A MCU shows very good performance in the 300-kHz switching frequency application field.

From the preceding test results, all the buck and boost converters show good performance both in a soft start process and the dynamic response. All of the load step voltage pulldowns and pullups can be controlled to less than 5% of the rated output voltage. But when comparing the voltage mode to the current mode, the current mode has the better load disturbance recovery performance.

7 References

1. *TMS320F2802x data sheet,* SPRS523G

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