Application Report
SPRABB3–June 2010

PCB Design Guidelines for 0.5mm Package-on-Package Applications Processor, Part I

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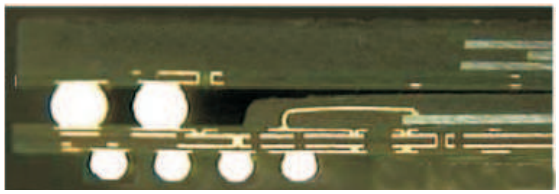
ABSTRACT

Ball grid array (BGA) packages having 0.5mm ball pitch require careful attention to printed circuit board (PCB) design parameters to successfully yield reliable and robust assemblies. PCBs with package-on-package (PoP) technology have additional assembly requirements and options that need to be considered when designing the PCB.

Fine-pitch PCB design is a team effort and may require more than a common list of design rules. Close coordination and communication between component supplier, PCB designer, PCB fabricator, and PCB assembly vendor is mandatory.

The following factors have a major effect on the quality and reliability of PCB assembly: pad design, via-in-pad (VIP) guidelines, via finishing, stencil design, solder paste requirements, solder paste deposition, and reflow profile. This application report provides a starting point for estblishing a set of design guidelines. It is strongly recommended that you perform actual studies in conjunction with your PCB assembly vendor and PCB fabricator to optimize the process.

Figure 1. Applications Processor (bottom device) and PoP Memory (top device) Stack Up on PCB



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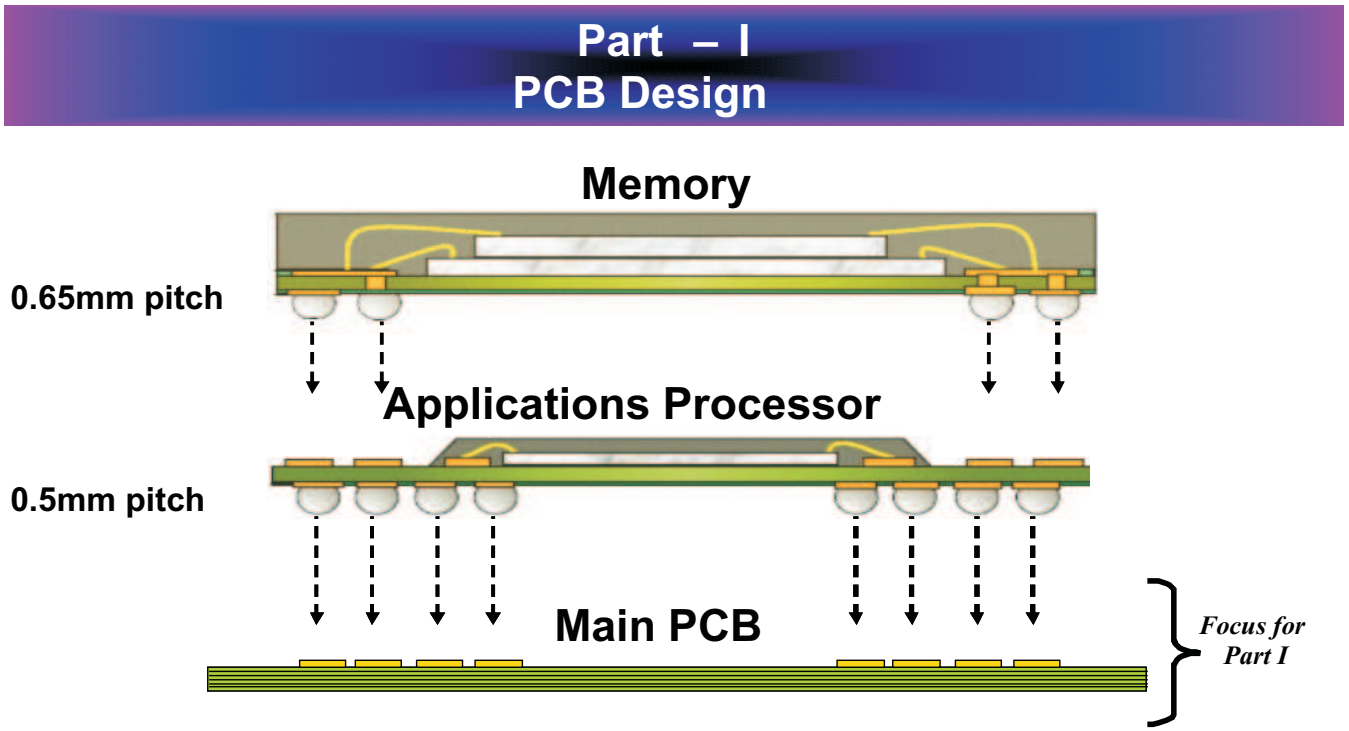
1 Introduction

This application report focuses on PCB design guidelines specific to the CBC package, with 0.5mm pitch, using PoP technology. Experience has shown that PCB design is the most crucial aspect of a design that contains PoP technology due to the extremely small pad pitches. Also, not all assembly vendors can build such small pitch assemblies or properly mount the memory on top of the applications processor.

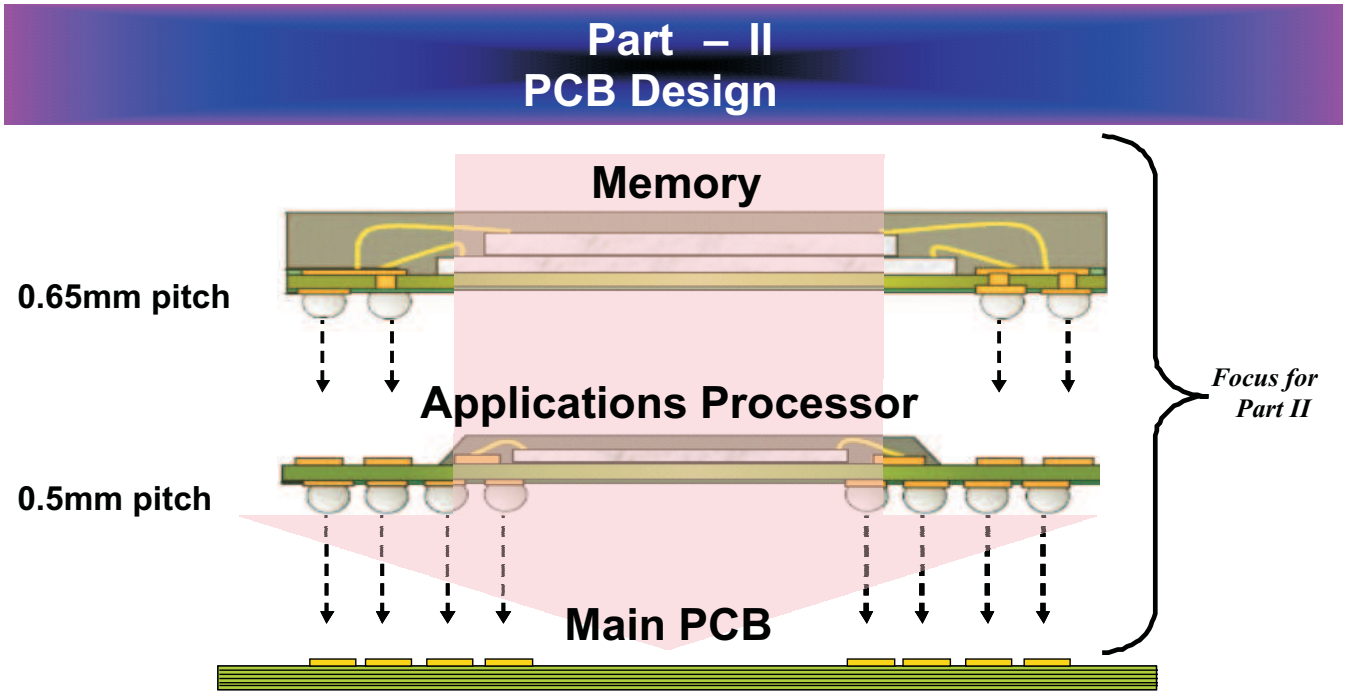
Figure 2 shows a 0.5mm pitch processor and its matching memory at 0.65mm pitch.

Figure 2. Part 1 - Focus for Part I - PCB Design



Guidelines for the assembly of PCBs that use PoP technology are covered in the companion article to this document, *PCB Assembly Guidelines for 0.5mm Package-on-Package Applications Processor Part II* (SPRABA8), which is referred to as Part II throughout the remainder of this document. Included are assembly options and suggestions to use when qualifying and working with your assembly vendors.

Figure 3. Focus for Part II - PoP Assembly



2 Scope of These Guidelines

This document discusses the BGA package and the main PCB immediately below the BGA. The guidelines do not cover all aspects of PCB design.

Since this is a rapidly evolving technology, spend some time reading recently published articles, papers, and company presentations on all aspects of fine-pitch PCB design.

A common theme emerged as this paper was developed – long standing “rules” for PCB design are no longer applicable at these small geometries.

The emergence of the theme came about as a result of many meetings among the different suppliers and designers. The meetings included representatives from four major team players of high yielding PoP design: PCB designers, PCB fabricators, component suppliers, and assembly vendors. Also, an extensive literature review was conducted and appropriate references are included at the end of this paper.

You should plan on performing your own experimental layouts and prototype runs before committing to volume production. Based on your findings, you’ll discover that your suppliers can handle the device or you may have to change PCB fabricators and/or find assembly vendors with better equipment.

3 Design For Manufacturability

The increasing focus on Design For Manufacturability (DFM) has resulted in expanding the scope of traditional design activities in order to identify and eliminate manufacturing problems during the design stage. DFM is as much a system as it is a task.

Although PCB design incurs only a small fraction of the total product cost, the decisions made during the PCB design phase determines the cost of the product over its life-cycle and can be crucial to the success or failure of the finished assembly.

In DFM all of the design goals and manufacturing constraints are considered simultaneously and analyzed. Such analysis can identify design elements that pose problems for manufacturing and suggest changes in the design to address these problems.

There are many ways to design a good PCB and the ideas presented here must be considered only as recommendations.

4 Teamwork

Everyone involved in the design, fabrication, and assembly of complex, fine-pitch PCBs must work together as a team to achieve low-cost and reliable products. The days of tossing circuit diagrams over the cubical wall to the PCB designer who then tosses them to the assembly vendor are gone. Most PCB designs being done today require a team approach and the entire process, from component selection to assembly, requires careful coordination.

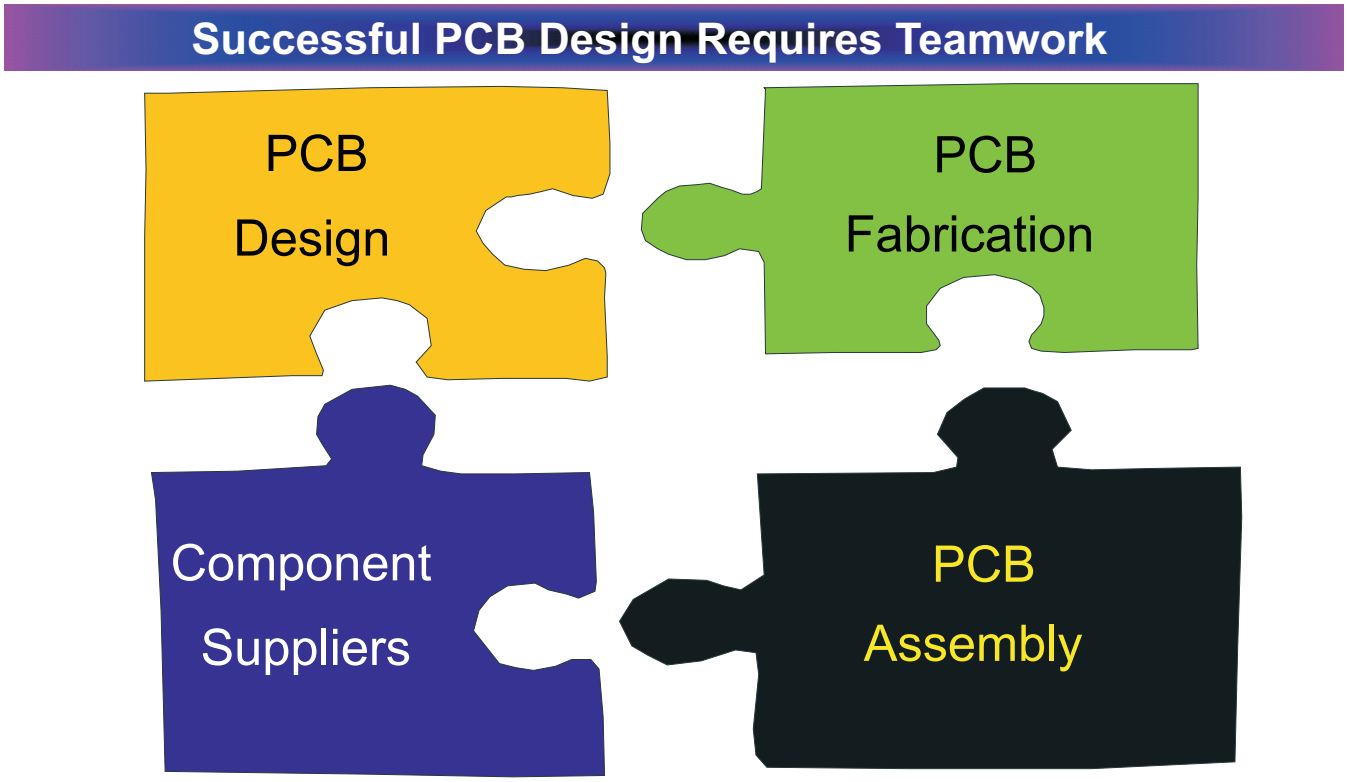
The typical team is composed of members from four sub-teams that represent the four major steps in product fabrication: the component supplier (semiconductors, passives, mechanical, etc.), the PCB designer, the PCB fabricator, and the PCB assembly vendor. In some cases there may be additional members or some members may do more than one job.

Each of the team members brings their own experiences and design guidelines to bear on the task. As a result, it is not uncommon to find conflicting guidelines. These conflicts must be resolved prior to the start of work. Unresolved conflicts will result in poor assembly yields at best or 100% failure at worst. Constant and frequent communication is the key to resolving conflicts and everyone must be in the loop.

Get to know your team members and be sure to have frequent meetings as the project proceeds from design through production. It will be money and time well spent.

A good relationship with the other members of your team assures that your company does not have to be the expert in all of these areas. Calling on the expertise of the rest of your team assures the best possibility of a manufacturable design.

Figure 4. Teamwork Needs for PCB Design



Failure to include the fabrication and assembly team members can prove costly since choices made early in the design will adversely impact the final cost and reliability of the assembled PCB.

5 Be Wary of Quotes

PCB fabrication cost estimates vary widely. One of the largest contributors to unit price is the quantity of PCBs being built in the production run.

Several PCB design and layout options may be provided on the quote with various pricing options that offer a lower price. However, the lower price assumes a relatively large number of PCBs are being fabricated. For smaller volumes, or for prototyping, the cost may be the same or even higher for some of these options.

Obtain several quotes and be wary of quick quotes that seem out of line. When this occurs, the PCB fabricator providing an out of line quote may classify your PCB design as advanced technology by their standards causing a relatively high quote compared to other PCB fabricators that classify your PCB design as standard technology. Press them hard for ways to lower the cost. Also be careful of quotes that are much lower than others. This may occur when a PCB fabricator does not understand the complexity of your PCB design.

6 Do Not Forget Your CAD Tools

Review the microvia capabilities of your CAD system. Blind microvias open up routing channels on the inner layers. Therefore, your CAD system must be capable of handling blind and buried microvias as well as through-hole vias. Your system's features and setup dictates the difficulty or ease with which the PCB will route. Some of the setup parameters include via size, span, and a whole slew of clearance rules. Most CAD vendors offer specialized training on high-density interconnects and fine-pitch BGA PCBs. Talk to them – they are also part of your design team.

Your CAD tool may have capabilities to automatically check your design for common DFM parameters; take advantage of these capabilities. Each CAD platform is different and has different capabilities. For example, the Altium PCB design rules checking section spans more than 119 pages. Your particular CAD platform will have various checks and tests that can be performed on the finished PCB design. Learn what these checks and tests do, and use them to verify your PCB design.

7 Metric Vs English

Using the metric system is one of the most common complaints about fine-pitch PCB design. Most designers dislike this simply because all of their familiar rule-of-thumb guidelines are in the English system. It is strongly suggested that you set the grid in your CAD system to micrometers (μm) and do away with the four decimal places of accuracy needed to represent small features in the English system. This will also aid in layout for metric footprints when using the "copy" style commands. Otherwise the lack of accuracy in translation can cause design rule check (DRC) violations.

8 PCB Fabrication Limits

Most PCB fabricators publish a table that indicates their limitations for various parameters like drill size, trace width, aspect ratio, etc. In many cases, these parameters may have more restrictive limitations when you consider other dependencies which result from one or two dominate characteristics of the PCB design. What this means is that there are tradeoffs and options for the PCB designer to consider. Always consult with your PCB fabricator for their limits and capabilities and remember that as you approach the limit of their equipment, yields go down and costs go up. As an example, we will describe a fabricator's technology and capabilities:

Standard Technology— Usually means this is the middle of the fabricator's capability and pricing. The technology does not push the limits of the fabricator's equipment. Our example fabricator may list a minimum trace width and clearance of 3 mils with 4 mil vias and 10 mil pads for standard technology.

High Yield Technology— Loosens up the specifications to provide more clearance and wider traces resulting in lower cost per unit PCB and higher yields. Our example fabricator may list a minimum trace width and minimum clearance of 4 mils with 4 mil vias and 10 mil pads for high yield technology. However, a PCB built using high yield technology may be larger and require more layers.

Engineering Development Technology— Really pushes the fabricator's capabilities to the limits of their equipment. Our example fabricator may list a minimum trace width and minimum clearance of 2.5 mils with 3 mil vias and 9 mil pads for engineering development technology. Do not make the mistake of thinking these limits can be used for production. The cost will be high and the yield may not be good.

9 Routing and Layer Stackup

One huge benefit of PoP is the elimination of the high-speed, balanced transmission lines between the processor and memory. The external memory's data and control lines no longer have to be routed out from under the processor. This is a huge savings in both time and the number of layers. For these reasons, OEMs have quickly adopted PoP as their applications processor package of choice. This also impacts your pad and layer stackup decisions.

A customer does not need to worry about PCB design requirements for external high-speed DDR memory when using PoP because this interconnect is not part of the main PCB design.

It is possible to use a 6-layer PCB and route all of the connections without requiring via in pad technology. There are several suitable layer stackups.

Layer 1	Signal (Top Copper)
Layer 2	Signal
Layer 3	Ground
Layer 4	Power
Layer 5	Signal
Layer 6	Signal (Bottom Copper)

If the stackup above is used, great care must be taken to minimize cross talk between the outside 2 layers on both the top and the bottom. Also, signals must still adhere to the impedance recommended in the respective component data sheet (45-65 ohms in most cases), so care must be taken to allow the traces to have a reference plane for impedance control.

Another popular stackup, shown below, allows for sensitive clock signals or relatively high speed lines to be routed between power planes.

Layer 1	Signal (Top Copper)
Layer 2	Ground
Layer 3	Signal - high speed
Layer 4	Signal - high speed
Layer 5	Power
Layer 6	Signal (Bottom Copper)

Another recommended stackup.

Layer 1	Ground with pad cutouts
Layer 1	Signal – high speed
Layer 3	Signal - high speed
Layer 4	Power
Layer 5	Ground
Layer 6	Signal (Bottom Copper)

At first it would seem that using ground as the top layer would not be efficient. Once the designer realizes that this reduces vias by ~30% (because of the number of pins connected directly to ground) and therefore promotes great routing efficiency on the second layer, the advantage is seen. Several high density interconnect (HDI) experts have used ground as the top layer and recommend this practice. This stackup also provides reduced EMI.

In addition to layer stackups, package footprints and pad stacks are the next important item to consider. Proper definitions and strict adherence to clearance will play a key role in the development of high yield PoP designs

10 Applications Processor Package

Familiarity with the basic dimensions of the applications processor package is helpful. This section discusses the key parameters of the CBC package.

Figure 5. Applications Processor CBC Package Specification Details

Package size	**14x14 mm**
Package designator	**CBC**
Solder ball chemistry	**LF35**
	[98.25Sn, 1.2Ag, 0.5Cu, 0.05Ni]
A Ball pitch (bottom)	**500um**
B Ball diameter	**250um min to 350um max**
C PAD pitch (top)	**650um**
D PAD diameter	**300um**

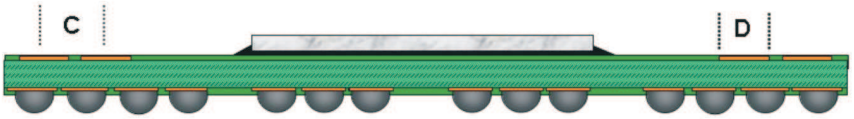
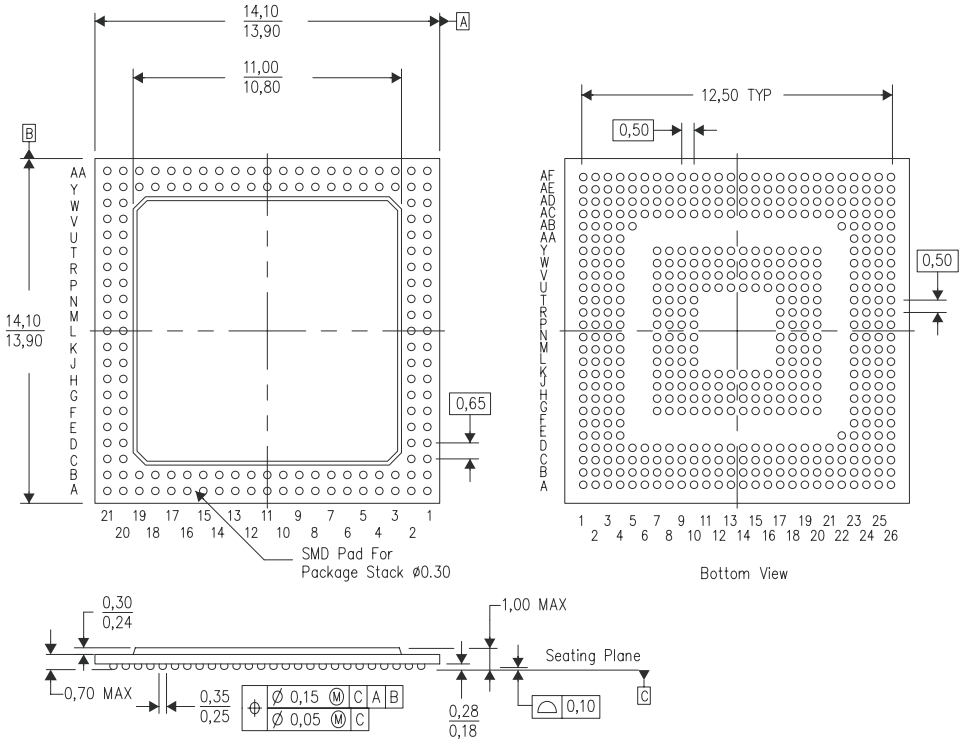


Figure 6. Applications Processor CBC Package Drawing



11 Applications Processor Power/Ground

There are a lot of power and ground pins on the applications processor. Decoupling capacitors are required and must be placed as close as possible to the ball connection. When selecting a power and a ground, choose the ground closest to the power pin for each decoupling capacitor. A single decoupling capacitor can serve up to 3 balls if placed closely to them.

Review the applications processor datasheet for power assignments and recommended decoupling capacitor values.

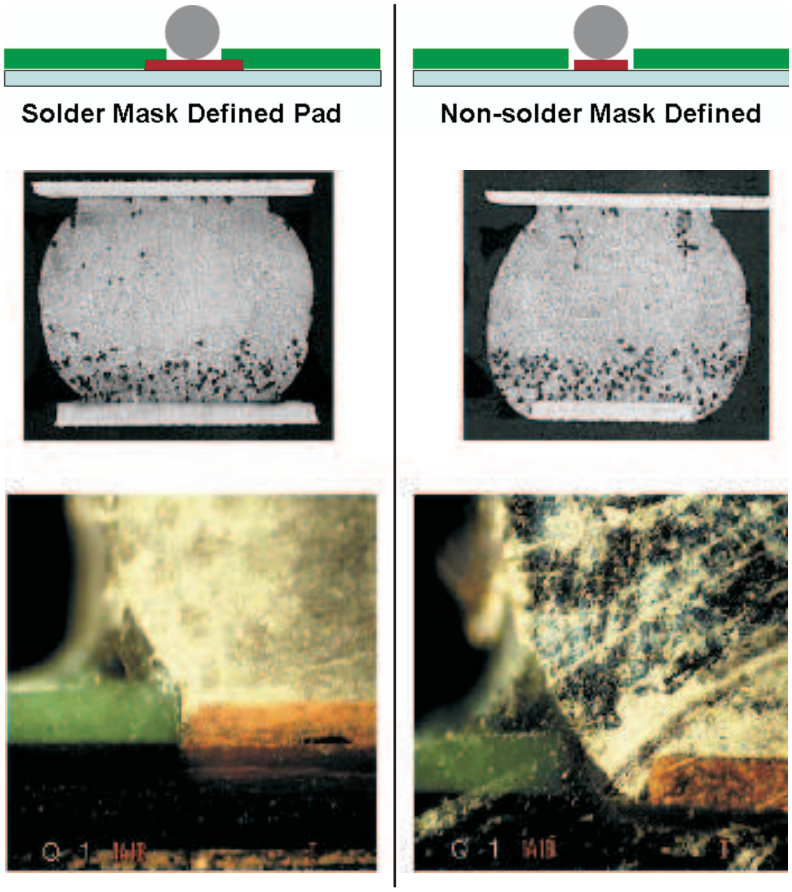
This paper will show the location of the decoupling capacitors for an example EVM module later.

12 Pad Type

Before getting into the specific details, it is important to understand the pros, cons, and unknowns concerning the two most common types of solder pads, solder-mask-defined (SMD) and non-solder-mask-defined (NSMD) pads.

Industry reliability studies have revealed that NSMD-type pads are highly recommended for most 0.5mm pitch PCB designs. They have the advantage of tighter copper dimensions, compared to solder mask dimensions, and the uniform coverage is better at the solder melting temperature. The pads are also smaller, allowing for improved routing. Another advantage of the NSMD pad is reduced stress concentrated on the solder joint, which increases solder joint reliability especially if paste overprinting is used. This concept will be covered later in a section that discusses solder stencil design.

Figure 7. Solder-Mask-Defined (SMD) and Non-Solder-Mask-Defined (NSMD) Pads



However, there are some companies that swear by SMD pads claiming that the greater copper area (of the pad) and the solder-mask overlap create better adhesion strength to the fiber/glass laminate. They claim that flexing and bending during accelerated thermal cycling testing causes a weak link where the pad attaches to the PCB and could be the main failure location, as opposed to the typical solder fracture which dominates the NSMD pad.

Be sure and talk to your PCB fabricator and your PCB assembly vendor and discuss their experiences and preferences before deciding which type of pad will be used on your PCB design.

13 PCB Dimensions for 0.5mm Pitch with Routing Track

Through several meetings with both PCB fabricators and PCB assembly vendors, the following recommendation has been created for the PCB BGA footprint of the applications processor having 0.5mm or 500 μm, pitch solder balls. The pattern shown in Figure 8 assumes there will be traces between solder pads on the top layer.

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad according to several industry studies. In addition, there is additional “grip” area around pad edge as previously described.

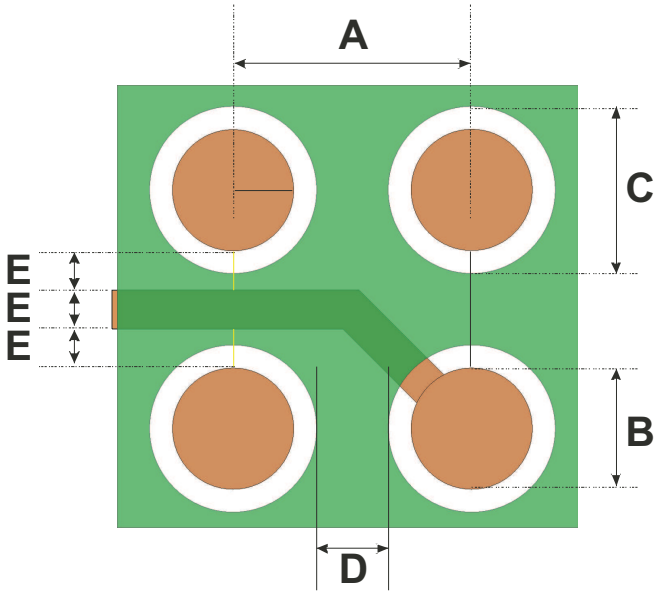
According to IPC (an industry association for PCB manufacturing) standards IPC-7351A, the most reliable design is a NSMD pad which has a diameter that is slightly smaller than the solder ball. For a ball size of 0.3mm, the IPC 7351A standard recommends a .25mm pad (~10 mils).

This will allow the use of a 82um (3.2mil) trace between pads, yet preserve 82um (3.2 mil) clearance between pads and traces. Some vendors suggest a 3.0mil trace (75um) with a 3.3mil (83um) clearance.

Finally, the suggested clearance around the pad for the solder mask opening is about 50um (2mil).

Pad Type	NSMD	
Pad Pitch	A	500μm (~20mils)
Pad Size	B	250μm (~10mils)
Mask Shape	Round	
Mask Opening	C	50μm around pad (350μm antipad for the 250μm pad)
Mask Web	D	150 μm
Trace Allowed Between	Yes	3.2mil trace maximum
Trace Width	E	82 μm (~3.2mil)
Pad to Trace Clearance	E	82 μm (~3.2mil)

Figure 8. PCB Pad Dimensions for 0.5mm Pitch Packages - Top Layer



14 PCB Dimensions for 0.5mm Pitch with Via

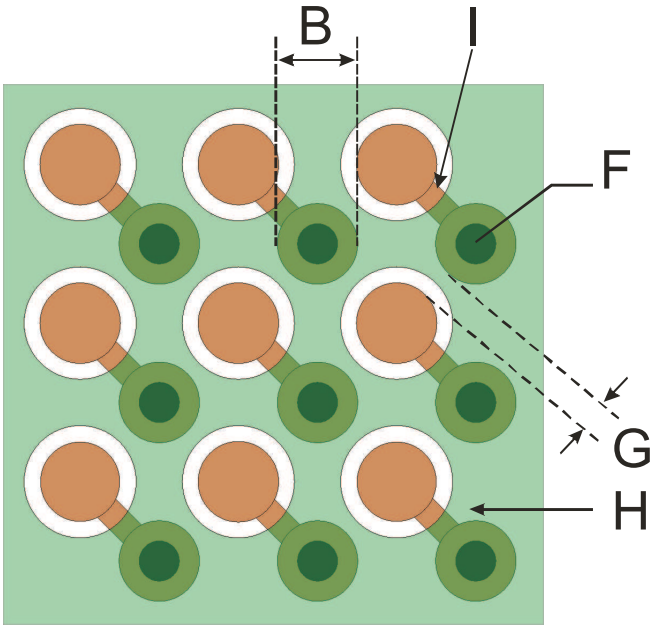
When you want to use vias to drop down to lower layers, the following technique is commonly used. At the 0.5mm pitch, there is sufficient space between pads to allow for a via that has the same dimension as the package ball pad. The pad and via are connected with a 200um wide trace. The pattern shown in Figure 9 shows how vias are used to connect solder pads on the top layer to subsequent layers.

For this size via, PCB fabricators will use a laser drill. Be sure and verify that your facility can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

This type of via is referred to as an “offset via” and is very robust. Note that the via is completely covered by the solder mask. This prevents short circuits during paste application, allows for paste overprinting (discussed later) and prevents etch entrapment.

Pad Type	NSMD	
Pad Pitch	A	500μm
Pad Size	B	250μm (~10mils)
Via pad size	B	254μm
Via drill size	F	127μm (5mil)
Pad to Via clearance	G	72μm
Pad to Via Trace	H	82μm wide (~3.2mil)
Length of Connecting Trace	I	354μm pad center to pad center

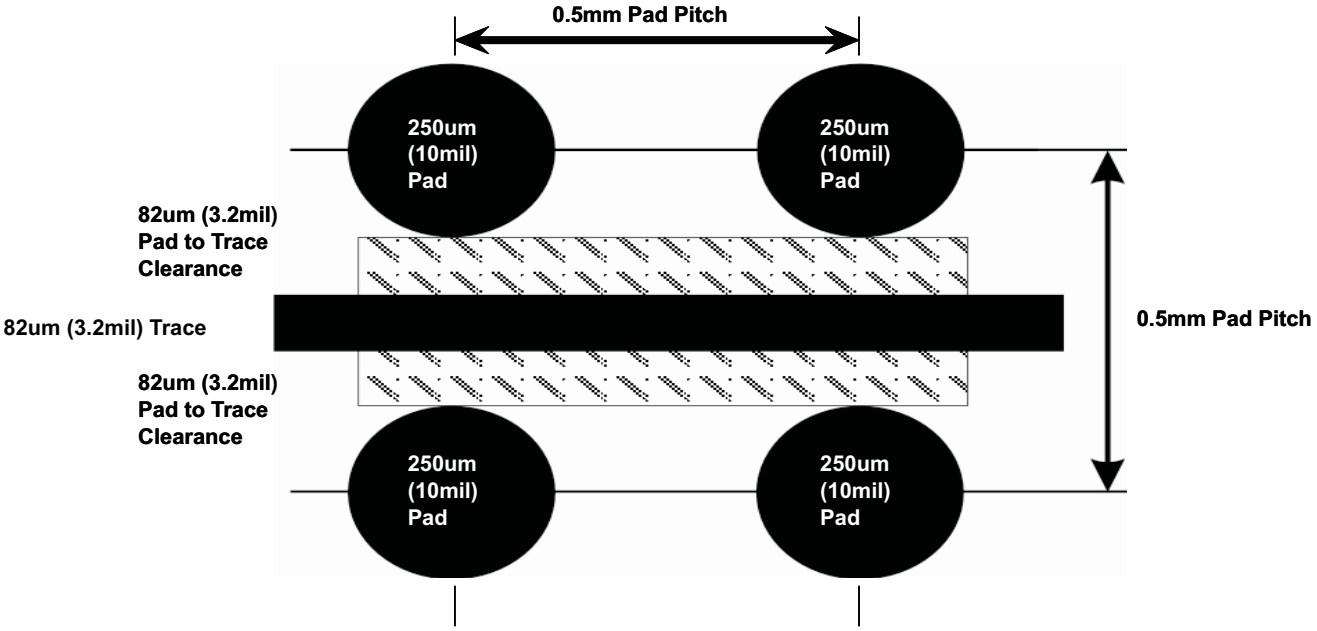
Figure 9. PCB Via Dimensions for 0.5mm Pitch Packages - Top Layer



15 Line Widths and Clearances

Top layer routing between 0.5mm pitch solder balls, can be accomplished if the pad size is no larger than 250um (10mils). This will allow a single trace, 82um (3.2mils) wide, with 82um (3.2mils) clearance between pad and trace. These are generic guidelines and should be used for the layer on which the 0.5mm BGA package is mounted. Most high quality PCB fabricators should have no problem if 82um (3.2mils) is used as the minimum clearance between pads, traces and combinations of both.

Figure 10. Line Width Figure



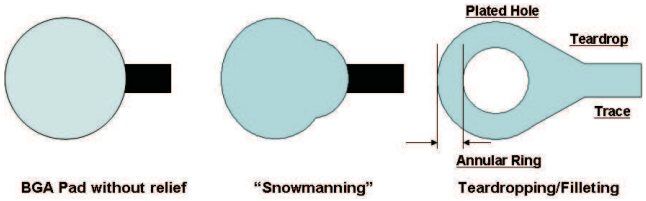
16 Teardrop and Snowman Pads

Teardrops should be used when traces exit the pad whether it is a solid pad or a pad with a via. One way of creating teardrops is to add secondary pads at the junction of an existing (primary) pad and the trace, sometimes called a “snowman.” These secondary pads are sized 0.05mm smaller than the primary pads, and the center is placed 0.075mm away from the center of the primary pad.

This technique is designed to provide additional metal at the critical junction of a pad and a trace. It becomes especially important during the process of registration and via drilling. This will reduce solder joint stresses, reduces risk of cracking, improves resistance to thermal shock and improves resistance to impact shearing. Use of teardrops, in conjunction with NSMD pads, provides additional ball-to-land contact area, making them more mechanically robust.

Check the latest IPC standards and discuss them with your PCB fabricator and PCB designer. In some cases, this feature is simply a check box on your CAD system or something that your PCB designer will do for you.

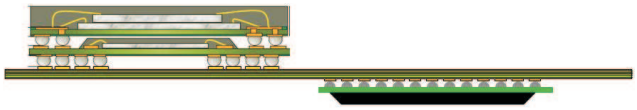
Figure 11. Teardrop and Snowman Pads



17 Multiple BGA Packages

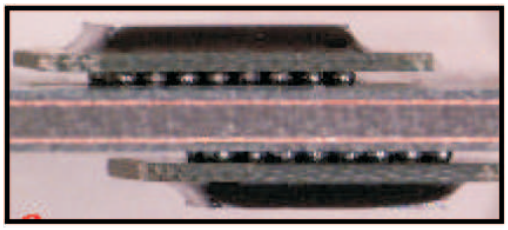
When BGA components are placed on both sides of the PCB, do not place one BGA component directly opposite another BGA component. The temperature cycle board-level-reliability (BLR) degrades if the PCB is designed with an overlap of BGA components.

Figure 12. Multiple BGA Components Should Be Off-Set



Several studies, including the one referenced here, show that temperature cycle (BLR) performance degrades if there is an overlap of package footprints. A small BGA opposite a large BGA or QFP, with its footprint within the unpopulated IO shadow of the larger package, has temperature cycle performance similar to that of a single-sided PCB assembly.

Figure 13. Multiple BGA Components Should not Be Overlapped



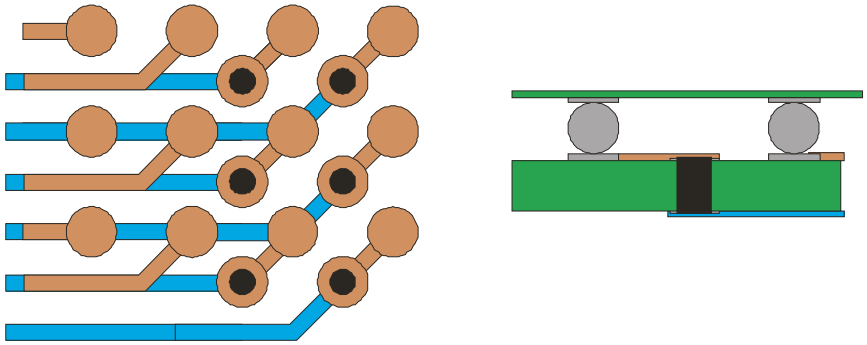
For additional information on this concept, please see section 5.4, Single-Sided Soldering and Double-Sided Soldering, of NEC’s, *Semiconductor Device Mount Manual*, http://www.necel.com/pkg/en/mount/.

18 BGA Routing

One trace can be routed between two solder pads of a 0.5mm pitch PGA. This allows the outer two rows of solder pads to be routed on the top layer. Therefore, each solder pad on the remaining rows will need a via to connect to another routing layer if all top layer routing tracks are used to route the second row of solder pads.

The inner rows of solder pads will connect to another routing layer for routing outside of the BGA area. VIP technology is not required if you consider the following routing strategy. The left portion of Figure 14 shows how a via can be placed between solder pads and connected to one of the adjacent solder pads on the top layer. This signal trace is routing outside of the BGA area using another layer in the PCB. This strategy can used for routing all of the inner solder pads. Since there is only enough space to route one trace between vias, this strategy requires an additional routing layer for every inner row of solder pads after the fourth row. The right portion of Figure 14 shows a cross-section side view of the via connections.

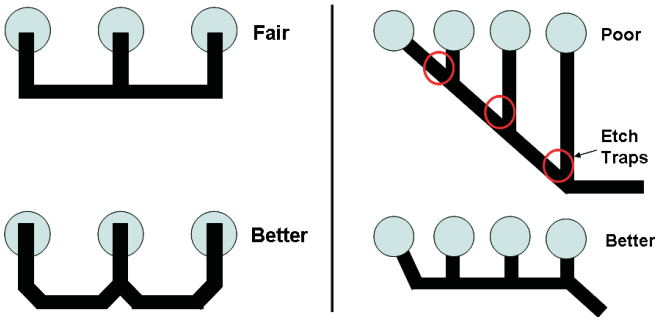
Figure 14. BGA Routing



19 Etch Traps and Heat Sinks

Be careful not to create etch traps when routing circuit traces. Figure 15 shows examples of etch trap routing guidelines. Another challenge with fine pitch PCB design is to ensure traces and vias do not pull heat away from the solder pad.

Figure 15. Etch Trap Routing Guidelines

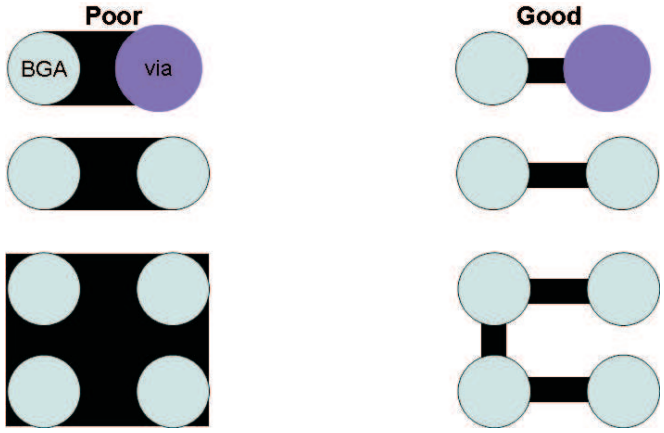


Small BGA pads do not have much solder and depend on uniform heating for a good joint. Here are some tips to ensure that traces and vias do not serve as heatsinks.

- Keep the trace smaller than the pad or via.
- Do not gang up pads with a copper pour such as around a ground plane without thermal reliefs.
- Use individual traces to interconnect the pads.

TI applications processors are relatively low-power devices so the smaller traces are appropriate.

Figure 16. Heat Sink Routing Guidelines



20 VIAS

The applications processor will need vias to make connections to other components. Fortunately, the use of PoP removes the cost, difficulty and challenge of routing high speed memory signals from under the applications processor to the memory. Instead, the memory sits on top of the processor and the connections are automatically made during PCB assembly.

The remaining connections from the applications processor can be accomplished using standard routing techniques. Exotic and expensive stacked vias or VIP technology will not be required for most PCB designs.

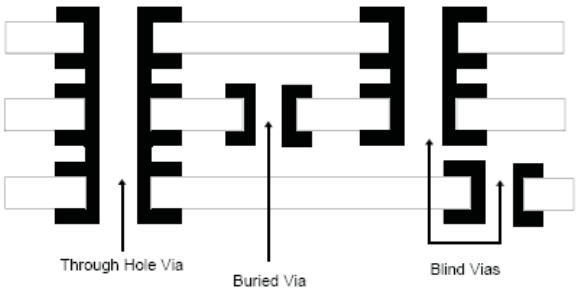
The 0.5mm pitch CBC package can be routed using an offset via with a 10mil diameter and a 5 mil hole. Although these vias might be called microvias, they are still constructed in the same fashion. It is common to classify a via that is 6mil or smaller as a microvia. There is nothing unique about them and can be drilled with either mechanical or laser drills.

The one key point to know is that vias with hole sizes over 0.4mm (15mil) cannot be tented because the solder mask falls into the holes and makes a mess.

Vias that pass through the entire PCB, from top to bottom, are through-hole vias. Vias that are visible on only one side are blind vias. And a via that is not exposed to the outside layers is called a buried via.

The formation of blind and buried vias may be accomplished through different processes. In some cases, they may be mechanically drilled and use standard equipment for making multilayer PCBs. The main difference is their smaller diameter, which requires greater care in the drilling process. The PCB fabricator needs to make certain the wall of the blind or buried via is clean and all debris is removed in order to ensure proper plating on the wall surfaces. Always talk to your PCB fabricator to discuss their limitations and recommendations.

Figure 17. Vias



20.1 Laser Blind Vias

A laser blind via should range from 5mils for standard vias to 2mils for advanced technology vias. The hole aspect ratio should be kept at a maximum of 0.75:1. Ratios can be as high as 1:1. Some holes used in modules can go to 1.5:1, but this should not be used for standard PCBs.

Laser vias are typically drilled through reinforced FR-4 material that is 0.002” thick or less. There is standard FR-4 or laser-drillable FR-4 that uses a more uniform glass weave. The LD glass has a cost adder to it, but produces a smoother hole wall surface which makes filling and capping easier. These decisions are best made by working with the PCB fabricator to see what has worked best in the past.

The minimum average copper plating thickness for a laser blind via hole should be specified as 0.0005” or should be specified as “In accordance with IPC-6012A, class 2.”

20.2 Via-In-Pad, Microvias, Stacked Vias, Filled Vias Introduction

Although not generally needed for 0.5mm pitch, you may be considering VIP technology for the smaller pitch devices. The VIP methodology places the via directly under the solder pad. However, this will require another step to seal the via. Usually this is done with either conductive or non-conductive filling of the vias.

For a 10mil solder pad, TI recommends the use of 4mil microvias that are laser drilled. After drilling, and depending on the PCB fabricator preferences, the vias are copper plated, then filled with a polymer consisting of a blend of copper and epoxy for a non-conductive option or copper, silver, and epoxy for a conductive option. It is important to ensure that the PCB vendor utilizes a via fill material with a copper particle size below 1 mil to ensure a complete penetration of the via by the fill material.

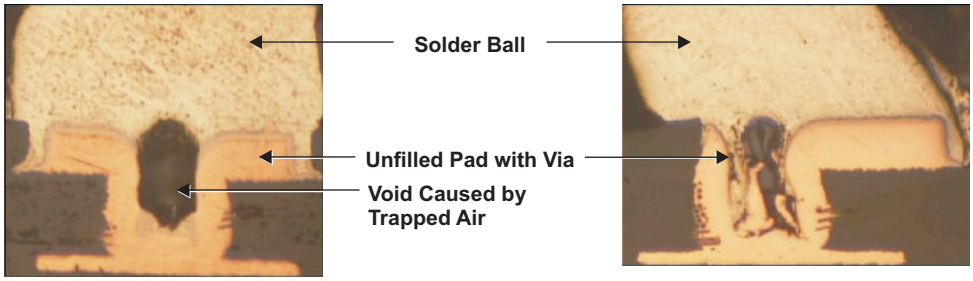
Once the vias are filled, cured, and planarized, the remainder of the plated holes are processed. This yields a flat copper plated cap over the vias which facilitates component attachment. The Via-in-Pad technology provides two primary benefits: higher component density and improved routing.

For most PCB fabricators, blind, stacked vias should be limited to only one or two layers, with three being the max. You must validate your PCB fabricator’s capability to reliably build with this class of technology.

All vias must be capped or filled to prevent voids and out gassing. The images in Figure 18 show the effect of an uncapped via. The voids and damage occurs during reflow. The right picture is a failure caused by the excessive package movement during reflow, caused by out gassing

Again, these decisions are best made by working closely with the PCB fabricator.

Figure 18. Effect of an Uncapped Via



20.3 Offset VIP

Offset VIP is a VIP with a hole that have been shifted from the center, towards one side of the solder pad. Studies have shown that the offset VIP will experience less voiding problems than a standard VIP with a centered hole. Sometimes these are called dogbones and depending on the distance from the pad center, they may be called snowman vias.

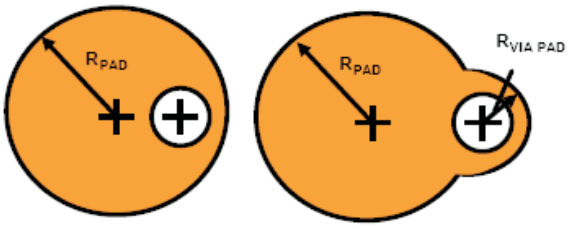
There are two generic configurations: the drilled hole is located between the center of the solder pad and the edge of the solder pad; or the drilled hole is located on a overlapping, or adjacent pad, where the hole is offset from the mounting pad center by up to $R_{PAD} + R_{VIA\ PAD} – 0.002$”. This is the equivalent of an overlapping adjacent pad.

Plated though hole vias must be filled with either conductive or non-conductive material and plated over. This will eliminate solder wicking down the via end eliminate trapped air in the via from moving up into the solder joint.

BGA pads with a pitch of 0.5mm to 0.8mm which utilize blind vias should have a drilled via diameter ≤0.004” and have an aspect ratio ≤ 0.75:1. These will not require any via fill or over plating. These vias will not significantly increase solder joint void formation versus pads with no vias.

The PCB assembler should be consulted prior to using a offset VIP configuration to establish their manufacturing requirements

Figure 19. Offset VIP



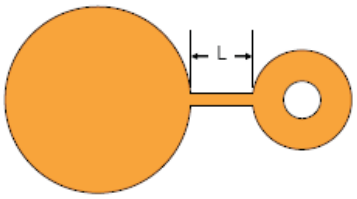
20.4 Adjacent Via

If space permits, this old fashioned dog-bone style via is best. It suffers from none of the voiding issues of the other techniques since the hole is not capped by the ball. However, it is still recommended that the via be covered up or plugged from the side that the component is mounted.

The trace length “L” connecting the via pad to the solder pad should be at least 0.005” long. This will eliminate solder flow from the pad into the via and allow for a soldermask dam to be placed across the trace. If the connecting trace is less than 0.003” the vias cannot be covered with solder mask. This is due to the high probability of getting solder mask on the solder pad.

Blind vias do not require any via fill or over plating. These vias will not significantly increase solder joint void formation versus pads with no vias.

Figure 20. Adjacent Via



20.5 Via Covering

TI strongly recommends that all vias be tented, filled and/or capped, especially under BGA packages. The PCB fabricator should be consulted prior to specifying via fill to establish their manufacturing requirements. Also, make sure your CAD system provides the required design files and the needed documentation. In some cases, additional files may be required.

Tom Hausherr, from PCLibraries, www.pclibraries.com , has a very good presentation covering various types of vias and via coverings. His presentation, “Metric Pitch BGA and Micro BGA Routing Solutions,” can be found on their website. They show seven different versions, each with different pros and cons. Please read this material since this paper will only highlight the three most commonly used types.

20.5.1 Tented Vias

A tented via is defined as a via that is completely covered by the solder mask. Tented vias are very popular because they have the lowest cost. Tenting can be used on a blind-via or a thru-hole via.

Vias under components are often tented to prevent the paste flux from running into the holes and onto the opposite side of the card, and to allow vacuum hold down on test equipment.

Tenting is normally done with a dry film solder mask rather than a liquid photo-imagable solder mask. However, a single-pass LPI mask cannot guarantee 100% coverage of the vias. Obtaining the best possible via coverage with screen printing is a compromise between hole size, surface tension of the liquid mask and PCB thickness. Thru-hole vias can be tented on both ends to reduce chances of chemical entrapment during surface precleaning. However, be aware that trapped gas will expand inside the hollow via during reflow and might present reliability problems.

A tented via which is open on one end may have another issue. This type of via can be subject to the "micro-etch" process. This is caused by a small amount of residual etchant trapped inside a tented via. This material will crystallize rapidly, creating copper sulfate crystals. Over time, these crystals can cause long term reliability issues. In the case of a electroless nickel immersion gold (ENIG) finish, the gold and small area of exposed copper near the tent could form a galvanic cell, accelerating the etch process.

Although tenting is inexpensive, other methods provide a more robust PCB design that does not suffer from the downsides of trapped gases or micro-etching. These factors must be carefully evaluated against the added processing cost of plugged vias which are much more reliable. Always discuss these options and considerations with your PCB fabricator before selecting any of these methods.

Figure 21. Tented Vias

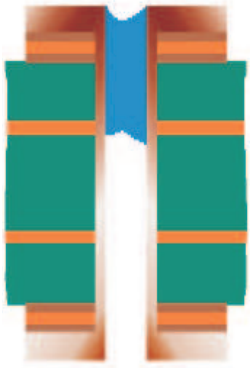
20.5.2 Plugged Vias

A plugged via is defined as a via that is partially filled with mask or other non conductive media. No surface finish is applied to via barrel. No surface finish is applied to the via.

Although sometimes confused with “filled vias,” a plugged via may not be completely filled. The material may be applied on either one side or both sides.

During solder mask application, the via is flooded with mask. And since it is only partially filled, chemical entrapment is a major concern.

Figure 22. Plugged Via



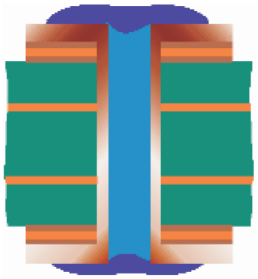
20.5.3 Filled Vias

Filled vias are 100% filled, usually with a non-conductive material. This process uses additional process steps. This is done to ensure 100% of the vias are covered.

There are several variations of the filled via.

A filled and covered via has a secondary covering of material (liquid or dry film solder mask) applied over the via. It may be applied from either one side or both sides.

Figure 23. Filled Via

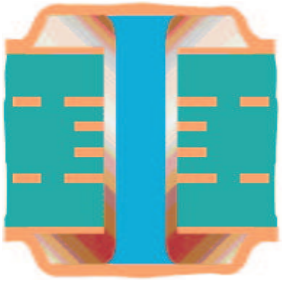


20.5.4 Filled and Capped Vias

This is the ultimate via and is commonly called Via-In-Pad (VIP). Vias are filled with a conductive or non-conductive media, planarized and then plated over. This process allows the use of via capture pads as SMD pads.

VIP has become very common in BGA PCB designs to reduce routing issues and lower inductance associated with high speed connections. However, it does drive up the overall PCB cost. If at all possible, consider other alternatives and use VIP only as a last resort.

Figure 24. Filled and Capped Via



21 Know Your Tools

Your CAD program must be setup correctly to define the appropriate pad and via stacks to support different types of vias. The additional process steps may require additional gerber files.

Your CAD manual and PCB fabricator will be your best friends as your tools are set up, so plan to learn and use all available supporting documentation as well as your extended team members.

NOTE: It is strongly recommended that all vias be covered, especially under BGA packages. In addition, the PCB fabricator should be consulted prior to specifying via fill to establish their manufacturing requirements, required design files, and the needed documentation.

22 Example PCB Design

The OMAP25x EVM is used as an example PCB design that required similar design guidelines as those discussed in this document. The OMAP25x component is not packaged in the same CBC package discussed, but it is similar enough to demonstrate good examples of PCB design guidelines presented in this document. Figure 25 from the layout of the OMAP25x EVM PCB, shows an example of the use of the discussed design guidelines. While the OMAP25x does not use exactly the same package as the OMAP35x, it is very similar and this PCB design shows some good examples of earlier discussions.

This example PCB design uses the previously discussed design guidelines and a six layer PCB. Each layer will be shown along with important notes about the PCB design.

These images of the OMAP25x EVM are from the Allegro viewer with the appropriate pins, vias and etch turned on for each layer. Figure 25 provides an overall PCB image, while Figure 26 through Figure 33 show various enlarged areas underneath the BGA package.

The color code is simple: green is etch, blue are vias, and gray is SMT pads for the components.

Figure 25. OMAP25x EVM PCB Layout

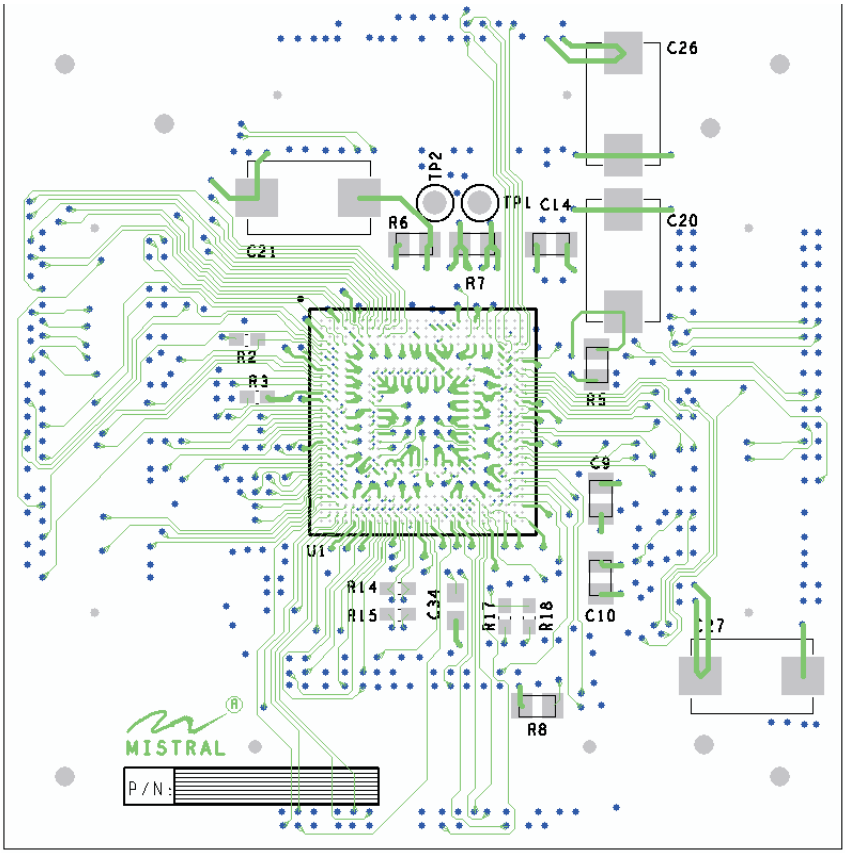
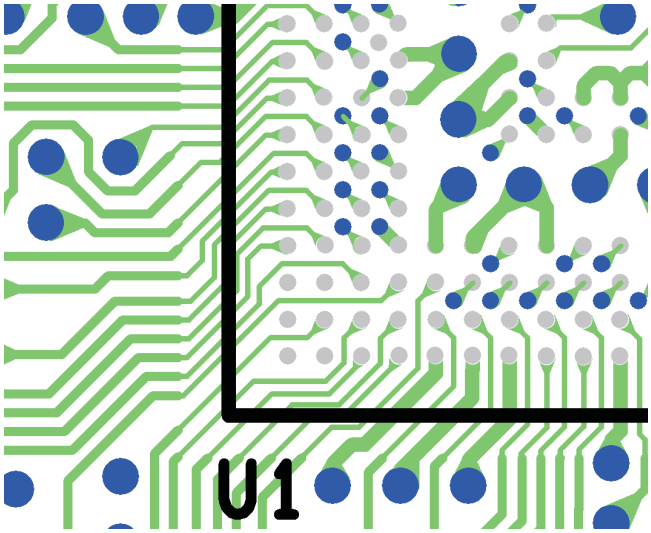


Figure 26. Layer 1 – Signal - Top Copper – Area Around The OMAP25x



Note that this viewer shows the individual traces used to approximate the teardrop trace exit from the pads and vias.

Figure 27. Layer 1 – Signal - Top Copper – Teardrop Trace

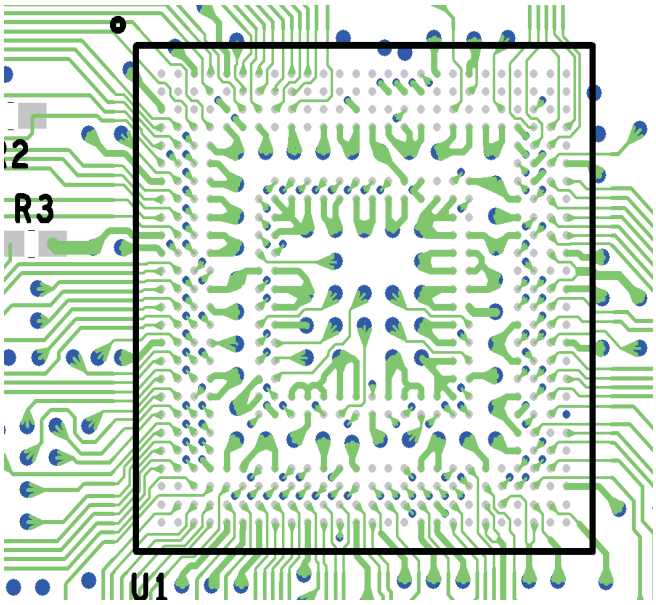
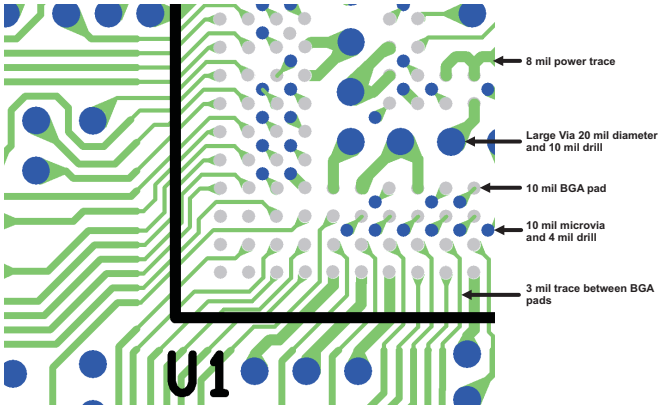


Figure 28. Layer 1 – Top Copper – Close Up View and Measurements



The microvia only goes between layer one and layer two on this design. There are no stacked vias. The small vias are from layer two to layer one. The large vias are through vias from top to bottom.

Figure 29. Layer 2 - Signal

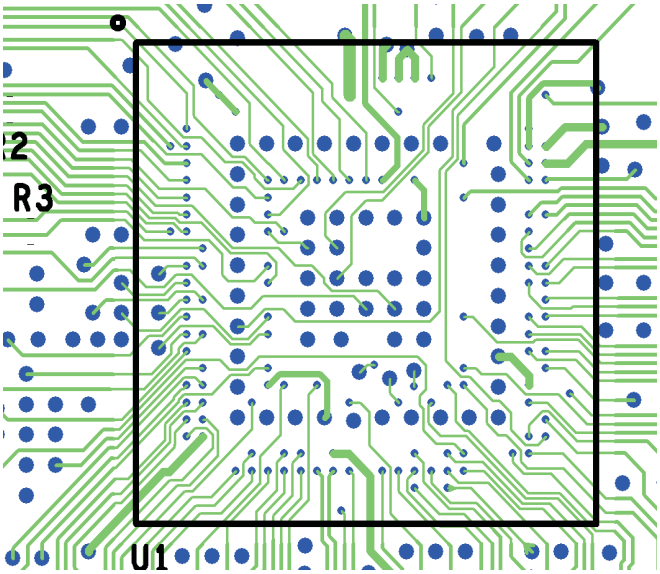


Figure 30. Layer 3 - Ground

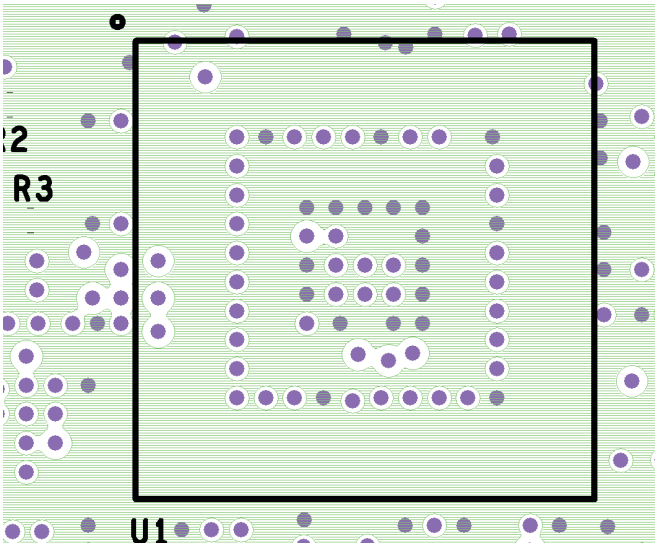


Figure 31. Layer 4 - Power

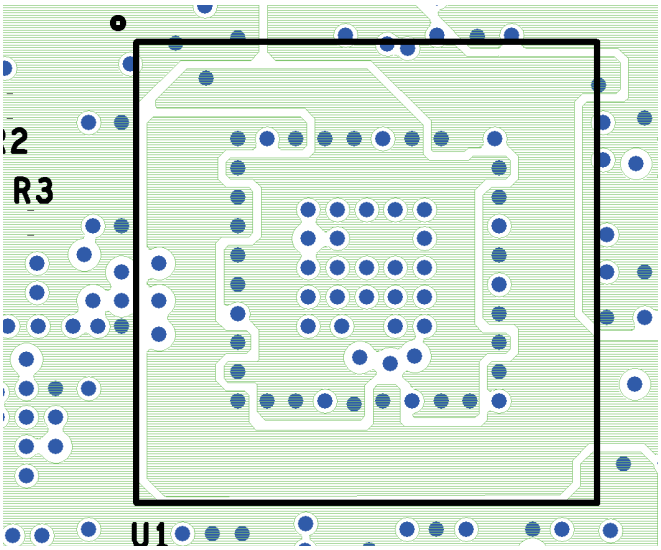


Figure 32. Layer5 - Signal

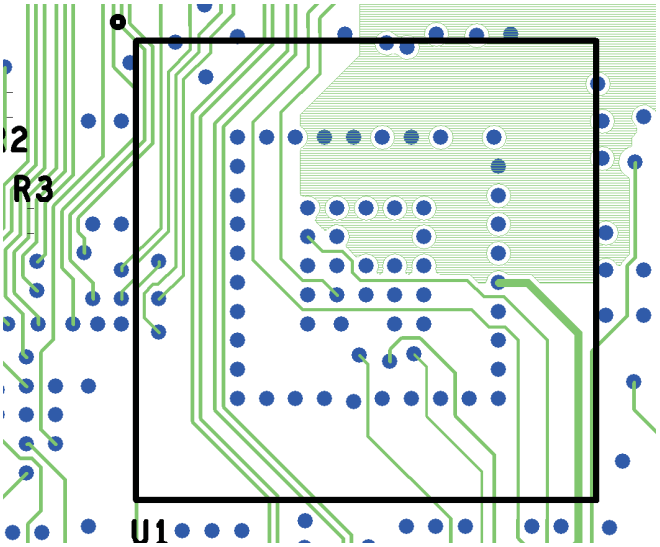
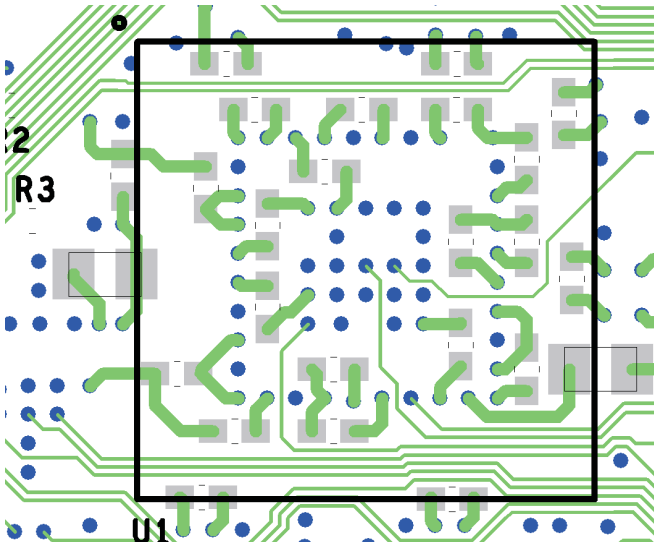


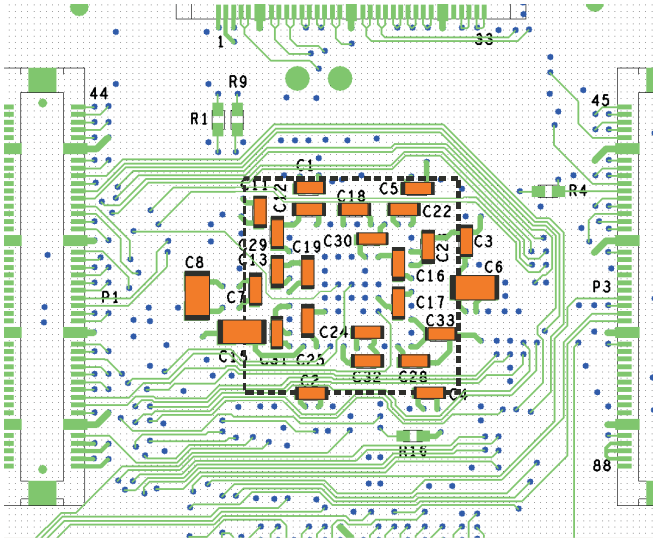
Figure 33. Layer 6 - Signal – Bottom Copper – Bottom Component Outlines



The majority of the components within the U1 outline (which is not physically present on the bottom silkscreen) are bypass capacitors.

Figure 34 shows the bottom side of the OMAP 25x EVM PCB showing the traces, vias and bypass capacitors. The outline of the OMAP processor is shown as a black dotted line. This illustrates how the bypass capacitors are literally as close as possible to the appropriate supply pins of the processor. Most are connected through vias to the top side of the PCB. Appropriate connections are also made to the power and ground layers.

Figure 34. Bottom Side of the OMAP EVM25x PCB



23 PCB Finishes for HDI

A surface finish provides a coating over the outer layer copper that prevents oxidation and provides an electrically conductive surface. This surface has two generic functional requirements: to provide a solderable surface for connecting components with solder and to attach a component without soldering, such as a wire bond or press-fit connector.

Organic Solderability Preservative (OSP)— This process coats a very thin coating of an organic material that inhibits copper oxidation. It is so thin that it is nearly impossible to see and measure. The organic material is removed by the solder flux used during PCB assembly. PCBs that have been OSP coated will have bright copper pad coloration. The most prevalent OSP is ENTEK CU-106A. This coating is used for PCB assemblies that will go through multiple assembly operations. PCB's that have multiple surface finishes can also use the CU-106A(X) finish.

Immersion Tin (ImSn)— This process coats a thin layer of tin directly on top of the copper surface. The tin produces an extremely flat surface for mounting of surface mount components with ultra fine-pitch components. This coating also provides a thicker, uniform surface that provides lubrication for press-fit pins.

Immersion Silver (ImAg)— This process plates a thin layer of silver directly on top of the copper surface. As with the other immersion surface finishes, the finished product produces a very flat surface; it is ideal for fine pitch components. This surface finish has the ability to maintain high solderability after multiple heat cycles. This can also be used as an aluminum wire bondable surface. It is compatible with no-clean assembly processes. This is becoming popular as a hot air solder leveling (HASL) replacement for lead-free soldering applications. This surface finish yields a dull tarnished looking surface. There is significant industry data showing that the dullness does not affect solderability or reliability.

Other Finishes— Other finishes include hot-air solder leveling and immersion nickel-gold (ImNiAu). Table 1, from a 2003 Surface Mount Technology Association (SMTA) paper, summarizes the attributes of each PCB finish.

Table 1. 2003 SMTA Paper Summary of Attributes of Each PCB Finish

Parameter	HASL	OSP	ENIG	ImAg	ImSn
Standard solder joints are predictable	P	P	P	P	P
BGA solder joints are predictable	P	P	M	P	P
Solderability shelf life is one year	P	M	P	M	M

Table 1. 2003 SMTA Paper Summary of Attributes of Each PCB Finish (continued)

Parameter	HASL	OSP	ENIG	ImAg	ImSn
Soldermask compatibility	P	P	M	P	M
Via plugging is safe and reliable	P	M	P	M	M
Improves overall via reliability	M	--–-	P	--–-	--–-
Flat surface benefits assembly	M	P	P	P	P
Conductive contact surface	P	M	P	P	P
Solderable over four heating cycles	P	P	M	P	P
Thickness variation is minimal	M	P	P	P	P
Coating is environment friendly	M	P	P	P	P
Tin whiskers are not a problem	P	P	P	P	M
P = plus, M = minus, N = neutral	8P	8P	9P	9P	7P
September 2003	SMTA International				

24 Solder Paste Stencil Design

Stencil design has several critical factors that affect solder paste deposition. For this discussion, the recommendations apply only to round pads for fine pitch, BGA packages with 0.5mm spacing. These recommendations can be considered as a starting point for building design rules that fit your manufacturing requirements and capabilities. These recommendations assume a lead-free process is used. In all cases, you must carefully monitor assembly startup so as to ensure the desired results are being achieved.

24.1 Area Ratio

The relationship between the surface of the aperture and the inside surface of the aperture walls in the stencil is referred to as the Area Ratio (AR). The area ratio is much more suitable for shapes such as circles than the aspect ratio. For fine pitch BGA pads, a round aperture is recommended.

An area ratio of ≥ 0.66 has been shown to provide the best transfer efficiency and repeatability of deposited solder paste. Values from 0.66 to 0.8 ensure a good paste release from the stencil.

The biggest impact on area ratio is the stencil thickness. The equation is

$$AR = Ap / Aw \geq 0.66$$

where Ap is the aperture opening area and Aw is the wall area

$$\pi r^2 / 2\pi rT \geq 0.66$$

Where r is the aperture opening radius and T is the stencil thickness. This table shows the various values of AR for different aperture openings and stencil thicknesses.

aperture opening (mils)	aperture radius (mils)	stencil thickness (um)	stencil thickness (mils)	AR	
10	5.0	100	3.94	0.64	100um stencil
11	5.5	100	3.94	0.70	
12	6.0	100	3.94	0.76	
13	6.5	100	3.94	0.83	
14	7.0	100	3.94	0.89	
15	7.5	100	3.94	0.95	
16	8.0	100	3.94	1.02	
10	5.0	125	4.92	0.51	125um stencil
11	5.5	125	4.92	0.56	
12	6.0	125	4.92	0.61	
13	6.5	125	4.92	0.66	
14	7.0	125	4.92	0.71	
15	7.5	125	4.92	0.76	
16	8.0	125	4.92	0.81	
10	5.0	127	5.00	0.50	5 mil stencil
11	5.5	127	5.00	0.55	
12	6.0	127	5.00	0.60	
13	6.5	127	5.00	0.65	
14	7.0	127	5.00	0.70	
15	7.5	127	5.00	0.75	
16	8.0	127	5.00	0.80	
10	5.0	152.4	6.00	0.42	6 mil stencil
11	5.5	152.4	6.00	0.46	
12	6.0	152.4	6.00	0.50	
13	6.5	152.4	6.00	0.54	
14	7.0	152.4	6.00	0.58	
15	7.5	152.4	6.00	0.63	
16	8.0	152.4	6.00	0.67	

24.2 Aperture Size and Overprinting

When depositing solder paste, overprinting of the pad is desirable to get additional solder on the pad for a more robust joint. This also helps to minimize coplanarity issues. In addition, there is sufficient solder to cover the sides of the NSMD pad, which helps distribute stress to a larger area.

When overprinting, it is mandatory that all traces and vias be plugged and covered with soldermask.

Based on studies by Avant of Austin, Texas, it is recommended to overprint a 0.5mm BGA's 10 mil pad from 1 to 3 mils around the pad's circumference. Thus a 10 mil copper pad will have a stencil aperture from 12 to 16 mils in diameter using a 6 mil thick stencil. While this may seem excessive, the solder paste will quickly wick back to the pad leaving a good solid foundation of solder and a very robust joint.

The table below summarizes the various overprint amounts and the resulting aperture opening. Use this value to confirm the correct AR value for the stencil thickness to be used.

Overprinting for BGA @ 0.5mm Copper Pad	radius	overprint amount	Aperture Opening
10	5	3	16
10	5	2	14
10	5	1	12

24.3 Aperture Shape

A round aperture shape is recommended for BGA pads. This allows for an equal amount of overprinting on a round pad. Square corners can result in unequal amounts of paste being deposited and should be avoided.

24.4 Stencil Material and Finishing

The solder stencil should be made from stainless steel, chromium or Cobalt Nickel. The apertures should be laser cut. The finish should be eletropolished to provide mirror smooth walls. The mirror smooth aperture walls ensure good paste release.

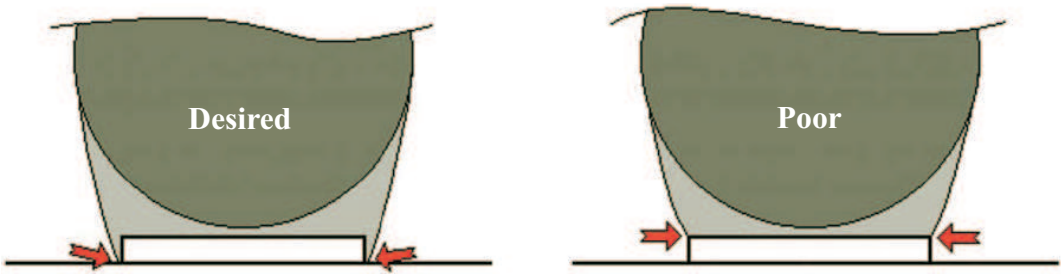
During assembly, the wider side of the aperture should be against the PCB.

The best solder joint for BGA packages, is created using a NSMD pad along with the recommended stencil design. In the figure below, the red arrows show the stress points for two types of pad and paste depositions. These stress points have been found to have the highest stress during thermal cycling.

When the paste is allowed to wet the side walls of the pad, a much more robust joint is formed.

With poor wetting of solder pad edges, the stress induced during thermal cycling will be more focused at the interface between solder and the copper pad. Furthermore, the poor wetting will cause a reduction of the solder fillet diameter at the level of the pad surface, which also will contribute to the significantly reduced fatigue life.

Figure 35. Desired & Poor Wetting



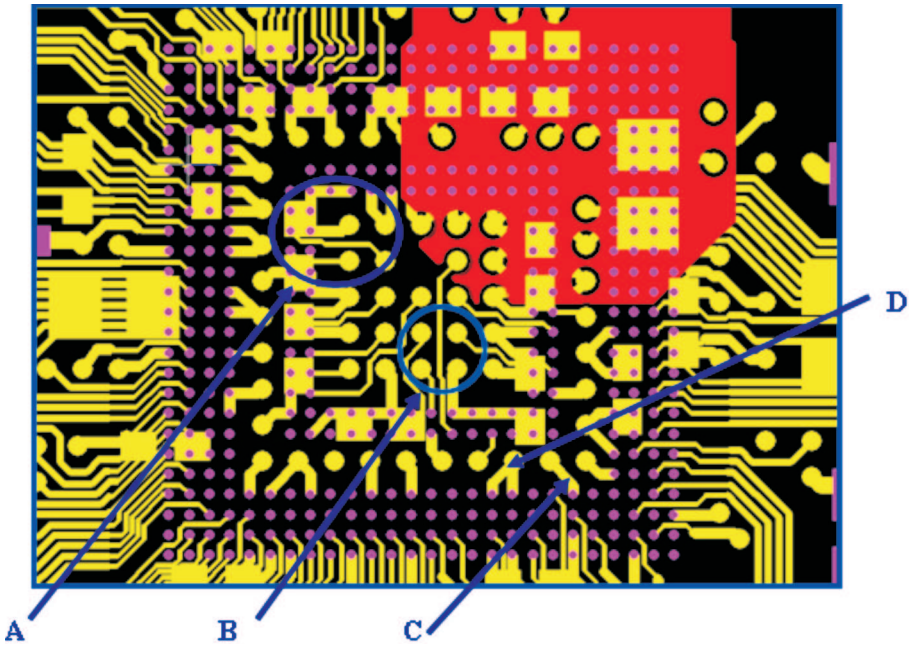
With proper stencil design, proper paste deposition, proper paste formulation and correct reflow temperatures, the solder will wet the solder ball and adhere to the edges of the copper pad resulting in a very strong and robust joint that can withstand the rigors of today's consumer products.

25 Real World Second Opinion

The first OMAP EVM PCB was designed prior to the release of these guidelines and was submitted to an assembly vendor where they performed a DFM analysis on the gerber files. Their comments related to the original PCB design are listed below and the locations being discussed are shown in Figure 36.

This demonstrates an example of valuable communications between members of the design team. If the original PCB design had gone into production, the yield would have been very poor. Our thanks to Elcoteq in Richardson, TX for their analysis of the PCB design.

Figure 36. First Pass DFM of the OMAP35x EVM



- At location A, seven BGA Pads are ganged together. This acts as a large heatsink during reflow.
- The traces between D and the BGA pad should be narrower. A trace entering a pad should never be larger than the diameter of the pad.
- In some cases the BGA to ground plane is done like D and the other is done like A. Neither are good techniques.
- In C, the trace width exiting the BGA pad is much too large. In this case the trace acts as a heatsink during reflow.
- As in details A,B,C and D, the heat transfer from the ground planes is passing through a large via through a large trace and fanned out across 7 BGA pads ganged together.
- Do not gang BGA pads together with a copper plane as this increases the heat sink effect.

26 Acknowledgments

- Clint Cooley and Franklin Troung, CircuitCo, 675 N. Glenville #195, Richardson, TX 75081, 214-466-6690, www.circuitco.com
- Elcoteq, Sinimaentie 8B, P.O. Box 8, FI-02631 Espoo, Finland
- Micron Technology, Inc., 8000 South Federal Way, Post Office Box 6, Boise, ID 83707-0006
- Ron Weindorf, Process Engineer, for his review and critique of this paper. His contributions and suggestions are gratefully acknowledged, received and incorporated. Avant Technology, 9715A Burnet Road, Austin, TX 78758

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