TMS320C6472 Power Consumption Summary

ABSTRACT

This document discusses the power consumption of the Texas Instruments TMS320C6472 digital signal processor (DSP). The power consumption on the TMS320C6472 device is highly application-dependent; therefore, a power spreadsheet that estimates power consumption is provided along with this application report. This spreadsheet can be used to model power consumption for user applications such as power supply design, thermal design, etc. To obtain good results from the spreadsheet, realistic usage parameters must be entered (see Section 3.1.3). The low-core voltage and other power design optimizations allow these devices to operate with industry-leading performance, while maintaining a low power-to-performance ratio.

The data presented in this document and in the accompanying spreadsheet were measured from devices at the maximum end of the power consumption for production devices. No production devices will have average power consumption that exceeds the spreadsheet values; therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

The spreadsheet discussed in this application report can be downloaded from http://www.ti.com/lit/zip/SPRAB76.

Contents

1 Activity-Based Models

Power consumption for the TMS320C6472 DSP can vary widely depending on the use of on-chip resources. Therefore, power consumption cannot be estimated accurately without an understanding of the components of the DSP in use and the usage patterns for those components. By providing the usage parameters that describe how and what is being used on the DSP, accurate power consumption numbers can be obtained for power-supply and thermal analysis. You can determine expected power consumption for worse case utilization, by choosing the peripherals in use.

The power spreadsheet divides the power consumption into two major components: baseline power and activity power.

1.1 Baseline Power

Baseline power consumption is the power consumed that is independent of chip activity; such as static leakage power, and core power (core power includes clock tree, internal memory, on chip module power, etc.). Baseline power is highly dependent on voltage, temperature, and CPU frequency.

1.2 Activity Power

Activity power consumption is power that is consumed by all active parts of the DSP: central processing until (CPU), enhanced direct memory access (EDMA), peripherals, etc. The activity power is independent of temperature, but highly dependent on activity levels of CPU, EDMA, peripherals, etc. In the power spreadsheet, activity power is separated by the major modules/peripherals within the device. Therefore the individual module/peripheral power consumption can be estimated independently. This helps with tailoring power consumption to specific applications.

Module/peripheral activity power consumption includes some necessary EDMA and CPU activity used to transfer data on-chip and off-chip when required. The power consumption associated with EDMA and CPU activity has been minimized to only show power consumption with respect to the module/peripheral tested.

2 Spreadsheet Parameters

The spreadsheet provides configurable parameters, which allows you to estimate power consumption based on configured usage parameters. To ensure realistic results, take care to make sure the spreadsheet is configured accurately. For more details, see Section 3.1. The parameters are as follows:

- Frequency: The operating frequency of a module/peripheral or the frequency of external interface to that module.
- Modes: Select
  - Ethernet media access controller (EMAC) modes/throughput
    - Throughput at 1000/100/10 Mbps
      - RGMII
      - GMII
    - Throughput at 100/10 Mbps
      - RMII
      - S3MII
      - MII
  - Serial RapidIO® (SRIO)
    - Number of lanes
    - Throughput
- % Utilization: The relative amount of time the module is active or in use versus off or idle.
- % Write: The relative amount of time (considering active time only) the module is transmitting versus receiving.
- Bits: The number of data bits being used in a selectable-width interface.
- % Switch: The probability that any one data bit on the relative data bus will change state from one cycle to the next.

2.1 Device Modules/Peripherals

The TMS320C6472 power estimation spreadsheet contains the following modules with adjustable parameters:

- CPU [5:0]
- Timer [11:0]
- DDR2
- EMAC [1:0]
- SRIO
- HPI
- UTOPIA
- TSIP [2:0]
- I2C

EDMA is not listed as a separate module because the module/peripheral activity already includes any necessary EDMA activity used for memory-to-memory transfers only. For available peripheral configurations, see the device-specific data sheet.

2.2 3.3 I/O Power Results

The 3.3 I/O power consumption for EMAC [1:0], host-port interface (HPI), Universal Test and Operations PHY Interface for ATM (UTOPIA), and Telecom serial interface ports (TSIP) [2:0] were estimated using the dynamic power equation, CV^2F, instead of measured silicon results. The following parameters were used for variables within the formula for each peripheral:

- Capacitance ©)
  - Input pins = 1 pF
  - Output pins = 10 pF
- Voltage = 3.3 V
- Frequency
  - Peripheral I/O operating frequency. Note control and data lines frequencies are scaled based on the appropriate toggling rates.

3 Using the Power Estimation Spreadsheet

Using the power estimation spreadsheet involves entering the appropriate usage parameters as input data in the spreadsheet. The following steps explain how to use the spreadsheet:

1. Choose the appropriate operating CPU frequency (375 MHz to 625 MHz):
   (a) Core voltage = 1 V for CPU frequencies 375 MHz to 500 MHz
   (b) Core voltage = 1.1 V for CPU frequencies 501 MHz to 625 MHz
   (c) Core Voltage = 1.2 V for CPU frequencies 626 MHz to 700 MHz
2. Choose the case temperature for which you want to estimate power, 1°C to 100°C. When the frequency is set to an option great than 625 MHz, the case temperature is limited to a maximum of 85°C.
3. Enable the appropriate peripherals used for your application including the mode, frequency, and bus width for that peripheral, if necessary.
4. Fill in the appropriate peripherals or modules % utilization, % writes, and % switching
5. Add an additional bus capacitance, if the peripherals I/O is connected to a shared bus.

The spreadsheet takes the provided information and displays the details of power consumption for the chosen configuration.

As the spreadsheet is being configured, the settings are checked for conflicts, i.e., the peripherals clock frequency out of allowed range, etc. For best results, the information should be entered from left to right starting at the top and moving downward.

3.1 Choosing Appropriate Values

The frequency and bits user values are determined by design and it will be clear what the correct values to enter are. You can disable modules in the spreadsheet that are completely unused and disabled from the peripheral configuration register by selecting the *Disabled* button/tab in the column labeled *Status*. The utilization, read/write balance, and bit switching require estimation and a good understanding of the user application to choose appropriate values.

3.1.1 Utilization

For modules, except CPU, utilization is simply the percentage of the time the module spends doing something useful, versus being unused or idle. For these peripherals, there are no varying degrees of use, so the value is just the average over time. For example, the DDR2 performs reads and writes one-quarter of the time, and has no data to move for the other three-quarters of the time (though it continues to perform background tasks like refreshes); this would be considered 25% utilization.

The CPU utilization is not as straightforward because there are varying degrees of use for the CPU. The spreadsheet estimates the CPU activity with respect to the following activity levels:

- Percent utilization with high activity means that all eight functional units are active every CPU clock cycle. The maximum amount of data is brought in every cycle. Few DSP algorithms will achieve 100% utilization, because this requires execution of all eight function units every cycle, with no stalls. Even intense applications do not spend all of the time in such highly parallel loops.
- Percent utilization with low levels of activity includes some type of task polling loop or background task. The activity requires execution of approximately two functional units executing every clock cycle. This type of code execution is normally considered to be control code.
- Zero percent utilization means the CPU is active, however, the CPU is idle doing no useful work (NOP execution)

System level issues may also reduce utilization. Though the spreadsheet accepts 100% utilization for all peripherals, this is not possible in reality. As memory and EDMA bandwidth is consumed, peripheral activity is throttled back due to these bottlenecks and, therefore, do not achieve 100% utilization. In applications with a lot of memory and/or EDMA usage, enter the individual module utilization numbers keeping this overall limitation in mind.

3.1.2 % Writes

Peripherals that transmit as much as they receive have 50% writes; the spreadsheet assumes the remaining 50% of the time is spent on reads. In some applications, peripherals transmit in only one direction, or have a known balance of data movement. In these cases, the % writes option is not available for configuration. For the peripherals that have the % write configuration, 50% is a typical number that should be used.

3.1.3 % Switching

Random data has a 50% chance that any bit will change from one cycle to the next. Some applications may be able to predict this chance using some a priori information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. All other applications should use the default number of 50%.

3.2 Peripheral Enabling and Disabling

As mentioned earlier, the TMS320C6472 device provides the capability to disable peripherals to reduce power consumption. You can do this by configuring the power/sleep controller (PSC). The spreadsheet also allows you to disable peripherals controlled by the PSC to ensure the peripherals' dynamic power is not included if the peripheral is not being used. For more details, see the device-specific data sheet and the *TMS320C6472/TMS320TCI6486 Power/Sleep Controller (PSC) User's Guide* (SPRUEG3).

A peripheral can be enabled or disabled in the spreadsheet from the column labeled *Status*. If the peripheral is disabled, the CV_{DD} and I/O power for the peripheral will be zero. If the peripheral is enabled with 0% utilization, the activity power for CV_{DD} and I/O will be zero; however, the peripheral will have baseline power consumption due to enabling/clocking the peripheral. For more information, see the *TMS320C6472/TMS320TCI6486 Power/Sleep Controller (PSC) User's Guide* (SPRUEG3).

The C6472 device also has the capability to disable the 3.3 I/O buffers for unused peripherals by configuring the Device Status Register (DEVSTAT). For more details, see the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612).

4 Using the Results

The power data presented in this document and the accompanying spreadsheet is collected from devices considered at the maximum end of power consumption for a production device; no production units will have an average power consumption that exceeds the spreadsheet values. Therefore, the power consumption estimated by the spreadsheet is considered average power consumption. Transient currents may cause power to spike above the spreadsheet values for a small amount of time; however, over a long period, the observed average power consumption will be below the spreadsheet value. The spreadsheet value may be used for board thermal analysis and power supply design as a maximum long-term average.

4.1 Adjusting I/O Power Results

I/O power is dependent on DSP activity, I/O switching rate, and the load driven. For loads with CMOS inputs, the power required to drive the trace dominates; therefore, the power will scale based on the capacitance loading. The data presented in the spreadsheet for TSIP [2:0], EMAC [1:0], HPI, UTOPIA, and inter-integrated circuit (I2C), were loaded with approximately 2.5 inches of 50 Ω trace, with serial termination.

The spreadsheet provides the capability to adjust the capacitive loading for EMAC [1:0], TSIP [2:0], HPI, UTOPIA, and I2C by enabling the trace capacitance in column I and J. You can increase the trance capacitance by entering a value in the trace column. Normally this feature is only used if the peripherals 3.3 I/O are connected to a shared bus with other devices or traces that exceed 2.5 inches in length.

For DDR2 and SRIO layout specifications, see the device-specific physical guidelines documents.

5 Spreadsheet Example

Section 5.1 demonstrates an example on how to choose appropriate values for a particular application. The values used in this example may be imported into the spreadsheet by clicking the appropriate macro button.

5.1 Sample Application

The following example provides an estimation of power consumption when the DSP is being used to process data for IDLE and Example 1 applications. The spreadsheet provides the estimated total power for core and I/O using the parameters defined below as input.

5.1.1 IDLE Power Configuration

In the spreadsheet, there is a button labeled *IDLE* that populates the spreadsheet with the following values:

- Case temperature: 85°C
- Device frequency: 500 MHz
- CPU[5:0]
  - 0% utilization of DSP code
  - 0% utilization of control code
- All peripherals (disabled)

The IDLE total power for CV_{DD} and I/O = 2 Watts

5.1.2 Example 1 Power Configuration

The spreadsheet includes a button labeled *Example 1* which is used to populate the spreadsheet with values similar to a moderate-to-heavy CPU activity system. The configuration assumes the following:

- Case temperature: 85°C
- Device frequency: 500 MHz
  - CPU[5:0]
    - 50% utilization of DSP code
    - 50% utilization of control code
  - Timer[11:0] (enabled)
  - DDR2 (enabled; 50% utilization, 50% switching, 32 bits)
  - EMAC0 (RGMII, 1000 Mbps)
  - EMAC1 (disabled)
  - SRIO (enabled; 50% utilization, 50% switching, 2 lanes, 3.125 rate)
  - HPI (disabled)
  - UTOPIA (disabled)
  - TSIP0 (12.5% utilization, 20% switching)
  - TSIP1 (12.5% utilization, 20% switching)
  - TSIP2 (disabled)
  - I2C (disabled)

The Sample Application total power for CV_{DD} and I/O = 4.4 Watts

6 TMS320C6472 Voltage Supply Reference List

The voltage supply reference list provides a description of the pins connected to each power rail for power consumption (see Table 1).

Table 1. Power Pins

Group Name	Signal Name	Description
T_CVDD	**CV** $_{DD}$	Core supply voltage
T_C1VDD_1.2	**C1V** $_{DD\_12}$	1.2 DDR2 core supply voltage V_{DD2}
T_C2VDD_1.2	**C2V** $_{DD1.2}$	EMAC core supply voltage V_{DD1}
TDVDD_3.3	**DV** $_{DD3.3}$	3.3 I/O voltage supply VDDSHV, HOUT, CPUEMU[1:0]
T_DVDD_1.8	**DV** $_{DD\_18}$	1.8 I/O voltage supply $V_{DD18MON}$, HHV18EN, V_{DDS1}
T_DVDD_1.5	**DV** $_{DD\_15}$	EMAC I/O voltage supply VHSTL
TDVDD_1.2	**DV** $_{DD\_12}$	SRIO I/O voltage supply V_{DDD} and V_{DDA}
T_DVDD_PLL	**DV** $_{DD\_PLL}$	PLL voltage supply V_{DDS2}

7 References

- *TMS320C6472/TMS320TCI6486 Power/Sleep Controller (PSC) User's Guide* (SPRUEG3)
- *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612)

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