TMS320DM6467T Power Consumption Summary

DSPS Applications

ABSTRACT

This application report discusses the power consumption of the Texas Instruments TMS320DM6467T digital media System-on-Chip (DMSoC). Power consumption on the DM6467T device is highly application-dependent; therefore, a spreadsheet that estimates power consumption is provided along with this document. To obtain good results from the spreadsheet, realistic usage parameters must be entered (see Section 2.1). The low-core voltage and other power design optimizations allow these devices to operate with industry-leading performance, while maintaining a low power-to-performance ratio.

The data presented in the accompanying spreadsheet was measured from strong units, representative of devices at the maximum end of power consumption for production units. No production units will have average power consumption that exceeds the spreadsheet values; therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

The spreadsheet discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/SPRAB64.

Table 1. Typical Activity

Sample	Core Voltage	Configuration	CPU Frequency	Power (mW) [1]			
				Core	IO18	IO33	Total
DM6467TZUT1/ DM6467TZUTD1	1.3 V	Static	0	655.22	50.76	84.16	790.15
		Standby	33 MHz	1038.51	104.09	84.16	1226.77
		DSP+ARM+DDR	1 GHz	2329.88	385.24	84.69	2799.82

[1] Static power consumption varies with process, temperature and voltage. Readings shown here are taken at room temperature (25°C). In standby power consumption, both static and clock in power is considered. In DSP + ARM + DDR power consumption, DSP is running at 1 GHz with 60% utilization ARM is running typical activity, DDR2 is configured at 400 MHz with 50% utilization, 50% writes, 32 bit width, and 50% bit switching.

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1 Model Activity

1.1 Activity-Based Models

Power consumption for the TMS320DM6467T can vary widely depending on the use of on-chip resources. Therefore, you cannot estimate power consumption accurately without an understanding of the components of the DMSoC in use and the usage patterns for those components. By providing the usage parameters that describe how and what on the DMSoC is being used, accurate consumption numbers can be obtained for power-supply and thermal analysis.

This model breaks down power consumption into two major components: baseline power and activity power. Using this model, various applications that use the DMSoC differently can get accurate predictions across the spectrum of possible power consumption on the DM6467T.

1.2 Baseline Power

Baseline power consumption is power that is independent of chip activity such as static power (leakage), phase-locked loop (PLL), oscillator power, DDR2 DLL consumption, and clock tree power to various subsystem components (e.g., SCR) that cannot be turned off via the on-chip power management module. While independent of chip activity, baseline power is dependent on the device operating frequency, voltage, and temperature. Therefore, you can affect baseline power only by changing the PLL(s) output frequency, the core voltage, or the operating temperature.

1.3 Activity Power

Activity consumption is power that is consumed by active parts of the DMSoC: CPU(s), EMIF, peripherals, etc. Activity power is independent of temperature, but dependent on voltage and activity levels. In the spreadsheet, activity power is separated by the major modules within the device. Therefore, the individual module power consumption can be estimated independently; this helps with tailoring power consumption to specific applications. The parameters used to determine the activity level of a module are frequency, utilization, read/write balance, bus size, and switching probability. Note that not all parameters apply to all modules.

- Frequency: The operating frequency of a module or the frequency of external interface to that module.
- Status: Indicates whether the module is in an enabled or disabled state.
- % Utilization: The relative amount of time the module is active or in use versus off or idle.
- % Write: The relative amount of time (considering active time only) the module is transmitting versus receiving.
- Bits: The number of data bits being used in a selectable-width interface.
- % Switch: The probability that any one data bit will change state from one cycle to the next.

Not all modules include all of the parameters.

1.4 DM6467T Parts

There are different types of TMS320DM6467T parts available that suit different applications and environment conditions.

- Normal part
- Industrial Temp part (-D parts)

For more details on the part numbers, see the Device Nomenclature in the *TMS320DM6467T Digital Media System-on-Chip Data Manual* (SPRS605).

Normal Parts operate at 1.3 V core voltage and up to 1 GHz core frequency under 0°C to 85°C case temperature.

Industrial Temp parts operate up to 1 GHz core frequency under -40°C to 85°C case temperature.

1.5 Modules

The DM6467T power estimation spreadsheet contains the following modules with adjustable parameters:

- Digital Signal Processor (DSP)
- ARM MM (megamodule) (see Section 6)
- High-Definition Video Image Co-Processor (HDVICP) (0 and 1)
- Video Data Conversion Engine (VDCE)
- Video Port Interface (VPIF) (display and capture)
- Transport Stream Interface (TSIF) (0 and 1)
- DDR2 Memory Controller
- External Memory Interfaces (EMIFA)
- Ethernet Media Access Controller (EMAC)
- AT Attachment (ATA)
- VLYNQ™
- Universal Serial Bus (USB) 2.0 (see Section 6 for limitations)
- Peripheral Component Interconnect (PCI)
- Universal Host Port Interface (UHPI)
- Multichannel Audio Serial Port (McASP) (0 and 1)
- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I2C)
- Timer (0 and 1)
- Watchdog Timer (WDT)
- Pulse Width Modulator (PWM) (0 and 1)
- Universal Asynchronous Receiver/Transmitter (UART) (0, 1 and 2)
- General-Purpose Input/Output (GPIO)
- Enhanced Direct Memory Access (EDMA3)

The EDMA3 activity power is included in the activity power of the module/peripheral serviced by the EDMA3; this includes McASP, SPI, UART, I2C, EMIFA, and DDR2.

2 Using the Power Estimation Spreadsheet

The power estimation spreadsheet involves entering the appropriate usage parameters as input data in the spreadsheet. Cells that are designed for user input are white in color. The following steps explain how to use the spreadsheet:

1. Choose the case temperature for the estimated power
2. Fill in the appropriate module use parameters

The spreadsheet takes the provided information and displays the details of power consumption for the chosen configuration.

As the spreadsheet is being configured, the settings are checked for conflicts, e.g., peripheral clock frequency out of allowed range, etc. For best results, enter the information from left to right starting at the top and moving downward.

2.1 Choosing Appropriate Values

The frequency and bit user values are determined by design and it will be clear what the correct values to enter are. For some modules, the frequency field is used to input the data rates (for instance, ATA, EMAC, etc). In order to choose appropriate values, you need a good understanding of read/write balance, bit switching required estimation, and utilization of the user application. You should also keep in mind the pin multiplexing configuration for the device to avoid enabling mutually exclusive peripherals/configurations at the same time. For available peripherals and peripheral configuration, see the device-specific data manual.

2.1.1 Utilization

For modules except DSP, C64x+™ and VCIP, utilization is simply the percentage of time the module spends doing something useful, versus being unused or idle. For these peripherals, there are not various degrees of use, so the value is just an average over time. For example, the EMIF performs reads and writes one-quarter of the time and has no data to move for the other three-quarters of the time (though it continues to perform background tasks like refresh); this would be 25% utilization.

For peripherals with I/O, utilization can be estimated by comparing used bandwidth with theoretical maximum bandwidth. If, for example, an application must transfer 160 Kb/s via the I2C port, with a theoretical 400 Kb/s maximum, the I2C port utilization would be about 40%. Similarly for ATA, when the DM6467T is running at 1 GHz, the max theoretical bandwidth possible is 99 Mbytes/sec in UDMA5 mode, so for an application using UDMA4 mode (expected bandwidth of around 66 Mbytes/sec), the % utilization would be 66.6%. In some cases, the max bandwidth allowed may be dependent on the device (SYSCLK1) frequency; factor this while calculating the utilization if doing the estimation at different device frequencies.

The CPU utilization is not as straightforward because there are varying degrees of use for the CPU. Here, 0% utilization means the CPU is active and does no useful work (NOP execution), where 100% utilization means all eight functional units are active every cycle and the maximum amount of data is brought in from L1P and L1D every cycle. Few DSP algorithms achieve 100% utilization because this requires everything to be used every cycle with no stalls. Even intense applications do not spend all of the time in such highly parallel loops. Time is typically also spent executing control code or less demanding algorithms. These types of code may execute only a few instructions in parallel and significantly reduce the I/O of the CPU, thus, reducing overall utilization. Since you must consider the balance of CPU use for the application, entering 100% utilization is not practical for real applications.

For example, an application that executes very dense CPU code (estimated at 90% of CPU capability) half of the time, and for the other half low activity, like waiting for commands from ARM along with some other house keeping activities (estimated at 10% of CPU capability), this application would have an average utilization of about 50% (10% × 50% + 90% × 50%). If the balance were changed to 25% low activity code and 75% DSP code, the weighted average would be about 70% utilization (25% × 10% + 90% × 75%). If the 25%/75% ratio is kept, but the DSP code does not fully use all the CPU resources (estimate now at 75% of CPU capability), then the overall utilization returns to about 59% (25% × 10% + 75% × 75%). An estimate of the overall CPU utilization can be obtained by using estimates of intensity and duration of blocks of code in the application.

System level issues may also reduce utilization. Though the spreadsheet accepts 100% utilization for all peripherals, this is not possible in reality. As concurrency in data movement increases and/or throughput requirements on high bandwidth modules (system DMA, VPIF, etc.,) increases, overall peripheral activity is throttled back due to bottlenecks created at various common end points. In such cases, peripherals might not achieve 100% utilization; therefore, you should enter individual module utilization numbers keeping this overall limitation in mind.

2.1.2 % Writes

Peripherals that transmit as much data as they receive have 50% writes; the spreadsheet assumes the remaining 50% of the time is spent on reads. In some applications, peripherals move data in only one direction, or have a known balance of data movement. In these cases, % writes should be changed to 0%, 100%, or the known ratio as appropriate for the cases when the DMSoC is reading all the time, writing all the time, or a combination of the two, respectively. Otherwise, 50% is a typical number that should be used.

2.1.3 % Switching

Random data has a 50% chance any bit will change from one cycle to the next. Some applications may be able to predict this chance using a priori information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. All other applications should use the default number of 50%.

2.2 Peripheral Enabling and Disabling

As mentioned previously, the DM6467T device provides the capability to disable modules that are not being used via the power sleep controller (PSC). When a peripheral is disabled, its clock is turned off reducing the power consumption of the device.

The spreadsheet accommodates this power saving feature by including fields from which a peripheral can be specified as disabled or enabled.

If a module is not used for a given application, then it is recommended to keep it in disabled state.

It is possible that the module is kept enabled but has no activity. To achieved this, program the % utilization and/or the frequency fields to a value of 0, then the numbers in the module's row will be indicative of the power consumed by clocking the module.

The DSP spreadsheet provides three states:

- Disabled: Indicates the *DSP* power domain OFF (DSP Subsystem clock gated off). This is also the default power-on reset condition in the *Host*-boot mode or DSP_BT =0 (see the *TMS320DM6467T Digital Media System-on-Chip Data Manual* (SPRS605) referred to as the DM6467T data manual throughout the remainder of this document).
- Idled: Indicates the DSP-sleep mode using the C64x+ internal power down controller (PDC)
- Active: Indicates the DSP state when it is not idled or powered down, you should put appropriate % utilization in this mode.

If DDR2 is enabled, then power estimation considers both DDR2 and PLL2 power; otherwise, it is assumed that the PLL2 is powered down and is operating in bypass mode with the DDR2 clock being directly fed by the input reference clock (33 MHz CLKIN).

If an application requires the use of VPIF, video data conversion engine (VDCE) and/or two TSIF modules in the system, this automatically implies that DDR2 is also enabled and active in the system. To estimate power for such scenarios, you need to make sure that the DDR2 fields are programmed with appropriate frequency and utilization, read/write percentage, etc., required by these modules.

2.3 Graphs

The output/results graphs in the spreadsheet provide a visual breakdown of the power consumption. A comparison is also provided of active power (based on the parameters supplied) and the baseline power, and pie charts show the relative contributions of each peripheral to the core and I/O power consumption.

The case temperature measurement spreadsheet shows worst case. Case temperature for an application and the heat sink calculation spreadsheet shows thermal impact adding a heat sink.

3 Using The Results

The intent of the power estimation spreadsheet is to provide estimates of the upper bounds in an application-specific loading and peripheral utilization scenario. The measured units were selected to be a strong unit at the maximum end of power consumption for production units. No production units will have average power consumption that exceeds the spreadsheet values; therefore, the spreadsheet data may be considered maximum average power consumption; the actual observed power may vary. That is, transient currents may cause power to spike above the spreadsheet value for a small amount of time; however, over a long period, the observed average consumption will be below the spreadsheet value. The spreadsheet value may be used for board thermal analysis and power supply design as a maximum long-term average.

3.1 Adjusting I/O Power Results

I/O power is dependent not only on the device and activity, but also the load being driven. For loads with CMOS inputs, the power required to drive the trace dominates, and is a better measure of load than the number of inputs or lumped load capacitance. If the target system has very different I/O loading, scale the spreadsheet results either up or down to compensate. For this reason, the spreadsheet allows you to specify the approximate load on the I/O pins for each module by using the trace length field. This parameter is used to adjust the reported I/O power numbers.

4 Example

The following examples demonstrate how to choose appropriate values for a particular application. These values may be imported into the spreadsheet by clicking the appropriate macro button.

4.1 Basic Configuration(s)

The *Static* macro button reports the static power for the device, when the MXI/CLKIN is cut off and voltage is applied to the various core and I/O rails

The *Standby* macro button reports the power consumed with the 33 MHz CLKIN. PLL1 is powered down/disabled and the system is operating in bypass mode with the CLKIN as the system clock. PLL2 is also powered down/disabled and is operating in bypass mode with the CLKIN passed through to DDR2 clock. The ARM is in the *wait for interrupt* sleep mode, the DSP subsystem power domain is OFF and all peripherals are disabled.

The macro button *1 GHz* can be used to quickly visualize the power number details at DSP 1 GHz, ARM 500 MHz and DDR-400 MHz shown in Table 1.

NOTE: In *Static* configuration, a *finite* current component is shown on the I/O rails (DV_{DD18} and DV_{DD33}), these values are system dependent and will differ (could be lower or higher) based on the state of pull up or pull downs and load on the device I/O lines.

4.2 Sample Application(s)

The *Sample Application* macro button reports the power consumed by the transcoding application. This application transcodes MPEG-2 HD into H.264 BP and streams these to a Wireless LAN enabled cell phone. HDVICP1 reads in a MPEG-2 1080i from a hard disk and decodes the MPEG-2 data content, VDCE scales it down to 480p and then HDVICP0 encodes it to H.264 BP. The transcoded stream is streamed out to a wireless LAN using RTSP protocol through EMAC. The cell phone receives the wireless stream and plays it using RealPlayer. Figure 1 shows a block diagram of this application.

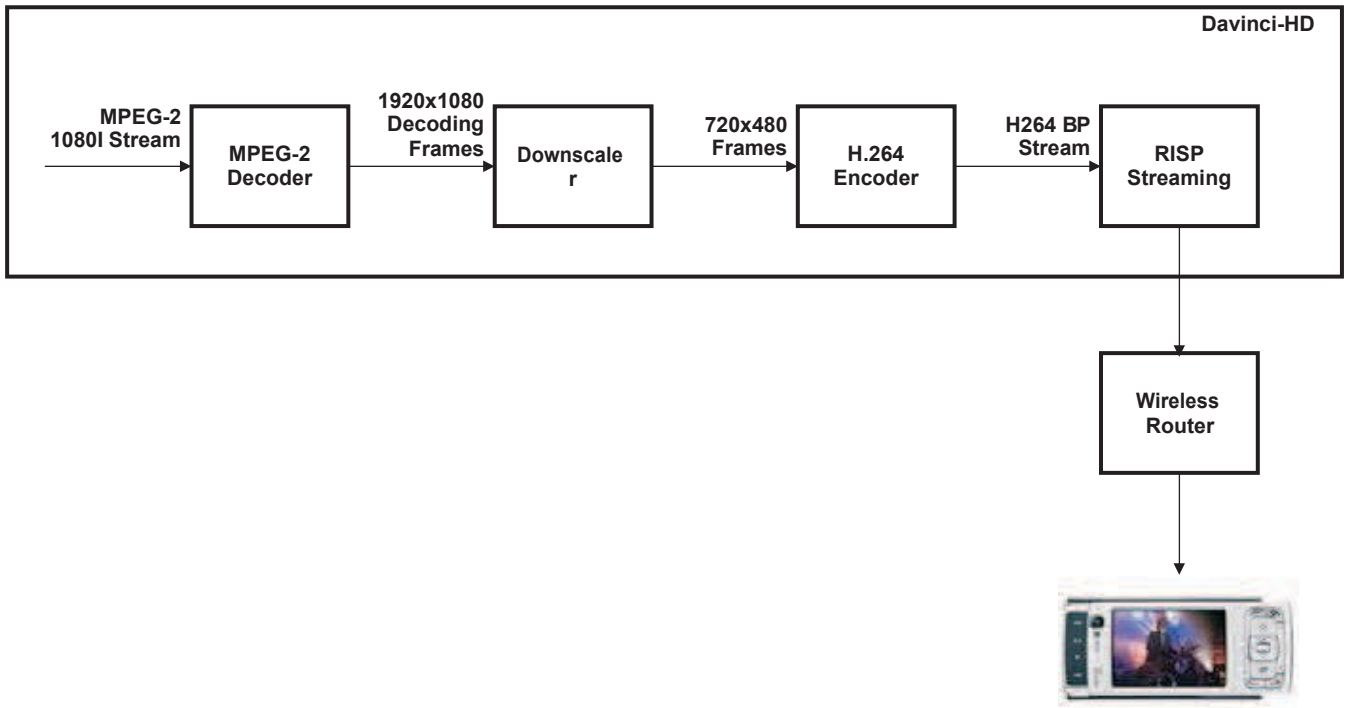


Figure 1. Sample Application(s) Block Diagram

The details of the peripherals used in this application are:

- Voltage: 1.3 V (CV_{DD} and CV_{DDDSP})
- Case temperature: 55°C
- CLKIN: 33 MHz
- ARM: *Typical activity* that involves configuring peripheral and other house keeping activities
- DSP: 1 GHz, 30% utilization. Estimation based on the following factors:
  – Background activities (waiting for commands from ARM, polling for response from HDVICP)
- HDVICP0: Enabled, 35% utilization
- HDVICP1: Enabled, 35% utilization
- VDCE: Enabled, 20% utilization
- DDR: Enabled, 20% utilization, 50% writes, 32% switching
- EMAC: Enabled, configured for 100 Mbps, 30% utilization
- All other modules are not used and disabled

Table 2 shows the approximate power estimation of this application calculated using the power spreadsheet.

Table 2. Power Consumption of HD-SD Transcoder Application

Core Voltage (V)	CPU Frequency	Power (Watts)				Case Temp
		Core	IO18	IO33	Total	
1.3	1 GHz	3.4510	0.3413	0.0991	3.8914	55°C

5 Thermal Considerations

As integrated circuit (IC) components become more complex, the challenge of producing an end equipment product with good thermal performance also increases. Thermal performance is a system level concern, impacted by IC packaging as well as printed circuit board (PCB) design, PCB characteristics, PCB layout, ambient temperature, and chassis configuration.

In the *TMS320DM6467T Digital Media System-on-Chip Data Manual* (SPRS605), TI specifies not to exceed the maximum operating junction temperature so that device reliability and/or proper operation can be maintained. To meet this requirement, it is important to understand the contribution of the other system characteristics (mentioned above) and design accordingly. Before finalizing system layout and PCB design, verify that the maximum operating junction temperature documented in the DM6467T data manual is met.

This section addresses the thermal considerations specific to the DM6467T device and should be used in conjunction with the *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9). The *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9) discusses many general thermal considerations that apply to DM64xx, DM64x, and C6000™ DSP devices. For more information regarding definitions of thermal terms, methods for calculating case temperature, recommendations for system thermal improvements, heat sink recommendations, and heat sink attachment methods, see the *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9).

One of the most commonly considered thermal improvement methods is the heat sink. A numerical approach that estimates the thermal impact of adding an off the shelf heat sink purchased from a vendor is shown below. This method requires ambient temperature, case temperature, and DM6467T power to be either measured or estimated without a heat sink in the real system. To be consistent with JEDEC measurement techniques, as well as to reference the most independent and static temperature point, TI recommends measuring the final system ambient temperature outside the enclosure; the inside the enclosure may be influenced by heating from other parts.

The spreadsheet that accompanies this application report includes a worksheet that performs the calculations described in the following heat dissipation examples. You must enter values for the following fields in the worksheet: package type, ambient temperature, case temperature, total power, and θ_{CA} from a heat sink data sheet. All of the remaining fields in the worksheet are calculated based on your inputs.

5.1 Thermal Heat Dissipation Example for the ZUT Package

Numbers for an actual application need to be calculated. From system analysis, suppose you determine:

- Ambient temperature: T_A = 25°C
- Case temperature: T_C = 70°C
- Device power = 2.0 W

NOTE: This is a reasonable example, but your specific information is required.

This is a reasonable example, but your specific information is required.

1. Calculate an estimate of $\theta_{JA,effective}$ using the following equation. Plug in values for ambient temperature, case temperature and device power from the list above. For the DM6467T, Ψ_{JT} = 0.3 °C/W at 0 m/s air flow. Ψ_{JT} is documented in the *TMS320DM6467T Digital Media System-on-Chip Data Manual* (SPRS605).

$$T_J = T_C + (\text{Power} \times \Psi_{JT}) = 70 + [2.0\text{W} \times 0.3\ ^{\circ}\text{C/W}] = 70.60\ ^{\circ}\text{C}$$

$$\theta_{JA,\ effective} = \frac{T_J - T_A}{\text{Power}} = \frac{70.60 - 25}{2} = 22.8\ ^{\circ}\text{C/W}$$

2. Estimate the percentage of heat flowing through the PCB vs. the top of the device. Based on experience with typical systems, TI estimates 80% of the heat flow is through the PCB, without a heat sink attached. The thermal resistance through the top and bottom of the device are two parallel resistances that equal $\theta_{JA,effective}$ (see Figure 2). Therefore, θ_{top} and θ_{bot} can be defined as follows:

$$\frac{80\%}{20\%} = 4 \text{ therefore, } \theta_{top} = 4 \times \theta_{bot}$$

$$\theta_{JA,\ effective} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bpt}}} = \frac{1}{\frac{1}{4\theta_{bot}} + \frac{1}{\theta_{bot}}}$$

$$1.25 \times \theta_{JA,\ effective} = \theta_{bot} = \frac{1}{4} \times \theta_{top}$$

$$5 \times \theta_{JA,\ effective} = \theta_{top}$$

Use the following equations to calculate θ_{top} and θ_{bot}:

$$\theta_{top} = \theta_{JA,\ effective} \times 5 = 22.8 \times 5 = 114\ ^{\circ}\text{C/W}$$

$$\theta_{bot} = \theta_{JA,\ effective} \times 1.25 = 22.8 \times 1.25 = 28.5\ ^{\circ}\text{C/W}$$

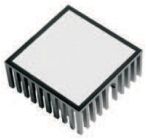
Check by calculating the parallel resistance of θ_{top} and θ_{bot}.

$$\theta_{JA,\ effective} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bot}}} = \frac{1}{\frac{1}{114} + \frac{1}{28.5}} = 22.8\ ^{\circ}\text{C/W}$$

3. Use the following equation to estimate the thermal resistance from the top of the DM6467T to the environment. This thermal resistance is called θ_{CA} (see Figure 2). For the DM6467T, θ_{JC} = 1.5 °C/W. θ_{JC} is documented in the *TMS320DM6467T Digital Media System-on-Chip Data Manual* (SPRS605).

$$\theta_{CA} = \theta_{top}\ (\text{step2}) - \theta_{JC} = 114 - 1.5 = 112.5\ ^{\circ}\text{C/W}$$

4. Replace θ_{CA}, calculated in step 3, with θ_{CA} specified from a heat sink data sheet and then recalculate the heat flow through the top of the device with a heat sink added. Note that θ_{CA} and θ_{top} should be reduced with the addition of a heat sink.
   For this example we chose a heat sink with θ_{CA} = 62.5 °C/W (for example heat sink).



Width	Length	Height	Fin Thickness Across Width	Fin Thickness Across Length	Base Thickness	# of Fins Across Width	# of Fins Across Length
15.20 mm	15.20 mm	6.35 mm	0.89 mm	0.89 mm	1.52 mm	8	8

Figure 2. Heat Sink Example Information

$$\theta_{top}\,(w/HS) = \theta_{CA}\,(\text{from HS}) + \theta_{JC} = 62.5 + 1.5 = 64.0\ \frac{^{\circ}C}{W}$$

5. Calculate the new $\theta_{JA,effective}$ with a heat sink as well as the improved T_C.

$$\theta_{JA,\,effective} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bot}}}$$

$$\theta_{JA,\,effective}\,(w/HS) = \frac{1}{\frac{1}{64} + \frac{1}{28.5}} = 19.72\ \frac{^{\circ}C}{W}$$

The new TC with heat sink can be calculated as follows:

$$T_J = T_A + \left(\text{Power} \times \varepsilon_{JA,\,effective}\right) = 25 + (2.0 \times 19.72) = 64.44\ ^{\circ}C$$

The heat sink in this application is estimated to improve the junction temperature from a value of 70.60°C to a value of 74.44°C.

NOTE: This example uses published data from an off-the-shelf heat sink. The same type of method can be used to estimate the impact of using a chassis as a heat sink, but the calculation is more difficult because this is not published data.

6 Limitations

The current implementation of the power estimation spreadsheet has the following limitations:

- ARM CPU power representation and reporting: ARM mega module power consumption estimation does not follow the traditional CPU usage parameters (like the DSP), and is currently broken into three main categories
  - Sleep Mode: Special *wait-for-interrupt* sleep mode
  - Low Activity: This is representative of ARM just performing low activity instructions (NOPs, etc.)
  - Typical Activity: This is representative of ARM performing typical activity, which would include peripheral configurations, load/stores and other house keeping activities (waiting for transfer completions, interrupts, etc.)
- USB2.0 Power representation: The USB2.0 module power consumption is based on modeled estimates and not actual measurements. Currently, the spreadsheet just allows you to estimate the core power consumed on enabling the USB2.0 module via PSC (and variations with device frequency). For USB /IO power, typical worst case *expected* numbers are provided for different usage modes (high-speed receive/transmit and full-speed receive/transmit).
- All measurements have been performed with a 33 MHz CLKIN provided by an external oscillator. The spreadsheet does not provide a capability of estimating power based on a different CLKIN value.

7 References

- *TMS320DM6467TDigital Media System-on-Chip Data Manual* (SPRS605)
- *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8)
- *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871)
- *TMS320DM644x Power Consumption Summary* (SPRAAD6)
- *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9)

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