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TMS320F280x to TMS320F2802x/TMS320F2803x Migration

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ABSTRACT

This application report describes differences between the Texas Instruments TMS320x280x/2801x/2804x and TMS320F2802x/2803x microcontrollers to assist in application migration. While the main focus of this document is migration from 280x/2801x/2804x to 2802x/2803x, you will also find this document useful if you are considering migrating in the reverse direction. Functions that are identical in both devices are not necessarily included. All efforts have been made to provide a comprehensive list of the differences between the two device groups in the 28x generation.

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1 Introduction

The TMS320x280x, TMS320x2801x, TMS320x2804x devices are members of the C2000™ MCU platform for use within embedded control applications. The TMS320x2802x and TMS320x2803x features the same enhanced control peripherals available on the TMS230x280x, 2801x and 2804x devices. In addition, the 2802x/2803x features internal zero-pin oscillators, internal voltage regulator, control law accelerator (CLA), analog comparators, local interconnect network (LIN), dual edge controlled HRPWM and low pin-count. These new peripherals and features enable the firmware engineer to solve challenging control problems effectively.

For purposes of migration, these devices can be thought of in two groups:

- TMS320x280x, TMS320x2801x and TMS320x2804x. This group will be referenced as 280x/2801x/2804x.
- TMS320x2802x and TMS320x2803x. This group will be referenced as 2802x/2803x.

As the focus of this document is to describe the differences between the two device groups, the descriptions are explained only to the extent of highlighting areas that require attention when moving an application from one device to the other. For a detailed description of features specific to each device, see the device-specific data manuals and user guides available on the TI website at http://www.ti.com/. This document does not cover the silicon exceptions or advisories that may be present on each device. Consult the following silicon errata for specific advisories and workarounds:

- *TMS320F280x, TMS320C280x, and TMS320F2801x DSC Silicon Errata* (SPRZ171)
- *TMS320F28044 DSP Silicon Errata* (SPRZ255)
- *TMS320F28020, TMS320F28021, TMS320F28022, TMS320F28023, TMS320F28026, TMS320F28027 Piccolo MCU Silicon Errata* (SPRZ292)
- *TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo MCU Silicon Errata* (SPRZ295)

> **NOTE:** Always refer to the TMS data manual for information regarding any electrical specifications.

1.1 Abbreviations

The following abbreviations are used in this document:

- 280x: Refers to the TMS320x280x devices. For example, TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2801 and TMS320C2802. The individual parts in this group are abbreviated 2809, 2808, 2806, 2802 and 2801.
- 2804x: Refers to the TMS320x2804x devices. For example, TMS320F28044.
- 2801x: Refers to the TMS320x2801x devices. For example, TMS320F28015 and TMS320F28016. Individual parts are abbreviated 28015 and 28016.
- 280x/2801x/2804x: Refers to the group of devices made up of TMS320x280x, TMS320x2801x and TMS320x2804x. For the purpose of migration, these three device families are very similar and can be thought of as one group.
- 2802x and 2803x: Refers to the TMS320F2802x and TMS320F2803x devices.

For a full list of devices currently available within the 2802x, 2803x, 280x, 2801x and 2804x family, see the TI website.

2   Central Processing Unit (CPU)

For 2802x/2803x, the main C28x CPU is the same fixed-point CPU as on 280x/2801/2804x devices. Some 2803x devices also provide a control law accelerator (CLA) that is independent of the main CPU.

2.1   Control Law Accelerator (CLA)

There is the C2000™ CLA that is new to the C2803x devices only. The CLA is a fully-programmable, 32-bit floating-point math processor. By operating in parallel with the main CPU, the CLA brings concurrent control-loop execution to the C28x DSP generation. The low interrupt-latency of the CLA allows it to read analog-to-digital converter (ADC) samples *just-in-time*. This significantly reduces the ADC sample to output delay to enable a faster system response and higher MHz control loops. By using the CLA to service time-critical control loops, the main CPU is free to perform other system tasks such as communications and diagnostics.

The main features of the CLA on the 2803x devices include:

- Clocked at SYSCLKOUT
- Fully programmable using 32-bit floating-point instructions
- Operates independently of the main CPU
- Interrupt driven with a low interrupt latency
- Responds to ADC, enhanced pulse width modulator (ePWM) and CPU Timer 0 interrupts
- Direct access to ADC result, comparator and ePWM+HRPWM registers
- Easily debugged in Code Composer Studio™ software through the same JTAG port as the main CPU

For more details on the CLA, see the *TMS320x2803x Piccolo Control Law Accelerator Reference Guide* (SPRUGE6). There is no CLA on the 2802x devices.

3   Development Tools

A new set of header files and peripheral examples are available for the 2802x and 2803x devices with the same structure as the 280x/2801x/2804x header files. For more information, see the *2802x C/C++ Header Files and Peripheral Examples* (SPRC832) and *2803x C/C++ Header Files and Peripheral Examples* (SPRC892).

Current C2000 emulation pods work with the C2802x and C2803x. As of this writing, the latest compiler is V5.2.0. 2803x CLA based assembly code requires C28x codegen tools V5.2.0 or later. Check the Code Composer Studio update advisor for future updates. CLA debugging capability is integrated in to Code Composer Studio.

4   Package and Pinout

The two device groups are neither package nor pin-compatible. Any application being moved from one to the other requires a new board layout to accommodate the changes in the pinout and the package.

5   Operating Frequency and Power Supply

The 280x devices require a 1.8-V nominal core voltage at all operating frequencies with a top operating frequency of 100 MHz. Some of the 280x and 2801x devices are also available in a 60 MHz version. The 2802x/2803x are available as 60 MHz or 40 MHz devices. Either version can operate at 1.8-V or 1.9-V core voltage. Both device groups require a 3.3-V input/output (I/O) supply.

5.1   Single Power Supply Source

The 280x/2801x/2804x requires both a core and I/O supply, however, a single 3.3-V supply is only required to operate the 2802x/2803x. There is an internal voltage regulator, which is enabled via the $\overline{\text{VREGENZ}}$ pin that supplies the core voltage on the 2802x/2803x.

> **NOTE:**   Always refer to the TMS data manual for information regarding any electrical specifications.

See the following data manuals for the most recent detailed electrical specifications:

- *TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801, and TMS320F2801x DSPs Data Manual* (SPRS230)
- *TMS320F28044 Digital Signal Processor Data Manual* (SPRS357)
- *TMS320F28020, TMS320F28021, TMS320F28022, TMS320F28023, TMS320F28026, TMS320F28027 Piccolo Microcontrollers* (SPRS523)
- *TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo Microcontrollers* (SPRS584)

6 Power Sequencing

Power sequencing requirements are identical for both device groups. That is, the V_{DDIO} and V_{DD} rail can ramp together. However, on 2802x/2803x there is no danger of the I/O pins glitching on startup if V_{DDIO} precedes V_{DD}.

See the appropriate data manual for each device for details related to power sequencing:

- *TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801, and TMS320F2801x DSPs Data Manual* (SPRS230)
- *TMS320F28044 Digital Signal Processor Data Manual* (SPRS357)
- *TMS320F28020, TMS320F28021, TMS320F28022, TMS320F28023, TMS320F28026, TMS320F28027 Piccolo Microcontrollers* (SPRS523)
- *TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo Microcontrollers* (SPRS584)

7 Memory Map

The memory maps are similar except for the changes described in this section.

7.1 SARAM

This section highlights the major differences in the SARAM memory subsystem.

- **Decreased Amount of SARAM**

  On the 280x/2801x/2804x, up to 18K x 16 words of SARAM are available. On 2802x, up to 6K x 16 words of SARAM are available. On 2803x, up to 10K x 16 words of SARAM are available.

- **Maximum SARAM Block Size 4K x 16**

  The maximum size of an SARAM block is now 4K x 16. The smaller memory blocks make it easier to partition code and data.

- **SARAM Blocks are Dual-Memory Mapped**

  L0 Memory block is dual mapped into both high memory and low memory in 2802x/2803x devices. On the 280x/2801x/2804x, L0 and L1 are mirrored. The dual mapping of the memory gives flexibility when partitioning code as required by the application. The memory region in the upper 64K range is required when running 24x compatible code, while the stack pointer (SP) can only access memory in the lower 64K. If the application is not porting 24x code, then either memory map location can be used for either data or code. Keep in mind that the stack pointer can still only access the lower 64K range.

- **Wait States**

  On 280x/2801x/2804x and 2802x/2803x, all SARAM blocks are 0 wait state in both program and data space.

Table 1. SARAM Addresses

Memory Address [1]	280x/2801x/2804x Memory Block	2802x Memory Block	2803x Memory Block
0x00 8000 – 0x00 8FFF	L0	L0	L0/L1/L2
0x00 9000 – 0x00 9FFF	L1	N/A [2]	L3
0x3F 8000 – 0x3F 8FFF	L0 Mirror	L0 Mirror	L0 Mirror
0x3F 9000 – 0x3F 9FFF	L1 Mirror	N/A	N/A
0x3F A000 – 0x3F BFFF	H0	N/A	N/A
Reserved locations during bootload process	0x400 - 0x44F	0x0002 - 0x004E	0x0002 - 0x004E

[1] Some SARAM blocks may not be available on some family derivatives. For more information, see the device-specific data sheets.

[2] N/A = Not available.

7.2 *Flash and One-Time Programmable (OTP)*

This section highlights the major differences in the Flash and OTP memory subsystem.

7.2.1 Size and Number of Sectors

The size and number of sectors has changed so the code must be rebuilt accordingly. The exact Flash size as well as sector configuration varies from device to device as shown in Table 2.

Table 2. Sector Configuration Per Device

	F2809	F2808 F28044	F2806 F2802	F2801 F28016 F28015	F28027 F28025 F28023 F28021	F28026 F28024 F28022 F28020	F28035 F28034	F28033 F28032
	8 Sectors 16K X 16	4 Sectors 16K X 16	4 Sectors 8K X 16	4 Sectors 4K X 16	4 Sectors 8K X 16	4 Sectors 4K X 16	8 Sectors 8K X 16	8 Sectors 4K X 16
Total	128K X 16	64K X 16	32K X 16	16K X 16	32K x 16	16K x 16	64K x 16	32K x 16

7.2.2 Flash Access Time

The access time of the Flash has increased by 4 ns. Depending on your CPU speed, you may need to update the waitstates accordingly.

> **NOTE:** Always refer to the device-specific data manual timing information.

7.2.3 Entry Point Into Flash and CSM Password Locations

On both device groups, the boot ROM entry point and code security module password locations are located at the highest addresses of sector A.

7.2.4 Entry Point Into OTP

On both device groups, the boot ROM entry point into the OTP is the first address within the OTP.

7.2.5 Flash Programming

The method for programming the device remains the same. TI supplies a Flash application programming interfaces (API) per device that is used as the basis of all programming solutions. The Flash API and programming algorithms for the F280x/F2801x/F2804x devices cannot be used on the F2802x/F2803x. New Flash APIs are required to program these devices; however, the Flash API function prototypes remain compatible.

> **NOTE:** The Flash API includes timing critical delay loops. These loops should always be run from 0 wait memory in order to be timing accurate..

7.3 Boot ROM

This section describes the major functional differences between the 280x/2801/2804x and 2802x/2803x boot ROMs. Some of the enhancements found on the 2802x/2803x include:

*   Additional IQmath tables
*   Inclusion of selected IQmath functions
*   Inclusion of the Flash API
*   24-bit addressable serial peripheral interface (SPI) flash support
*   Ability to program a specified-boot mode by programming OTP locations
*   The boot ROM on 2802x/2803x calibrates the ADC and on-chip oscillators as described in Section 9.2.

7.3.1 Boot ROM Memory Location

On 280x devices, the boot ROM reserved memory is the first 80 words starting at 0x400. On 2802x/2803x devices, the boot ROM is the first 80 words starting at address 0x0002. Take care not to allocate code or data to these memory locations.

Boot ROM reserved memory (used for stack, .ebss) used during the bootload process:

*   On F280x, F2801x, F2804x devices, addresses 0x400 - 0x44F are reserved during bootload process
*   On F2802x devices, addresses 0x0002 - 0x004E are reserved during bootload process
*   On F2803x devices, addresses 0x0002 - 0x004E are reserved during bootload process

7.3.2 Boot-Mode Selection

The boot-mode selection on the 280x/2801/2804x devices is done by configuring three GPIO pins at boot up. These three pins always determine the boot mode of the device.

For 2802x/2803x, the boot mode is determined by the state of $\overline{TRST}$ and two GPIO pins.

If $\overline{TRST}$ is high, then the boot ROM assumes that an emulator is connected. In this case, the boot ROM uses two locations in RAM to determine the boot mode. You can modify these locations to invoke any of the boot modes. If $\overline{TRST}$ is low, then the boot ROM assumes that an emulator is not connected. In this case, two GPIO pins are used to determine the boot mode. By default the modes on 2802x/2803x are:

*   Parallel GPIO
*   Serial Communication Interface (SCI)
*   Wait
*   GetMode

The parallel GPIO and SCI are similar to those on the 280x/2801/2804x. The Wait mode and GetMode were not supported on 280x/2801/2804x. Wait is used to emulate a *wait-in-reset* mode, which must be used when trying to connect an emulator when the code security module password is programmed. The GetMode option reads two locations in the OTP memory (0x3D 7BFE and 0x3D 7BFF) to determine the boot mode. The default for GetMode is to branch to Flash.

7.3.3   Bootloaders

On the 280x/2801/2804x, all possible boot options can be invoked by using three GPIO pins at boot time. On the 2802x/2803x, only the emulation, parallel GPIO, SCI, Wait and GetMode options can be invoked by pins. If you want to use one of the other bootloaders, program the OTP locations 0x3D 7BFE and 0x3D 7BFF for the GetMode boot option. All of the boot loaders can also be accessed during debug by using the emulation boot RAM locations at addresses 0xD00 and 0xD01.

The boot ROM in 280x/2801/2804x devices do not support the CAN bootload option. The 2803x devices support this option. The CAN bootloader configures the CAN for 100 kbps operation. Since one of the boot-mode select pins (TDO) is part of JTAG, the following approach can be used if debugger connection is desired while testing the bootloader: Load 0x55AA @ 0xD00 and 0x0007 @ 0xD01. After a reset, this forces the boot-ROM to branch to the CAN boot-loader.

The SPI-A bootloader has been updated to support both serial 16-bit addressable EEPROMs and 24-bit addressable SPI Flash.

Parallel GPIO boot on the 2803x and 2802x devices is limited to an 8-bit input data stream. The 280x/2801/2804x offer both 16- and 8-bit data streams. The data lines and handshake lines are different on all three device types: 280x/2801/2804x, 2802x and 2803x.

7.3.4   IQmath Routines and Tables

The 2802x/2803x devices have selected IQmath functions programmed into the ROM. These include: IQNatan2(), IQNcos(), IQNdiv(), IQNisqrt(), IQNmag(), IQNnsin(), IQsqrt() for N = 15, 20, 24 and 29. These functions can be called directly from the application.

The boot-ROM IQmath tables have been extended to include tables used by the IQNexp(), IQNasin() and IQNacos() functions.

For more information on the boot ROM, see the following reference guides:

- *TMS320x280x, 2801x, 2804x Boot ROM Reference Guide* (SPRU722)
- *TMS320x2802x Piccolo Boot ROM Reference Guide* (SPRUFN6)
- *TMS320x2803x Piccolo Boot ROM Reference Guide* (SPRUGO0)

8   Clocks and System Control

This section describes changes that affect device clocking and system control. This includes new and renamed registers, pin functionality, new logic, and other enhancements. For more information on system control, see the following reference guides:

- *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (SPRU712)
- *TMS320F2802x Piccolo System Control and Interrupts Reference Guide* (SPRUFN3)
- *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* (SPRUGL8)

8.1 Register Changes

Table 3 shows a summary of registers that were added, renamed, or modified. The following sections describe changes that were made.

Table 3. New, Updated, and Removed Registers

Register	Change	Description
XCLK	Updated	XCLKINSEL bit is added to select between GPIO38 and GPIO19 for the XCLKIN input source.
PLLSTS	Updated	CLKINDIV (single bit) is now DIVSEL (two bits) in PLLSTS. MCLKSTS bit gets automatically cleared when the missing clock detection circuit switches to OSCCLKSRC1 from OSCCLKSRC2 upon the failure of OSCCLKSRC2. NORMRDYE bit is added to control the gating of phase-locked loop (PLL) using NORMRDY signal from VREG.
CLKCTL	New	New register to select the source for OSCCLK, WDCLK, CPU Timer 2. This register supports control to turn off internal zero-pin oscillators, external -XCLKIN oscillator input and external crystal oscillator. This register supports control for internal zero-pin oscillators and watchdog to ignore halt mode. This register also supports control to select the generation of MCLKRSn either by the detection of missing clock condition or NMI watchdog reset.
PLLLOCKPRD	New	Programmable PLL lock counter period register. This register allows configuration of PLL lock time.
INTOSC1TRIM	New	New register that allows trimming of internal zero-pin oscillator 1
INTOSC2TRIM	New	New register that allows trimming of internal zero-pin oscillator 2
PCLKCR0	Updated	Removed clock enable/disable bits for peripherals that do not exist. 2802x only: Updated to support HRPWM clock enable/disable bit. 2803x only: Updated to support clock enable/disable bit for HRPWM, LINA.
PCLKCR1	Updated	Removed clock enable/disable bits for peripherals that do not exist.
PCLKCR2	Removed	Enable/disable clocks to ePWM modules.
PCLKCR3	New	2802x only: New register supports enable/disable clocks for COMP1, COMP2, CPUTIMER0, CPUTIMER1, CPUTIMER2 and GPIOIN. 2803x only: New register supports enable/disable clocks for COMP1, COMP2, COMP3, CPUTIMER0, CPUTIMER1, CPUTIMER2, GPIOIN and CLA.
PLLCR	Updated	In 2802x, DIV can vary from 0 to 12 where as in 280x, 2801x, 2804x devices, DIV can vary from 0 to 10.
HISPCP	Removed	Removed HSPCLK bits that are used to configure the high-speed peripheral clock rate relative to SYSCLKOUT.
JTAGDEBUG	New	New register that allows enable/disable JTAG port.

8.2 Input Clock Options and Clock Control

2802x, 2803x devices have two zero pin internal oscillators in addition to Crystal/Resonator (X1/ X2) option and External oscillator (XCLKIN) option. Internal zero-pin Oscillator 1 is selected from reset as the default clock source. Nominal frequency of the internal oscillators is 10 MHz.

INTOSC1TRIM and INTOSC2TRIM registers are provided on 2802x, 2803x devices to allow trimming of internal zero-pin Oscillator 1 and internal zero-pin Oscillator 2 respectively. Internal oscillators provide clock for core, watchdog and CPU Timer 2. CLKCTL, a new clock control register is added to configure external and internal oscillator options.

On 2802x, 2803x devices, if XCLKIN clock source is not used or the respective pins are used as GPIOs, XCLKIN should be turned off using XCLKINOFF bit in CLKCTL register. On 2802x, 2803x devices, if external crystal/resonator is not used as the clock source, X1/X2 option should be turned off using XTALOSCOFF bit in CLKCTL register.

8.3 CLKIN Input Multiplier and Divider

On 280x/2801x/2804x, the PLL multiplier (PLLCR[DIV]) can be between 0 and 10. On 2802x/2803x devices, PLL multiplier can be between 0 and 12. On 2802x/2803x, the PLL output should be between 50 MHz and 400 MHz.

On 280x/2801x/2804x, the clock into the CPU is either equal to or one-half of the PLL output. This divider is controlled by bit 1 (CLKINDIV) of the PLL Status Register (PLLSTS). By default, PLLSTS[CLKINDIV] is configured for the divide-by-two (multiply by one-half) operation.

On 2802x/2803x, the divider is controlled by bits 7 and 8 (DIVSEL) of the PLLSTS register. The PLLSTS[DIVSEL] divider can be set to equal, one-half or one-fourth. By default, at power-up, the divider is set for 1/4. The 1/4 divider can be used to allow a more gradual step up of clocks and to reduce inrush current.

On 2802x/2803x, PLL lock period can be configured using the PLLLOCKPRD register to reduce the lock time.

> **NOTE:** The boot ROM changes PLLSTS[DIVSEL] so the loaders will run at the input clock. The boot ROM leaves the divider in this state, which is compatible with 280x/2801x/2804x.

8.4 Peripheral Clock Enable Registers

Due to new peripherals and additional instances of old peripherals, the registers to enable and disable the clocks to individual peripherals have been updated. For 2802x, 2803x devices, there is an additional register to enable and disable the clocks to the comparators, CPU Timers and GPIO input logic: Peripheral Clock Control Register 3 (PCLKCR3). For 2803x devices, the PCLKCR3 register has a clock enable/disable bit for CLA. Peripheral Clock Control Register 2 (PCLKCR2) is removed on 2802x/2803x devices. For 2802x devices, Peripheral Clock Control Register 0 (PCLKCR0) is updated to support HRPWM clock enable bit. For 2803x, PCLKCR0 is updated to add clock enable bits for LINA, HRPWM. All the peripheral clock enable registers are updated to remove clock enable/disable bits for peripherals that do not exist.

8.5 XCLKOUT Control

On 280x/2801x/2804x, XCLKOUT is a dedicated pin. On 2802x/2803x, XCLKOUT is brought out on a GPIO pin. On 280x/2801x/2804x, turning off XCLKOUT will put the dedicated XCLKOUT pin in high-impedance mode. On 2802x/2803x, it is up to you to configure GPIO as input or output and/or enable/disable pull-up on pin.

8.6 XCLKIN Source Selection

A source select bit for the XCLKIN pin (XCLKINSEL) is added in the XCLK register to select from two possible pin sources for the XCLKIN signal. XCLKIN source should be selected when the device is running from the internal oscillator.

8.7 Clock Pre-scalar Registers

On 2802x, 2803x devices, HISPCP clock pre-scale is removed and ADC is clocked directly from SYSCLK. CAN and the new LIN peripherals are clocked at a fixed /2 rate of SYSCLK. All other peripherals are clocked at the SYSCLK rate and all clock pre-scalers are contained within the peripherals.

8.8 Non-Maskable Interrupt (NMI) Watchdog

On 280x/2801x/2804x devices, MCLKRSn is generated automatically upon missing clock detection. On 2802x, 2803x devices, a CLOCKFAILn interrupt is fed to NMI watchdog logic and NMI watchdog logic can be configured to fire MCLKRSn.

8.9 VREG/POR/BOR

2802x/2803x devices are provided with an on-chip voltage regulator (VREG) to generate V_{DD} voltage from V_{DDIO} supply. The $\overline{VREGENZ}$ signal can be pulled high to disable VREG and, in this case, an external regulator can be used to supply core logic voltage to V_{DD} pins.

On 2802x/2803x devices, internal power-on reset (POR) and brown-out reset (BOR) circuits monitor both the V_{DD} and V_{DDIO} rails during power-up and run mode, eliminating a need for any external voltage supervisory circuits. Additionally, V_{DD} rail has an overvoltage circuitry on 2802x/2803x. When monitoring the V_{DD} rail, the BOR pulls XRS low when V_{DD} is above its overvoltage trip point. BOR and overvoltage circuits for V_{DD} rail are not active when $\overline{VREGENZ}$ is high.

8.10 Low Power

The low-power modes remain the same: idle, halt and standby. On 280x/2801x/2804x devices, the XNMI signal can be used to exit idle mode. XNMI signal is not the in 2802x/2803x devices.

2802x/2803x devices provide two options to automatically wake up from HALT and STANDBY modes, without the need for an external stimulus. For more information, see the *Options for Automatic Wakeup in Low-Power Modes* section in *TMS320x2802x Piccolo System Control and Interrupts Reference Guide* (SPRUFN3) and *TMS320x2803x Piccolo System Control and Interrupts Reference Guide* (SPRUGL8).

The CPU Timer clocks can now be disabled in the PCLKCR3 register. The CPU Timer clocks are enabled by default to be compatible with 280x/2801x/2804x.

Another new clock control is the GPIOINENCLK bit in PCLKCR3. When this bit is cleared, the input path of the GPIO will be disabled if the pin is configured as an output. This can be used to lower power when the pin is used as an output. Clearing the GPIOINENCLK bit resets the synchronization and qualification logic. By default, GPIOINENCLK is enabled, which is compatible with the 280x/2801x/2804x.

> **NOTE:** When GPIOINENCLK is disabled, the GPIO input logic is turned off for any pin configured as an output. This means the respective bit in the DAT register is an undefined value and can not be used to read the current state of the pin.

On 2802x/2803x devices, WDCLK should be configured for the same source as the CPU clock when entering HALT and STANDBY modes.

9   Peripherals

This sections briefly describes peripherals that have been added and/or updated. For an overview of all peripherals available, see the *TMS320x28xx, 28xxx Peripherals Reference Guide* (SPRU566).

9.1   New Peripherals

The 2802x/2803x devices include new peripherals that are not available on the 280x/2801x/2804x devices.

9.1.1   Core Voltage Regulator (VREG)

The 2802x/2803x has an internal voltage regulator to supply the 1.9-V core voltage so that the device can be powered from a single 3.3-V supply. The VREG can be enabled or disabled through the $\overline{VREGEN\ Z}$ pin. For more information, see the following reference guides:

- *TMS320F2802x Piccolo System Control and Interrupts Reference Guide* (SPRUFN3)
- *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* (SPRUGL8)

9.1.2   Power-On Reset Protection (POR)

The 2802x/2803x has an internal power-on reset supervisor. For more information, see the following reference guides:

- *TMS320F2802x Piccolo System Control and Interrupts Reference Guide* (SPRUFN3)
- *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* (SPRUGL8)

9.1.3   Brown-Out Reset Protection (BOR)

The 2802x/2803x has an internal brown-out reset supervisor. For more information, see the following reference guides:

- *TMS320F2802x Piccolo System Control and Interrupts Reference Guide* (SPRUFN3)
- *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* (SPRUGL8)

9.1.4   Zero-Pin Internal Oscillators

The 2802x/2803x has two zero-pin internal oscillators that are trimmed at the factory to 10 MHz and are fed into the PLL.

9.1.4.1   Internal Oscillator Calibration

On the 2802x/2803x, the internal oscillators are calibrated by the boot-ROM software at boot time. The Device_Cal() routine is programmed into TI-reserved OTP memory by the factory. The boot ROM automatically calls the Device_Cal() routine to initialize the oscillator trim registers (OSCCOARSETRIM and OSCFINETRIM) with device-specific calibration data. During normal operation, this process occurs automatically and no action is required by you. If the boot ROM is bypassed by the Code Composer Studio during the development process, then the oscillator trim registers must be initialized by other methods, such as the application or a Code Composer Studio GEL file. For more detailed information on the Device_Cal() function, see the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (SPRUGE5).

9.1.5   Comparator/Digital-to-Analog Converter (DAC)

The 2802x/2803x has a comparator/DAC block. The 2802x has two comparator/DAC blocks, and the 2803x has three. The comparators are asynchronous analog comparators that feed to the ePWM trip zone block. The A and B input pairs to the comparators are accessed through the ADCIN channels. Also, the B-input terminal can be driven from an internal DAC. For more information, see the Comparator/DAC sections of the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (SPRUGE5).

9.1.6   Control Law Accelerator (CLA)

There is the C2000 CLA that is new to the C2803x devices only and described in Section 2.1.

9.1.7   Internal Temperature Sensor

The 2802x/2803x has an internal temperature sensor that can be sampled by the internal ADC via a MUX selection. The temperature sensor connection to the ADC is done internally such that any circuitry attached externally to the ADCIN pin is not disturbed. For more detailed information on the temperature sensor, see the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (SPRUGE5).

9.2   *Analog-to-Digital Converter (ADC)*

The ADC, on the 2802x/2803x, is documented in the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (SPRUGE5). The changes in the ADC from the 280x/2801x/2804x are as follows:

- **ADC Calibration**

   On the 2802x/2803x, the ADC is calibrated by the boot ROM software at boot time. The Device_Cal() routine is programmed into TI-reserved OTP memory by the factory. The boot ROM automatically calls the Device_Cal() routine to initialize the ADC Reference Select Register (ADCREFTRIM) and the ADC Offset Trim Register (ADCOFFTRIM) with device-specific calibration data. During normal operation, this process occurs automatically and no action is required by you. If the boot ROM is bypassed by the Code Composer Studio during the development process, then ADCREFTRIM and ADCOFFTRIM must be initialized by other methods, such as the application or a Code Composer Studio GEL file. For working examples and GEL files, see the ADC initialization in the *2802x C/C++ Header Files and Peripheral Examples* (SPRC832). For more detailed information on the Device_cal() function, see the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (SPRUGE5).

- **ADC Result Registers**

   On the 2802x/2803x, the ADC result registers are located starting at 0xB00 and are right aligned. The 280x/2801x/2804x had two result register locations: one left aligned and right aligned.

   The ADC results registers are accessible by both the CPU and CLA on the 2803x only. There is no CLA on the 2802x.

- **ADC Principle of Operation**

   Contrary to previous ADC types, this ADC is not sequencer based. Instead, it is SOC based. The term SOC is configuration set defining the single conversion of a single channel. In that set, there are three configurations: the trigger source that starts the conversion, the channel to convert, and the acquisition (sample) window size. Each SOC is independently configured and can have any combination of the trigger, channel, and sample window size available. Multiple SOC's can be configured for the same trigger, channel, and/or acquisition window as desired. This provides a very flexible means of configuration conversions ranging from individual samples of different channels with different triggers, to over-sampling the same channel using a single trigger, to creating your own series of conversions of different channels all from a single trigger.

   For more information on the ADC wrapper, see the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (SPRUGE5)

- **ADC Support Pins**

   The 280x/2801x/2804x had ADC support pin, ADCREFP, ADCREFM, and ADCRESEXT, which required specific external components tied to them. These pins are no longer needed in 2802x/2803x devices.

- **Minimum ADC Acquisition (Sample and Hold) Window**

   The 280x device's minimum ADC acquisition sample and hold window register value is 0, however on 2802x/2803x devices, the minimum register value is 6, which gives a sample/hold window of 7 (i.e., 6 cycles plus 1 hard coded cycle).

- **ADC Internal Reference Mode**

  The internal reference mode has a fixed analog input range of 0 V to 3.3 V, instead of 0 V to 3 V as on 280x. The digital value converted is governed by: Digital Value = 4096 [(Input – VREFLO)/3.3 v] when 0 V < Input < 3.3 V.

- **ADC External Reference Mode**

  The external reference for 280x was based only on a single pin, ADCREFIN. On 2802x/2803x devices, there are two external reference pins: VREFHI and VREFLO. On the packages where these signals are brought out to independent pins, the 2802x/2803x devices ADC is fully ratio-metric. The digital value converted is governed by: Digital Value = 4096 [(Input – VREFLO)/(VREFHI – VREFLO)] when VREFLO < Input < VREFHI.

- **Internal VREFLO Connection for Offset Error Correction**

  Previously on the 280x/2801x/2804x, the ADC offset error can be corrected by connecting an ADCIN pin externally to GND and adjusting the ADCOFFTRIM register accordingly. New to the 2802x/2803x, VREFLO can be sampled with the ADC instead of connecting GND to an external ADCIN pin, thereby saving that ADCIN pin for application use. The VREFLO connection to the ADC is done internally such that any circuitry attached externally to the ADCIN pin is not disturbed. For more detailed information on the internal VREFLO connection and how to use it to correct offset error, see the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (SPRUGE5).

9.3 Code Security Module (CSM)

9.3.1 F2802x Code Security Module (CSM)

This module protects the Flash, OTP, and L0/L1 SARAM blocks as it did on the 280x/2801x/2804x devices. On the 2802x/2803x, the module protects both mappings of the L0.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to Flash, user OTP, or L0 memory while the emulator is connected will trip the ECSL and break the emulation connection. To allow emulation of the secure code, while maintaining the CSM protection against secure memory reads, you must write the correct value into the lower 64 bits of the KEY register, which matches the value stored in the lower 64 bits of the password locations within the Flash. Note that dummy reads of all 128 bits of the password in the Flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match.

When initially debugging a device with the password locations in Flash programmed (i.e., secured), the CPU starts running and may execute an instruction that performs an access to a protected ECSL area. If this happens, the ECSL trips and causes the emulator connection to be cut. The solution is to use the Wait boot option. This will sit in a loop around a software breakpoint to allow an emulator to be connected without tripping security. You can exit this mode once the emulator is connected by using one of the emulation boot options as described in the *TMS320x2802x Piccolo Boot ROM Reference Guide* (SPRUFN6). Unlike, 280x/2801x/2804x devices, 2802x devices do not support a hardware wait-in-reset mode.

The CSM password is still the last 128 bits within sector A of the Flash. As in 280x/2801x/2804x, the password locations for 2802x is at 0x3F7FF8 - 0x3F7FFF.

CSM detailed information is included in the appropriate System Control and Interrupts Reference Guide:

- *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (SPRU712)
- *TMS320x2802x Piccolo System Control and Interrupts Reference Guide* (SPRUFN3)

9.3.2 F2803x Code Security Module (CSM)

This module protects the Flash, OTP, and L0/L1 SARAM blocks as it did on the 280x/2801x/2804x devices. On the 2803x, the module was extended to protect both mappings of the L0 as well as L1, L2 and L3.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to flash, user OTP, L0, L1, L2 (or) L3 memory while the emulator is connected will trip the ECSL and break the emulation connection. To allow emulation of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct value into the lower 64 bits of the KEY register, which matches the value stored in the lower 64 bits of the password locations within the flash. Note that dummy reads of all 128 bits of the password in the flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match.

When initially debugging a device with the password locations in flash programmed (i.e., secured), the CPU will start running and may execute an instruction that performs an access to a protected ECSL area. If this happens, the ECSL will trip and cause the emulator connection to be cut. The solution is to use the Wait boot option. This will sit in a loop around a software breakpoint to allow an emulator to be connected without tripping security. The user can then exit this mode once the emulator is connected by using one of the emulation boot options as described in the TMS320x2802x Piccolo Boot ROM Reference Guide (SPRUFN6). Unlike, 280x/2801x/2804x devices, 2803x devices do not support a hardware wait-in-reset mode.

The CSM password is still the last 128-bits within sector A of the Flash. As in 280x/2801x/2804x, the password locations for 2803x is at 0x3F7FF8 - 0x3F7FFF.

CSM detailed information is included in the appropriate System Control and Interrupts Reference Guide:

*   *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (SPRU712)
*   *TMS320x2803x Piccolo System Control and Interrupts Reference Guide* (SPRUGL8)

9.4 General-Purpose Input/Output (GPIO)

The GPIO multiplexing scheme is the same as the 280x/2801x/2804x devices. Additional ports have been added to support the additional GPIOs on the device. Register changes are shown in Table 4.

Table 4. New, Updated, and Removed Registers

Register	Change	Description
GPBCTRL	Updated	Added Support for GPIO36 to GPIO44
GPBQSEL1	Updated	Added Support for GPIO36 to GPIO44
GPBMUX1	Updated	Added Support for GPIO36 to GPIO44
GPBDIR	Updated	Added Support for GPIO36 to GPIO44
GPBPUD	Updated	Added Support for GPIO36 to GPIO44
GPBDAT	Updated	Added Support for GPIO36 to GPIO44
GPBSET	Updated	Added Support for GPIO36 to GPIO44
GPBCLEAR	Updated	Added Support for GPIO36 to GPIO44
GPBTOGGLE	Updated	Added Support for GPIO36 to GPIO44
GPIOXNMISEL	Removed	GPIO XNMI Interrupt Select Register
GPIOXINT3SEL	New	XINT3 GPIO Input Select Register
AIOMUX1	New	Analog, I/O MUX 1 register (AIO0 - AIO15)
AIODIR	New	Analog, I/O Direction Register (AIO0-AIO15)
AIODAT	New	Analog I/O Data Register (AIO0 - AIO15)
AIOSET	New	Analog I/O Data Set Register (AIO0 - AIO15)
AIOCLEAR	New	Analog I/O Data Clear Register (AIO0 - AIO15)
AIOTOGGLE	New	Analog I/O Data Toggle Register (AIO0 - AIO15)
GPAMCFG	Removed	2804x only: Selects the pinout configuration for the ePWM

9.4.1 GPIO Ports and MUX

There are three I/O ports. On 2803x, port A consists of GPIO0-GPIO31, port B consists of GPIO32-GPIO44 and the analog port consists of AIO0-AIO15. On 2802x, port A consists of GPIO0-GPIO31, port B consists of GPIO32-GPIO38 and the analog port consists of AIO0-AIO15. 2802x/2803x have additional GPIO pins in port B than that of 280x/2801x/2804x.

On 2802x, GPIO8 to GPIO11, GPIO13 to GPIO15, GPIO20 to GPIO27, GPIO30 to GPIO31, and GPIO39 to GPIO44 are not supported.

On 2802x/2803x, ADC channel inputs and comparator inputs are shared with digital I/Os referred to as AIOs. For information regarding the registers and bit definitions for controlling the AIOs, see the *General-Purpose Input/Output (GPIO)* section in the device-specific System Control and Interrupts Reference Guide.

On 2802x/2803x, XCLKIN can be sourced from GPIO19 or GPIO38.

On 2802x/2803x, the JTAG pins (GPIO35 to GPIO38) can also be used as GPIO pins.

9.4.2 GPIO Qualification

On 2802x/2803x devices, the type of qualification required for input signals on GPIOs can be specified by you just as it is on 280x/2801x/2804x. This qualification applies whether the pin is configured as a GPIO or peripheral.

9.4.3 External Interrupt Signal Selection

The 2802x/2803x devices have one more external interrupt XINT3. GPIO signals from port A (GPIO0-GPIO31) can be assigned to be the interrupt source for XINT3. For more information, see Section 10.3.

9.5 Communication Peripherals

The FIFO level on the serial communications interface (SCI) and inter-integrated circuit (I2C) modules has been reduced from 16 to 4. Otherwise, these modules remain functionally the same between the 280x/2801x/2804x devices and the 2802x/2803x devices. The register sets are identical on the two device groups. The memory addresses of the registers for each instance of peripheral are also identical. For example, the SCI-A registers on 280x/2801x/2804x are at the same location as SCI-A registers on 2802x/2803x. In addition, the interrupt vector locations in the PIE vector table are identical. There is no SCI-B on the 2802x/2803x, so code written for SCI-B on the 280x/2801x/2804x cannot be targeted for these devices.

The FIFO level on the serial peripheral interface (SPI) module on the 2802x/2803x devices has also been reduced from 16 down to 4. Additionally, there is a bi-directional 3-wire SPI option via the $\overline{\text{TRIWIRE}}$ bit in the SPIPRI register on these devices. The 2803x also includes an inversion option for the $\overline{\text{SPISTE}}$ pin (STEINV in SPIPRI register) that allows for left and right-channel digital audio data receive transfers via two SPI modules. This option is not available on the 2802x devices.

> **NOTE:** In *2802x C/C++ Header Files and Peripheral Examples* (SPRC832) and *2803x C/C++ Header Files and Peripheral Examples* (SPRC892) software packages, the AL bits in the I2C Interrupt Enable Register (I2CIER) and the I2C Status Register (I2CSTR) have been renamed ARBL bits. This is to allow the header files to an be used an assembly project where AL is a reserved word.

The 2803x eCAN is now clocked at one-half the SYSCLKOUT frequency, 280x/2801x/2804x, which clocks the eCAN module at SYSCLKOUT. Code written for the eCAN needs to take this timing change into account. Otherwise, the eCAN module is functionally the same and the register sets are identical on the two device groups. There is no eCAN module on the 2802x device family.

The 2803x devices also feature a new local interconnect network (LIN) module that did not exist on the 28x/2801x/2804x devices. There is no LIN-A module on the 2802x devices.

Table 5. Available Communication Peripherals

Device	I2C	SCI Modules	SPI Modules	eCAN Modules	LIN
28035PAG, 28034PAG, 28033PAG, 28032PAG	I2C-A	SCI-A	SPI-A	eCAN-A	LIN-A
28035PN, 28034PN, 28033PN, 28032PN	I2C-A	SCI-A	SPI-A, SPI-B	eCAN-A	LIN-A
28027, 28026, 28023, 28022, 28021, 28020	SCI-A	SCI-A	SPI-A	-	-
2809, 2808	I2C-A	SCI-A, SCI-B	SPI-A, SPI-B, SPI-C, SPI-D	eCAN-A, eCAN-B	-
2806	I2C-A	SCI-A, SCI-B	SPI-A, SPI-B, SPI-C, SPI-D	eCAN-A	-
2802, 2801	I2C-A	SCI-A	SPI-A, SPI-B	eCAN-A	-
28044	I2C-A	SCI-A	SPI-A	-	-
28016	I2C-A	SCI-A	SPI-A	eCAN-A	-
28015	I2C-A	SCI-A	SPI-A	-	-

9.6 Enhanced Control Peripherals

The eCAP module remains functionally the same between the device families. Because there is only 1 eCAP module on the 2802x/2803x devices, code written for eCAP2-6 on the 280x/2801x/2804x devices cannot be ported. The 2802x devices do not have an eQEP module, so code written for the eQEP module on the 280x/2801x/2804x cannot be ported to these devices. Otherwise, the eQEP-1 module remains functionally the same for the 280x/2801x/2804x and the 2803x devices. Unlike the 280x/2801x/2804x devices, there is no eQEP-2 module on any of the 2803x devices. Therefore, code written for the eQEP-2 module cannot be directly ported. For the eCAP and eQEP modules, the register sets are identical on the two device groups: the memory addresses of the registers for each instance of peripheral are also identical. For example, eCAP1 registers on the 280x/2801x/2804x are at the same location as eCAP1 registers on 2802x/2803x. In addition, the interrupt vector locations in the PIE vector table are identical.

There is one notable difference to the eCAP module on the two device families:

- **ePWM and eCAP Synchronization**

    The synchronization scheme varies slightly between 280x, 2801x, 28044 and 2802x/2803x. For more information, see the device-specific enhanced pulse width modulator (ePWM) Reference Guide and the device-specific Enhanced Capture (eCAP) Module Reference Guide.

Table 6. Available Control Peripherals

Device	ePWM	HRPWM	eCAP	eQEP
28335, 28235	ePWM1-ePWM6	ePWM1A-ePWM6A	eCAP1-eCAP6	eQEP1-eQEP2
28334, 28234	ePWM1-ePWM6	ePWM1A-ePWM6A	eCAP1-eCAP4	
28332, 28232	ePWM1-ePWM6	ePWM1A-ePWM4A	eCAP1-eCAP4	eQEP1-eQEP2
2809	ePWM1-ePWM6	ePWM1A-ePWM6A	eCAP1-eCAP4	eQEP1-eQEP2
2808	ePWM1-ePWM6	ePWM1A-ePWM4A	eCAP1-eCAP4	eQEP1-eQEP2
2806	ePWM1-ePWM6	ePWM1A-ePWM4A	eCAP1-eCAP4	eQEP1-eQEP2
2802, 2801	ePWM1-ePWM3	ePWM1A-ePWM3A	eCAP1-eCAP2	eQEP1
28044	ePWM1-ePWM16	ePWM1A-ePWM16A	-	-
28016, 28015	ePWM1-ePWM4	ePWM1A-ePWM4A	eCAP1-eCAP2	-

9.7 *Enhanced Pulse Width Modulator (ePWM)*

Code written for the ePWM modules on the 280x/2801x/2804x devices can be almost directly ported to the 2802x devices. Code written to generate an event based off of the $\overline{TZ4}$, $\overline{TZ5}$, and $\overline{TZ6}$ trip zone inputs will need to change because these signals no longer come from GPIO-muxed TZ pins. Instead, $\overline{TZ4}$ is now connected to an $\overline{EQEP1ERR}$ signal (on 2803x devices only), $\overline{TZ5}$ is connected to a $\overline{CLOCKFAIL}$ signal from the CPU, and $\overline{TZ6}$ is connected to an EMUSTOP signal from the CPU. There are also a large number of new features on the 2802x/2803x ePWM module which include:

- **Increased Dead-Band Resolution**

  The dead-band clocking has been enhanced to allow half-cycle clocking to double resolution.

- **Enhanced Interrupt and SOC Generation**

  Interrupts and ADC start-of-conversion can now be generated on both the TBCTR == zero and TBCTR== period events. This feature enables dual edge pulse width modulator (PWM) control. Additionally, the ADC start-of-conversion can be generated from an event defined in the digital compare sub-module.

- **High Resolution Period Capability**

  Provides the ability to enable high-resolution period. This is discussed in more detail in the device-specific HRPWM Reference Guide.

- **Digital Compare Sub-Module**

  The digital compare sub-module enhances the event triggering and trip zone sub-modules by providing filtering, blanking and improved trip functionality to digital compare signals. Such features are essential for peak current mode control and for support of analog comparators.

New bits and registers have been added to the ePWM modules to support these features.

Code written for the HRPWM extension to the ePWM can be directly ported unless the Scale Factor Optimization library (SFO_TI_Build.lib and SFO_TI_Build_V5(B).lib) functions were being utilized for the 280x/2801x/2804x devices. The 2802x/2803x devices use a different SFO library, SFO_TI_Build_V6.lib, which calls the SFO() function instead of the MepEn() or MepDis() functions from the previously libraries. This function can be called in background code without affecting the high-resolution output of any of the ePWM modules. For more information, see the *TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (SPRUGE9) for more information.

If the SFO libraries were not being used with code written for the HRPWM module, the code can be directly ported to the 2802x/2803x devices. Like the ePWM module, a number of new features have been added to the 2802x/2803x HRPWM module as well. They are:

- **High-Resolution B-Channel Output**

  Enables high-resolution output on he B signal path of PWM via PWM channel path swapping and inversion.

- **High-Resolution Period Capability**

  Enables high-resolution period control in addition to high-resolution duty and phase control.

- **Auto-Conversion Feature**

  When enabled, you need to fill CMPAHR, TBPRDHR, or TBPHSHR with fractional duty, period, or phase. The hardware automatically converts this to the appropriate number of delay steps for micro-edge movement on the HRPWM output. On the 280x, 2801x, 2804x devices, this conversion was done manually by user code in the software.

New bits and registers have been added to the ePWM+HRPWM modules to support these features.

Table 7. Available Control Peripherals

Device	ePWM	HRPWM	eCAP	eQEP
28035PAG, 28034PAG, 28033PAG, 28032PAG	ePWM1-ePWM6	ePWM1A-ePWM6A	eCAP1	eQEP1
28035PN, 28034PN 28033PN, 28032PN	ePWM1-ePWM7	ePWM1A-ePWM7A	eCAP1	eQEP1
28027, 28026, 28023, 28022	ePWM1-ePWM4	ePWM1A-ePWM4A	eCAP1	-
28021, 28020	ePWM1-ePWM4	-	eCAP1	-
2809	ePWM1-ePWM6	ePWM1A-ePWM6A	eCAP1-eCAP4	eQEP1-eQEP2
2808	ePWM1-ePWM6	ePWM1A-ePWM4A	eCAP1-eCAP4	eQEP1-eQEP2
2806	ePWM1-ePWM6	ePWM1A-ePWM4A	eCAP1-eCAP4	eQEP1-eQEP2
2802, 2801	ePWM1-ePWM3	ePWM1A-ePWM3A	eCAP1-eCAP2	eQEP1
28044	ePWM1-ePWM6	ePWM1A-ePWM16A	-	-
28016,28015	ePWM1-ePWM4	ePWM1A-ePWM4A	eCAP1-eCAP2	-

10 Interrupts

Changes to interrupts include updates to the peripheral interrupt expansion (PIE) module and handling of external interrupts and NMI.

10.1 NMI-Watchdog

On 2802x/2803x, NMI is used to monitor clock failure in the system and is not sourced from outside the system. On 280x/2801x/2804x, a clock failure will result in a system reset. On 2802x/2803x, when a clock failure is detected through limp-mode, a $\overline{\text{CLOCKFAIL}}$ signal is generated and latched as an NMI interrupt, which is fed to NMI-watchdog. NMI-watchdog forces a system reset if the CPU fails to respond to the NMI within a given time.

Table 8. New NMI Internal Support Registers

Register	Change	Description
NMICFG	New	NMI Configuration Register
NMIFLG	New	NMI Flag Register
NMIFLGCLR	New	NMI Flag Clear Register
NMIFLGFRC	New	NMI Flag Force Register
NMIWDCNT	New	NMI Watchdog Counter Register
NMIWDPRD	New	NMI Watchdog Period Register

10.2 Peripheral Interrupt Expansion (PIE) Module

The functionality of the PIE module and of the PIE configuration registers remains the same. The PIE vector table has been updated to accommodate the interrupts issued by the new peripheral blocks such as LIN, CLA, and modified peripheral blocks such as ADC.

10.3 External Interrupts

On 280x/2801x/2804x, there are three external interrupts:XINT1, XINT2 and XNMI_XINT13. On 2802x/2803x, there are three external interrupts: XINT1, XINT2 and XINT3. On 2802x/2803x, XNMI_XINT13 is replaced with XINT3 and NMI is not affected by XINT3.

Table 9. External Interrupt Registers

Register	Change	Description
XNMICR	Removed	External NMI Interrupt Control Register
XNMICTR	Removed	External NMI Interrupt Counter
XINT3CR	New	XINT3 configuration register
XINT3CTR	New	XINT3 counter register
GPIOXNMISEL	Removed	GPIO XNMI Interrupt Select Register
GPIOXINT3SEL	New	XINT3 GPIO Input Select Register

For more information on Interrupts and their supporting registers, see the device-specific TMS System Control and Interrupts Reference Guide.

11 Errata Fixes

280x/2801x/2804x errata that have been fixed on 2802x/2803x include:
- When the CAN option is invoked in the boot ROM, the code may hang occasionally.
- SCI bootloader does not clear the ABD bit after auto-baud lock
- Incorrect operation of SCI in address bit mode
- Flash and OTP prefetch butter overflow
- eCAN-A Boot Mode in Boot Rom
- Change to Watchdog Module: Bad key writes to WDKEY no longer cause RESET/interrupt to be generated.
- Limitation on Watchdog Module: Corrupted watchdog key writes
- Configuration change in Boot ROM

For more information on the various advisories, see the TI website for the most recent device specific silicon errata.
- *TMS320F280x, TMS320C280x, and TMS320F2801x DSP Silicon Errata* (SPRZ171)
- *TMS320F28044 DSP Silicon Errata* (SPRZ255)
- *TMS320F28020, TMS320F28021, TMS320F28022, TMS320F28023, TMS320F28026, TMS320F28027 Piccolo MCU Silicon Errata* (SPRZ292)
- *TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo MCU Silicon Errata* (SPRZ295)

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- *TMS320F280x, TMS320C280x, and TMS320F2801x DSC Silicon Errata* (SPRZ171)
- *TMS320F28044 DSP Silicon Errata* (SPRZ255)
- *TMS320F28020, TMS320F28021, TMS320F28022, TMS320F28023, TMS320F28026, TMS320F28027 Piccolo MCU Silicon Errata* (SPRZ292)
- *TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo MCU Silicon Errata* (SPRZ295)
- *TMS320C28x Digital Signal Controller Plus Floating Point Unit* online training available from the TI website at http://www.ti.com/
- *TMS320C28x DSP CPU and Instruction Set Reference Guide* (SPRU430)
- *TMS320x2803x Piccolo Control Law Accelerator Reference Guide* (SPRUGE6)
- *2802x C/C++ Header Files and Peripheral Examples* (SPRC832)

- *2803x C/C++ Header Files and Peripheral Examples* (SPRC892)
- *TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801, and TMS320F2801x DSPs Data Manual* (SPRS230)
- *TMS320F28044 Digital Signal Processor Data Manual* (SPRS357)
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- *TMS320x280x, 2801x, 2804x Boot ROM Reference Guide* (SPRU722)
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- *TMS320x28xx, 28xxx Enhanced Capture (eCAP) Module Reference Guide* (SPRU807)

Revision History

Changes from B Revision (December 2009) to C Revision   **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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