Application Report
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Migrating from TMS320DM6446 to TMS320DM6467

DSPS Applications

ABSTRACT

This document describes considerations for migration from Texas Instruments TMS320DM6446 Digital Media System-on-Chip (DMSoC) to the TMS320DM6467 DMSoC. Both devices feature a dual-core architecture utilizing a high-performance TMS20C64x+™ Digital Signal Processor (DSP) core and an ARM926EJ-S central processing unit (CPU) core. While the TMS320DM6446 features video front-end and back-end processing capabilities, the TMS320DM6467 includes a high definition video/imaging co-processor and video data conversion engine. This application report describes the feature differences to consider when performing this migration.

This document assumes familiarity with the TMS320DM6446 device and its documentation. Further documentation on the TMS320DM6446 and the TMS320DM6467 can be found on the TI website in the device specific product folder.

TMS320DM6446 - http://focus.ti.com/docs/prod/folders/print/tms320dm6446.html

TMS320DM6467 - http://focus.ti.com/docs/prod/folders/print/tms320dm6467.html

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1 Basic Feature Comparison

The basic hardware features of the TMS320DM6446 and the TMS320DM6467 are highlighted in Table 1. This document will discuss the difference between the device features, along with the new features of the TMS320DM6467. Reference to appropriate documentation is provided for further information.

Table 1. Basic DM6446/DM6467 Feature Comparison

Hardware Features				DM6446	DM6467
CPU	DSP			C64x	C64x+
	ARM			ARM926EJ-S	ARM926EJ-S
Speeds	DSP			513-/894 MHz	594-/729 MHz
	ARM			256.5/297 MHz	297/364.5 MHz
Endianness				Little	Little
Memory	DSP	Cache: L1P		32 K-Byte	32 K-Byte
		Cache: L1D		80 K-Byte	32 K-Byte
		Cache: L2		64 K-Byte	128 K-Byte
	ARM	Data/Program RAM		16 K-Byte	32 K-Byte
		Data/Program ROM		8 K-Byte	8 K-Byte
		Instruction Cache		16 K-Byte	16 K-Byte
		Data Cache		8 K-Byte	8 K-Byte
Peripherals		VCXO Interpolated Control Port		VPFE, VPBE	NA
		Video/Imaging Coprocessor		VICO	2 HDVICP
		Video Port Interface (VPIF)		NA	1
		Video Data Conversion Engine (VDCE)		NA	1
		Transport Stream Interface (TSIF)		NA	2
		DDR2 EMIF		1	1
		Asynchronous EMIF (EMIFA)		1	1
		EDMA	EDMA Controller	1	1
			Transfer Controller	2	4
		Timers		2, 64 bit	2, 64 bit
		Watchdog Timer		1	1
		UART		3	3
		SPI		1	1
		PLL		2	2
		I2C		1	1
		Serial Ports		1 ASP	2 McASP
		EMAC		10/100 EMAC	10/100/1000 EMAC
		USB 2.0		1	1
		VLYNQ		1	1
		HPI		1 16 bit	1 16-/32 bit
		GPIO		Up to 71pins	Up to 33 pins
		PWM		3 outputs	2 outputs
		ATA/ATAPI I/F		NA	1 32 bit, 33 MHz
		PCI		1 32 bit, 66 MHz	1 32 bit, 33 MHz
		Clock Recovery Generator		-	1
Voltage		Core (V)		1.2 V	1.2 V
		I/O (V)		1.8 V, 3.3 V	1.8 V, 3.3 V
Packages				361-pin BGA	529-pin BGA

2 CPU Core Considerations

The DM6446 and DM6467 devices contain the C64x+™ DSP core and the ARM926EJ-S CPU core. The features of the CPU cores of the devices are discussed in the following sections.

2.1 DSP CPU Core Considerations

The TMS320DM6446 and TMS320DM6467 contain the same TMS320C64x+ DSP core; therefore, code written on the DM6446 is compatible with that of the DM6467. The devices differ in application-specific hardware logic, on-chip memory, and peripherals. When migrating to the DM6467 functionality of peripheral modules as well as differences in the memory map must be considered. These differences are discussed in greater detail in the remainder of this document.

2.2 ARM CPU Core Considerations

The TMS320DM6446 and TMS320DM6467 contain the ARM926EJ-S CPU core. The DM6446 is fully software compatible with the DM6467. The differences in the peripheral modules as well as memory map must be accounted for when migrating applications from the DM6446 to the DM6467.

2.3 CPU Clock Speeds

The DM6446 and the DM6467 can be operated at a range of clock speeds to accommodate a variety of different performance requirements. The DM6467 is available with a DSP CPU speeds of 594/729 MHz and an ARM speeds of 297/364.5 MHz. Each device has an input clock of 27 MHz. Table 2 shows a summary of the different speed versions of the DM6446 and DM6467.

Table 2. Available Performance Versions of the DM6446 and DM6467

	DM6446	DM6467
ARM CPU	297 MHz (3.37 ns cycle time)	297 MHz (3.37 ns (cycle time)
	256.5 MHz (3.9 ns cycle time)	364.5 MHz (2.74 ns cycle time)
DSP CPU	594 MHz (1.68 ns cycle time)	594 MHz (1.68 ns cycle time)
	513 MHz (1.95 ns cycle time)	729 MHz (1.37 ns cycle time)

For additional information regarding performance, timing requirements, and characteristics for the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403).

2.4 Endianness Considerations

The DSP and ARM of the DM6446 and the DM6467 both operate in little endian format; therefore, there are no endianness considerations when migrating an application from the DM6446 to the DM6467.

3 Internal Memory Comparisons

The DMSoC has multiple on-chip memories associated with its two processors and various subsystems. Both devices feature several different types of cache memory, allowing significant flexibility in using this memory to enhance algorithm performance. These devices also provide an on-chip read-only memory (ROM) that contains the bootloader program. Since there are some differences between the memory architectures on the two devices, some software modifications are required to migrate applications from the DM6446 to the DM6467.

The DM6446 and DM6467 contain ARM and DSP CPU cores, memory usage is partitioned between the two CPUs; therefore, certain areas of internal memory, although accessible to both CPUs, are typically used more by one CPU than the other.

3.1 DSP Internal Memory Comparison

The DM6467 C64x+ core uses a two level cache-based architecture. The Level 1 program memory/cache consists of 32 K-bytes of memory space that can be configured as mapped-memory or direct-mapped cache. The Level 1 data memory/cache consists of 32 K-bytes that can be configured as mapped-memory or 2-way set associative cache. The Level 2 memory/cache (L2) consists of a 128 K-bytes of RAM memory space that is shared between program and data space. L2 memory can be configured as mapped-memory, cache, or a combination of both. Table 3 shows a comparison of the DM6446 and DM6467 DSP internal memory.

Table 3. DSP Internal Memory Comparison

Memory Type	DM6446	DM6467
L1P Program Memory	32K-bytes RAM/Cache (direct mapped), flexible allocation	32K-bytes RAM/Cache (mapped memory or direct mapped cache)
L1D Data Memory	80K-bytes RAM/Cache (2-way set associative), flexible allocation	32K-bytes RAM/Cache (mapped memory or 2-way set associative cache)
L2 RAM Memory	64K-bytes Unified Mapped RAM/Cache (4-way set associative), flexible allocation	128K-bytes Unified Mapped RAM/Cache

3.2 ARM Internal Memory Comparison

The ARM on both devices has access to 8 K-bytes ARM Internal ROM that can be used for instructions or data. The TMS320DM6446 also includes 16 K-bytes ARM internal RAM on tightly-coupled memories (TCM) interface logically separated into two 8K-byte pages, while the TMS320DM6467 includes 32 K-bytes ARM internal RAM logically separated into 16K-byte pages. Each device also contains 16K-bytes instruction Cache and 8K-bytes of data Cache used by the CPU to enhance instruction and data handling. Table 4 shows a comparison of the DM6446 and DM6467 ARM internal memory.

Table 4. ARM Internal Memory Comparison

Memory Type	DM6446	DM6467
Data/Program RAM	16 K-bytes	32 K-bytes
Data/Program ROM	8 K-bytes	8 K-bytes
Program Cache	16 K-bytes	16 K-bytes
Data Cache	8 K-bytes	8 K-bytes

For additional detailed information regarding use of the DM6467 internal memory, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403) and the *TMS32064x+ DSP Cache User's Guide* (SPRU862).

4 Peripherals

The TMS320DM6446 and the TMS320DM6467 feature a wide variety of peripheral modules that are useful in many different system environments. This section presents a comparison of the peripheral offerings on these two devices.

4.1 Video Processing Subsystem (VPSS)

The DM6446 and DM6467 feature video processing peripherals that can accept video input and generate video output. The video processing capabilities on the DM6446 are implemented in the VPSS, which is partitioned into two subsections, an input video processing front end (VPFE) and an output video processing back end (VPBE). The DM6467 uses the video data conversion engine (VDCE) and the video port interface (VPIF). The peripheral modules on the devices are different; therefore, modifications of hardware and software are necessary to migrate an application from the DM6446 to the DM6467. This section presents the features available in the DM6467 VDCE/VPIF and the DM6446 VPSS.

4.1.1 DM6446 Video Processing Front End (VPFE)

The DM6446 VPFE is an input interface for external imaging peripherals, such as image sensors, video decoders, etc. This peripheral module is comprised of a CCD controller (CCDC), a preview engine (previewer), Histogram module, auto-exposure/white balance/focus module (H3A), and resizer. The CCDC is capable of interfacing to common video decoders, CMOS sensors, and CCDs. The previewer is a real-time image processing engine that takes raw imager data from a CMOS sensor or CCD and converts from an RGB Bayer Pattern to YUV4:2:2. The Histogram and H3A modules provide statistical information on the raw color data for use by the DM6446. The resizer accepts image data for separate horizontal and vertical resizing from 1/4x to 4x in increments of 256/N, where N is between 64 and 1024.

Although the DM6467 does not contain the VPFE, it is able to provide some of the features in the VPIF and VDCE. For more information, see Section 4.1.3, DM6467 Video Port Interface, and Section 4.1.4, Video Data Conversion Engine.

4.1.2 DM6446 Video Processing Back End (VPBE)

The DM6446 VPBE is an output interface for display devices, such as analog SDTV displays, digital LCD panels, and HDTV video encoders. The VPBE is comprised of an on-screen display (OSD) engine and a video encoder (VENC). The OSD engine is capable of handling two separate video windows and two separate OSD windows. The VENC provides four analog digital-to-analog converter (DACs) that run at 54 MHz, providing a means for composite NTSC/PAL video, S-Video, and/or component video output. The VENC also provides up to 24 bits of digital output to interface to RGB888 devices. A digital output of 8-bit BT.656 and up to 16-bit video output with separate horizontal an vertical syncs is supported.

Although the DM6467 does not contain the VPBE, it is able to provide some of the features in the VPIF and VDCE. For related features, seeSection 4.1.3 , DM6467 Video Port Interface, and Section 4.1.4, Video Data Conversion Engine.

4.1.3 DM6467 Video Port Interface (VPIF)

The DM6467 features a VPIF that allows capture and display of digital video streams. The DM6467 VPIF has two input channels that receive video byte stream data and two output channels that video byte stream data is asserted.

Channels 0 and 1 are prepared only for input. The following configurations are allowed for the input channels; two 8-bit standard definition video with embedded timing codes (BT.656); or one single 16-bit high definition video with embedded timing codes (BT.1120); or a single Raw video (8-/10-/12-bit). Channels 2 and 3 are prepared only for output. The following configurations are allowed for the output channels; two 8-bit standard video display channels with embedded timing codes or one single 16-bit HD video display with embedded timing codes. There are no analog DACs on the DM6467 VPIF as in the DM6446 VPBE.

The VPIF capture channel input data format is selectable based on the settings of the specific Channel Control Register, Channels0-3. Both NTSC and PAL formats are supported for this device. VBI is not supported for ITU-BT.1120 (HDTV). VBI is necessary only for ITU-BT.656 (SDTV); in this case, VBI format has to be based on ITU-BT.1364. Table 6 describes the usage combinations that are supported in the VPIF.

Table 5. VPIF Supported Video Formats

	DM6467	
TV System Format	HDTV(rec.1120)	SDTV (rec. 656)
NTSC	1125 line/60 field (vertical)	525 line/60 field (vertical)
	2200 pixel (horizontal)	858 pixel (horizontal)
PAL	1250 line/50 field (vertical)	625 line/50 field (vertical)
	2304 pixel (horizontal)	864 pixel (horizontal)
Square pixel common image format	1080-30p	-

Table 6. Input and Output Usage Combinations on VPIF

Input Format	DM6467		
	HDTV Output	SDTV Output	No Output
HDTV Input (1 channel only)	X	X	X
Raw Capture Mode	X	X	X
SDTV input	X (both 1-channel and 2-channel input)	X (both 1-channel and 2-channel input/output)	X(both 1-channel and 2-channel input)
No input	X	X(both 1-channel and 2-channel output)	

In the VPIF, both the input data and output data are stored in SDRAM. All video data is divided into image data and VBI data. The image data is divided into luminance and chrominance data in each field independently. Each start address in SDRAM can be configured by the ARM processor through the register interface.

For more detailed information regarding the use of the DM6467 VPIF, see the *TMS320DM646x DMSoC Video Port Interface (VPIF) User's Guide* (SPRUER9).

4.1.4 Video Data Conversion Engine

The DM6467 features a video data conversion engine (VDCE) used for video data processing. The VDCE has several capabilities of not only pure video data processing but also functions that are required from a video codec module.

The VDCE supports a down-scaler function on horizontal (HRSZ) and vertical (VRSZ) with ratio defined by 256/N (N is natural number that ranges from 256 to 2048) with 4 taps interpolation. Magnification ratio of horizontal and vertical down-scaler can be configured separately.

The horizontal down scaler module has an anti-alias filter (7 taps) for luminance data, pixel interpolation (4 taps) for common use of luminance and chrominance data, and size clipping to configure size on module register. The method of vertical down-scaler varies from picture format, interlace, or progressive. In interlace format, the vertical down-scaler function performs for each field independently. All source pixels of interpolation are derived by the same field.

The VDCE also features a chrominance conversion module used for format conversion of chrominance signal between 4:2:2 and 4:2:0 formats. The 4:2:0 format is mainly used for video codec and the 4:2:2 format is mainly used for input or output video signals such as BT.656 or BT.1120.

The VDCE does not have multiple video window/OSD window support as in the DM6446 VPBE. The VDCE features a 2-bit hardware menu overlay function that can blend video image and artificial bitmap data (2bits/pixel), like a light OSD function. The 2-bit hardware menu overlay function reads two kinds of data (video and bitmap) from SDRAM, and overlays them to one display output data with blending.

The VDCE also features edge padding for enhancement of reference image data to be used in motion compensation function with unrestricted motion vector that is defined in specification H.264, VC-1, and MPEG-4. This module copies all edge pixels to the external side of the reference data with configured width for both horizontal and vertical directions (both upper and lower, both left and right of the image data). The method of edge padding varies in two ways, one is progressive format and the other is interlaced format.

For detailed information regarding the use of the VDCE, see the *TMS320DM646x DMSoC Video Data Conversion Engine (VDCE) User's Guide* (SPRUEQ9).

4.2 Video/Imaging Coprocessor (VICP)

The DM6446 contains a video/imaging coprocessor (VICP) engine, while the DM6467 contains two programmable high definition video/imaging coprocessor engines (HDVICP). Both coprocessors can be used to perform operations that offload many video and imaging processing tasks from the DSP core, making more DSP MIPS available for common video and imaging algorithms.

The HDVICP supports a range of encode, decode, and transcode operations, including H.264, MPEG2, VC1, and MPEG4 SP/ASP. The VICP and HDVICP, however, are not documented in detail other than for providers of algorithms specifically using this peripheral. For more information on the HDVICP enhanced codecs, such as H.264 and MPEG4, please contact your nearest TI sales representative.

4.3 Transport Stream Interface

The DM6467 contains two independent transport stream interface (TSIF0 and TSIF1) modules with corresponding clock reference generator modules for system time-clock recovery. This added module is used to parser stream including TS (Time Stamp) header, adaptation field, and payload and packet ID (PID) table. It is also used to input an output stream with a parallel and serial interface. Table 7 describes the input/output (I/O) signals provided by the TSIF.

Table 7. TSIF Signal Descriptions

Serial					Parallel			
Synchronous			Asynchronous		Synchronous		Asynchronous	
Port Name	I/O	Function	I/O	Function	I/O	Function	I/O	Function
TSn_CLKO	O	Transmit clock	O	Transmit clock	O	Transmit clock	O	Transmit clock
TSn_ENAO	O	Data enable	O	Data enable	O	Data enable	O	Data enable
TSn_WAITIN	I	Not used	I	Wait in	I	Not used	I	Wait in
TSn_PSTO	O	Packet start out	O	Packet start out	O	Packet start out	O	Packet start out
TSn_DOUT7	O	Data Out	O	Data Out	O	Data[7] out	O	Data[7] out
TSn_DOUT[6:0]	O	Not used	O	Not used	O	Data[6:0] out	O	Data[6:0] out
TSn_CLKIN	I	Receive clock	I	Receive clock	I	Receive clock	I	Receive clock
TSn_EN_WAITO	I	Data enable	O	Wait out	I	Data enable	O	Wait out
TSn_WAITO	O	Not used	O	Not used	O	Not used	O	Wait out
TSn_PSTIN	I	Packet start in	I	Packet start in	I	Packet start in	I	Packet start in
TSn_DIN7	I	Data in	I	Data in	I	Data[7] in	I	Data[7] in
TSn_DIN[6:0]	I	Not used	I	Not used	I	Data[6:0] in	I	Data[6:0] in

The TSIF0 module is able to use the parallel interface and serial interface, while the TSIF1 module is able to use only the serial interface.

Four types of PID filter methods are supported and are controlled by the PID_FILTER_CTL and PID_FILTER_EN bits in the TSIF control register 1(CTRL1): bypass mode, full-manual mode, semi-automatic (mode-A and mode-B), and full-automatic mode.

For more detailed information regarding the use of the TSIF, see the *TMS320DM646x DMSoC Transport Stream Interface (TSIF) Module User's Guide* (SPRUEQ2).

4.4 External Memory Interface (EMIF)

The DM6446 and DM6467 feature flexible external interfaces that support accessing various types of memories. Both devices support two independent memory interfaces, each architected for specific memory types. These two memory interfaces are the DDR2 memory interface, specifically designed to gluelessly interface to industry-standard DDR2 memories, and the asynchronous memory interface, are designed to efficiently interface to a variety of asynchronous memory types. They are similar on both devices making migration of applications from the DM6446 to the DM6467 straightforward. There are, however, some differences in using these peripherals on the two devices. The following paragraphs describe migration of applications using these two interfaces.

4.4.1 DDR2 EMIF

The DDR2 interface on the DM6446 and DM6467 uses a 32-bit data bus and is optimized for use with high-speed, high-density, DDR2 memory for storage of programs and large blocks of data. Additionally, both devices also have the capability to use the interface data bus in 16-bit mode, instead of 32-bit mode, if desired to save pin-out connections.

There are a few significant differences between the DDR2 EMIF on these two devices. First, the DDR2 EMIF peripheral module is clocked by a different clock on the DM6467 than on the DM6446. On the DM6446, the DDR2 EMIF is clocked by the PLL2 SYSCLK2 clock, while on the DM6467 the DDR2 EMIF is clocked by the PLL2 SYSCLK1 clock. This does not affect the performance, it only affects which registers must be written to during initialization. Note that these two clocks do not default to the same frequencies following reset; therefore, for identical performance, the control registers for these clocks must be modified on the DM6467 to achieve the same performance as with the DM6446.

As stated before the devices have a maximum data bus that is 32-bits wide. The address bus on the DM6446 is 13-bits wide with an additional 3 bank address pins, while the address bus on the DM6467 is 15-bits wide with an additional 3 bank address pins. Both devices feature two differential output clocks driven by internal clock sources, command signal (row and column address strobe, write enable strobe, data strobe, and data mask), one chip select and one clock enable signal. Table 8 describes the memory controller signals available on the DM6446 and DM6467.

Table 8. DDR2 Memory Controller Signal Descriptions

DM6446 Pin	DM6467 Pin	Type [1]	Description
DDR_CLK0	DDR_CLK	O/Z	Clock: Clock Output
$\overline{\text{DDR\_CLK0}}$	$\overline{\text{DDR\_CLK}}$	O/Z	Clock: Differential Clock Output
DDR_CKE	DDR_CKE	O/Z	Clock enable: Active High
$\overline{\text{DDR\_CS}}$	$\overline{\text{DDR\_CS}}$	O/Z	Chip select: Active Low
$\overline{\text{DDR\_WE}}$	$\overline{\text{DDR\_WE}}$	O/Z	Write Enable: Active Low, command output
$\overline{\text{DDR\_RAS}}$	$\overline{\text{DDR\_RAS}}$	O/Z	Row access strobe: Active low, command output
$\overline{\text{DDR\_CAS}}$	$\overline{\text{DDR\_CAS}}$	O/Z	Column access strobe: Active low, command output
DDR_DQM[3:0]	DDR_DQM[3:0]	O/Z	Data mask: Output mask signal for write data
DDR_DQS[3:0]	DDR_DQS[3:0]	O/Z	Data Strobe: Data strobe, bi-directional signal. Output with write data, input with read data
$\overline{\text{DDR\_DQS[3:0]}}$	$\overline{\text{DDR\_DQS[3:0]}}$	I/O/Z	Data Strobe: Differential data strobe, bi-directional signals. Output with write data, input with read data
	DDR_ODT0	O/Z	ODT control: DDR2 On-die termination control. Active High
DDR_BS[2:0]	DDR_BA[2:0]	O/Z	Bank Select: Output, defining which bank a given command is applies
DDR_A[12:0]	DDRA[14:0]	O/Z	Address: Address Bus
DDR_D[31:0]	DDR_D[31:0]	I/O/Z	Data: Bi-directional data bus. Input for read data, output for write data
	DDR_DQGATE[3:0]	I/O/Z	Data strobe gate enable: Data strobe gate signals for data bus
	DDR_VREF	I	Reference Voltage: Reference Voltage
DDR_ZN, DDR_ZP	DDR_ZN, DDR_ZP	O	Output Impedance control: Required to set the DDR2 output impedance

(1) I = Input, O = Output, Z = Hi-Impedance

The DM6467 DDR2 memory controller supports the on die termination (ODT) function, whereas the DM6446 DDR2 memory controller does not include any on-die terminating resistors.

For detailed information regarding the use of the DDR2 Memory Controller, see the *TMS320DM646x DMSoC DDR2 Memory Controller User's Guide* (SPRUEQ4).

4.4.2 Asynchronous External Memory Interface (EMIF)

The DM6446 and DM6467 use the same peripheral module for the asynchronous EMIF (EMIFA), therefore, migration of an application utilizing this interface between these two devices requires only minor modification of hardware or software.

The asynchronous memory interface on the DM6446 and DM6467 is designed for slower special-purpose memory such as static random access memory (SRAM), NOR, NAND Flash memory, ROM, and other asynchronous memory types.

Since the DM6446 and the DM6467 utilize the same asynchronous EMIF peripheral module, some of the main differences in usage between the peripheral modules on these two devices are signal locations within the device pinouts and the pin multiplexing configuration settings.

The EMIFA of the DM6446 and DM6467 provide an 8-bit or 16-bit data bus, an address bus width up to 24-bits, and four dedicated chip selects, along with memory control signals. On the DM6446, the signals are multiplexed with other peripherals such as VLYNQ™ communications interface products, AT attachments (ATA), and general-purpose input/output (GPIO). On the DM6467, pins are multiplexed with peripheral component interconnect (PCI), host-post interface (HPI), GPIO, and ATA. See the device-specific data manual for instructions on how to select EMIF pins for proper operation. Table 9 shows a comparison of the DM6446 and DM6467 EMIF pins.

Table 9. DM6446 and DM6467 EMIF Pin Comparison

DM6446 Pin(s)	DM6467 Pin(s)	I/O (1)	Description
EM_A[21:0]	EM_A[23:0]	O	EMIF address bus
EM_BA[1:0]	EM_BA[1:0]	O	EMIF bank address
$\overline{\text{EM\_CS}}$[5:2]	$\overline{\text{EM\_CS}}$[5:2]	O	Active-low chip enable pin for asynchronous devices
EM_D[15:0]	EM_D[15:0]	I/O	EMIF data bus
$\overline{\text{EM\_RW}}$	$\overline{\text{EM\_RW}}$	O	Read/write select pin
$\overline{\text{EM\_OE}}$	$\overline{\text{EM\_OE}}$	O	Active-low pin enable for asynchronous devices
$\overline{\text{EM\_WE}}$	$\overline{\text{EM\_WE}}$	O	Active-low write enable
EM_WAIT	EM_WAIT[5:2]	I	Wait input with programmable polarity

(1) I = Input, O = Output

Both devices feature an extended wait mode in which the external asynchronous device may assert control over the length of the strobe period. The extended wait mode can be entered by setting the EW bit in the Asynchronous Configuration Register (AnCR-DM6446, ACFGn-DM6467). There are four EM_Wait pins on the DM6467 and only one on the DM6446.

Another difference to note is the device EMIFs internal clock source. The DM6446 EMIFs internal clock is sourced from the CLKDIV6 clock domain of PLL controller 1 and cannot be sourced directly from an external input clock, while the DM6467 is sourced from the SYSCLK3 domain of PLL controller 0. Therefore, changes to the frequency of the input clock to PLL controller 0 and to the PLL controller multiplier values alters the operating frequency of the DM6467 EMIF.

For detailed information regarding the use of the Asynchronous EMIF, see the *TMS320DM646x DMSoC Asynchronous External Memory Interface (EMIF) User's Guide* (SPRUEQ7).

4.5 Enhanced Direct Memory Access (EDMA) Controllers

The DM6446 and DM6467 feature EDMA controllers that can be used to transfer data to and from numerous locations, both on and off chip. Both devices support 64 independent EDMA channels that service peripheral devices and external memory.

The EDMA controllers used on these two devices are based on the EDMA 3.0 peripheral module, however, there are some differences between the peripheral modules on the devices. Specifically, the DM6467 EDMA implements several advanced features beyond those available on the DM6446.

The DM6446 and DM6467 EDMA controller have a RAM-based architecture. The parameter RAM (PaRAM) table is segmented into multiple PaRAM sets, each including eight 4-byte PaRAM set entries that includes typical DMA transfer parameters such as source address, destination address, transfer counts, indexes, options, etc. There are 128 PaRAM sets in the DM6446 and 512 PaRAM sets in the DM6467.

Another difference is that the DM6446 provides two EDMA queues and two transfer controllers, while the DM6467 has four of each. The DM6467 also offers six transfer completions interrupts and five error interrupts, while the DM6446 only provides three completion interrupts and four error interrupts. Table 10 shows a comparison of the DM6446 and DM6467 EDMA features.

Table 10. DM6446 to DM6467 EDMA Comparison

Feature	TC	DM6446	DM6467
Number of PaRAM sets		128	512
Number of Queues		2	4
Number of Transfer Controllers		2	4
Default Burst Size	TC0	Fixed – 16 bytes	Fixed – 32 bytes
	TC1	Fixed – 32 bytes	Fixed – 32 bytes
	TC2	NA	Fixed – 32 bytes
	TC3	NA	Fixed – 32 bytes
Transfer Completion Interrupts		2 (Shadow Region, 0,1)	6 (Shadow Region 0,1,4,5,6,7)
Error Interrupts		3 (Global + TC0 + TC1)	5 (Global+TC0+TC1 +TC2 +TC3)

The 64 possible EDMA channel synchronization events are predefined to various sources on the device. Table 11 shows a comparison of the DM6446 and DM6467 EDMA channel synchronization events.

Table 11. EDMA Channel Synchronization Events Comparison

EDMA Channel	Event Name	DM6446 Event Description	EDMA Channel	Event Name	DM6467 Event Description
0-1	-	Reserved	0-3	-	Unused
2	REVT	ASP Transmit Event	4	AXEVTE0	McASP0 transmit Event
3	REVT	ASP Receive Event	5	AXEVTO0	McASP0 transmit Event
4	HISTEVT	VPSS Histogram Event	6	AXEVT0	McASP0 transmit Event
5	H3AEVT	VPSS H3A Event	7	AREVTE0	McASP0 receive Event
6	PRVUEVT	VPSS Previewer Event	8	AREVTO0	McASP0 receive Event
7	RSZEVT	VPSS Resizer Event	9	AREVT0	McASP0 receive Event
8	IMXINT	VICP Interrupt	10	AXEVTE1	McASP1 Transmit Event
9	VLCSINT	VICP VLCD Interrupt	11	AXEVTO1	McASP1 Transmit Event
10	ASQINT	VICP ASQ Interrupt	12	AXEVT1	McASP1 Transmit Event
11	DSQINT	VICP DSQ Interrupt	13-15	-	Unused
12	-	Reserved	16	SPIXEVT	SPI Transmit Event
13	-	Reserved	17	SPIREVT	SPI Receive event
14	-	Reserved	18	URXEVT0	UART 0 Receive Event
15	-	Reserved	19	UTXEVT0	UART 0 Transmit Event
16	SPIXEVT	SPI Transmit Event	20	URXEVT1	UART 1 Receive Event
17	SPIREVT	SPI Receive Event	21	UTXEVT1	UART 1 Transmit Event
18	URXEVT0	UART 0 Receive Event	22	URXEVT2	UART 2 Receive Event
19	UTXEVT0	UART 0 Transmit Event	23	UTXEVT2	UART 2 Transmit Event
20	URXEVT1	UART 1 Receive Event	24-27	-	Unused
21	UTXEVT1	UART 1 Transmit Event	28	ICREVT	I2C Receive Event
22	URXEVT2	UART 2 Receive Event	29	ICX	I2C Transmit Event
23	UTXEVT2	UART 2 Transmit Event	30-31	-	Unused
24	-	Reserved	32	GPINT0	GPIO 0 Interrupt Event
25	-	Reserved	33	GPINT1	GPIO 1 Interrupt Event
26	MMCRXEVT	MMC Receive Event	34	GPINT2	GPIO 3 Interrupt Event
27	MMCTXEVT	MMC Transmit Event	35	GPINT3	GPIO 3 Interrupt Event
28	I2CREVT	I2C Receive Event	36	GPINT4	GPIO 4 Interrupt Event
29	I2CXEVT	I2C Transmit Event	37	GPINT5	GPIO 5 Interrupt Event
30-31	-	Reserved	38	GPINT6	GPIO 6 Interrupt Event
32	GPINT0	GPIO 0 Interrupt Event	39	GPINT7	GPIO 7 Interrupt Event
33	GPINT1	GPIO 1 Interrupt Event	40	GPBNKINT0	GPIO bank 0 Interrupt Event

Table 11. EDMA Channel Synchronization Events Comparison (continued)

EDMA Channel	Event Name	DM6446 Event Description	EDMA Channel	Event Name	DM6467 Event Description
34	GPINT2	GPIO 3 Interrupt Event	41	GPBNKINT1	GPIO bank 1 Interrupt Event
35	GPINT3	GPIO 3 Interrupt Event	42	GPBNKINT2	GPIO bank 2 Interrupt Event
36	GPINT4	GPIO 4 Interrupt Event	43	CP_ECDCMP1	HDVICP1 ECDCMP Event
37	GPINT5	GPIO 5 Interrupt Event	44	CP_MC1	HDVICP 1 MC Event
38	GPINT6	GPIO 6 Interrupt Event	45	CP_BS1	HDVICP 1 BS Event
39	GPINT7	GPIO 7 Interrupt Event	46	CP_CALC1	HDVICP CALC Event
40	GPBNKINT0	GPIO Bank 0 Interrupt Event	47	CP_LPF1	HDVICP LPF Event
41	GPBNKINT1	GPIO Bank 1 Interrupt Event	48	TEVTL0	Timer 0 Interrupt Event
42	GPBNKINT2	GPIO Bank 2 Interrupt Event	49	TEVTH0	Timer 0 Interrupt Event
43	GPBNKINT3	GPIO Bank 3 Interrupt Event	50	TEVTL1	Timer 1 Interrupt Event
44	GPBNKINT4	GPIO Bank 4 Interrupt Event	51	TEVTH1	Timer 1 Interrupt Event
45	-	Reserved	52	PWM0	PWM 0 Event
46	-	Reserved	53	PWM 1	PWM 1 Event
47	-	Reserved	54-56	-	Unused
48	TINT0	Timer 0 Interrupt	57	CP_ME0	HDVICP ME Event
49	TINT1	Timer 1 Interrupt	58	CP_IPE0	HDVICP0 IPE Event
50	TINT2	Timer 2 Interrupt	59	CP_ECDCMP0	HDVICP0 ECDCMP Event
51	TINT3	Timer 3 Interrupt	60	CP_MC0	HDVICP 0 MC Event
52	PWM0	PWM 0 Event	61	CP_BS0	HDVICP 0 BS Event
53	PWM1	PWM 1 Event	62	CP_CALC0	HDVICP CALC Event
54	PWM2	PWM 2 Event	63	CP_LPF0	HDVICP LPF Event
55-63	-	Reserved			

For detailed information regarding the use of EDMA on the DM6467, see the *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA3) Controller User's Guide* (SPRUEQ5).

4.6 Peripheral Component Interconnect (PCI) Interface

While the DM6446 does not feature a PCI interface, the DM6467 does, therefore, this added capability can be utilized in DM6467 systems.

The DM6467 PCI interface is compatible with the industry-standard PCI interface version 2.3, which allows communication with devices compliant to the PCI Local Bus Specification Revision 2.3. The PCI peripheral support PCI-bus operation of speeds up to 33 MHz and uses a 32-bit data/address bus. The PCI interface can operate in either master or slave mode.

On the DM6467 device, the pins of the PCI peripheral are multiplexed with the pins of the EMIFA, GPIO, HPI, and ATA peripherals.

For detailed information regarding the use of the PCI interface on the DM6467, see the *TMS320DM646x DMSoC Peripheral Component Interconnect (PCI) User's Guide* (SPRUER2).

4.7 Serial Ports

The DM6446 and the DM6467 feature serial port interfaces to provide connectivity to a wide variety of external devices including codecs, communications peripherals, and other processors. The DM6446 features an audio serial port (ASP), while the DM6467 features two multi-channel audio serial ports (McASP). The following sections describe migration between these peripheral modules in detail.

4.7.1 ASP Serial Port

The DM6446 features an ASP interface, while the DM6467 does not; therefore, DM6446 applications utilizing the ASP requires some modifications when migrating between these two devices.

4.7.2 McASP Serial Port

While the DM6446 does not feature the McASP peripheral, the DM6467 does, therefore, this added capability can be utilized in the DM6467 systems.

The DM6467 McASP functions as a general-purpose audio serial port optimized for the needs of multi-channel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, inter-integrated sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

The McASP0 section consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The McASP0 module also includes a pool of four shift registers that can be individually configured to operate as either transmit data or receive data.

The DM6467 McASP1 module is a reduced feature version of the McASP peripheral. This module provides a single transmit-only shift register and can transmit data in DIT format only.

For detailed information regarding the use of the McASP on the DM6467, see the *TMS320DM646x DMSoC Multi-channel Audio Serial Port (McASP) User's Guide* (SPRUER1).

4.8 Serial Peripheral Interface (SPI) Port

The DM6446 and DM6467 feature a dedicated SPI port that allows a serial bit stream of programmed length to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMS and analog-to-digital converters (ADC). When migrating an application to the DM6467 the supported features and register configurations must be considered.

First, the SPI peripheral is clocked by a different clock on the DM6467 than on the DM6446. On the DM6446 device, the SPI internal system clock, output clock, and maximum clock bit rate is derived from SYSCLK5. The DM6467 SPI internal clock is derived from SYSCLK3 and the output clock generated (SPI_CLK) is a derivative of the internal SYSCLK3 clock. The maximum clock bit rate supported by the DM6467 SPI peripheral is SYSCLK3/4. The phase and polarity of the SPI clock signals for both devices are also programmable.

The DM6446 SPI allows serial communication with other SPI devices through a 3-pin or 4-pin mode interface; the DM6467 additionally features a 5-pin interface. Table 12 shows a comparison between the DM6446 and DM6467 SPI pins used to interface to external devices.

Table 12. DM6446 and DM6467 SPI Pins

DM6446			DM6467		
Pin	**Type** [1]	**Function**	**Pin**	**Type**	**Function**
SPI_CLK	O	Serial Clock	SPI_CLK	I/O	Serial clock input in slave mode, serial clock output in master mode
SPI_DI	I	Serial Data Input	SPI_SIMO	I/O	Serial data input in slave mode, serial data output in master mode
SPI_DO	O	Serial Data Output	SPI_SOMI	I/O	Serial data output in slave mode, serial data input in master mode
	O	Slave 0 chip select		I/O	Slave 0 chip select output in master mode, input in slave mode
	O	Slave 1 chip select		I/O	Slave 1 chip select output in master mode, input in slave mode
				I/O	Input in master mode, output in slave mode indicating slave is ready to be served

(1) I = Input, O = Output, I/O = Input/Output

Both devices support the multi-chip select operation for up to two SPI slave devices. The SPI on the DM6446 can operate as a master device, while the DM6467 operates as both a master and a slave device. On the DM6467, the MASTER and CLKMOD bits in the SPI Global Control Register 1 (SPIGCR1) must be set to 1 for SPI to function as a master and cleared to 0 for SPI to function as a slave.

Table 13. DM6446 and DM6467 SPI Feature Comparison

Feature	DM6446	DM6467
Operation Mode	Master	Master/Slave
Chip Selects	$\overline{\text{SPI\_EN0}}$, $\overline{\text{SPI\_EN1}}$	$\overline{\text{SPI\_CS1}}$, $\overline{\text{SPI\_CS0}}$
Wire Interface	3-pin, 4-pin modes	3-pin, 4-pin , 5-pin modes

For detailed information regarding the use of the SPI on the DM6467, see the *TMS320DM646x DMSoC Serial Peripheral Interface (SPI) User's Guide* (SPRUER4).

4.9 PLL/Clock Generator

Clock generators with PLLs are used to provide clocks for the DM6446 and DM6467. While the DM6446 and DM6467 PLLs are slightly different in architecture, their overall features allow them to provide comparable system clocking, which allows easy migration between the two devices.

4.9.1 DM6446 Phased-Locked Loop (PLL)

There are three PLLs on the DM6446 which are used to generate a variety of different clocks for the device from the input clocks. PLL1 can multiply its input clock by a programmable value, and the resultant clock can then be post-divided by 1, 2 or 3. Five system clocks are then generated for the device using fixed dividers of 1, 2, 3, 4, and 6 (note that the divide-by-four clock is reserved). These system clocks are then used to satisfy the clocking requirements for most of the different parts of the DM6446 device. PLL1 also provides the additional feature of being able to use the input clock directly, bypassing the PLL, and divide this by a programmable value between 1 and 32, to produce an additional clock which drives the CLKOUT0 output.

PLL2 can also multiply its input clock by a programmable value, and the resultant clock is then divided by programmable values between 1 and 16 to produce two output clocks. These two clocks are then used to satisfy the clocking requirements of the VPSS and the DDR2 interface on the device. PLL2 also provides the additional feature of being able to use the input clock directly, bypassing the PLL, and divide this by a programmable value between 1 and 32, to produce an additional clock which drives the DDR2 VTP.

Figure 1 and Figure 2 show the architecture of PLL1 and PLL2 on the DM6446.

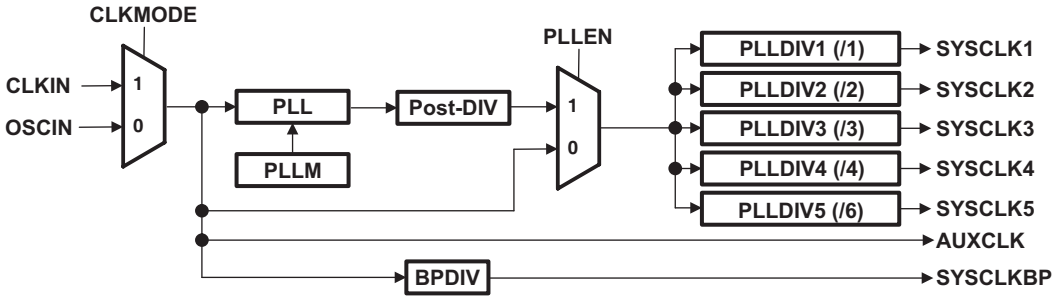


Figure 1. PLL1 Structure in the TMS320DM6446 DMSoC

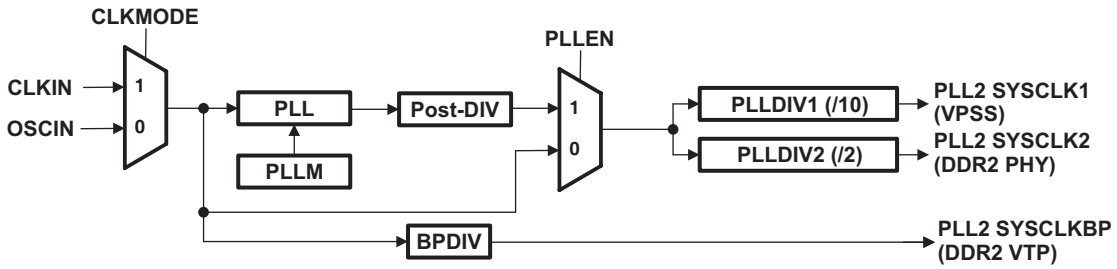


Figure 2. PLL2 Structure in the TMS320DM6446 DMSoC

PLL3 is used to provide clock for the USB interface. Its 24 MHz input clock is multiplied by 2.5 to generate a 60 MHz clock for the USB peripheral module.

4.9.2 DM6467 PLL

There are three PLLs on the DM6467 that are used to generate a variety of different clocks for the device from the input clocks. PLL1 supplies the primary DM6467 system clock. Software controls the PLL1 operation through the system PLL Controller 1 Register (PLLC1). PLL1 can multiply its input clock by a programmable value. PLLC1 generates several clocks from the PLL1 output clock for use by the various processors and modules. All PLL1 SYSCLKn dividers are programmable; however, divider values should not be changed to maintain the clock ratios between various modules of the device. Only the power-up default divider values for all PLL1 SYSCLKn dividers should be used for normal device operation.

PLL2 provides the clock from which the DDR2 memory controller clock is derived. This is a separate clock from the PLL1 clocks provided to the other components of the system. Software controls PLL2 operation through the PLL Controller 2 Register (PLLC2). The PLLM bits in the PLL Multiplier Control Register (PLLM) control the PLL2 multiplier. The PLL2 multiplier may be modified in software. The SYSCLK1 output clock divider value defaults to /1, but can be modified in software using the RATIO bit in the PLLDIV1.

Figure 3 and Figure 4 show the architecture of PLL1 and PLL2 on the DM6467

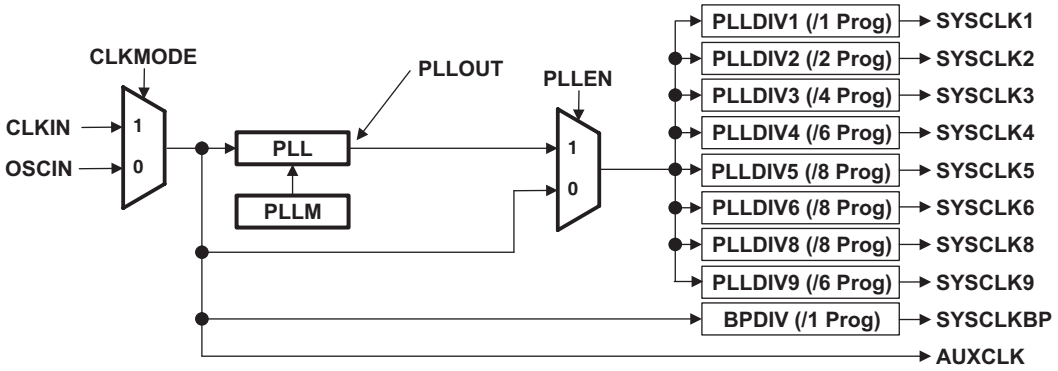
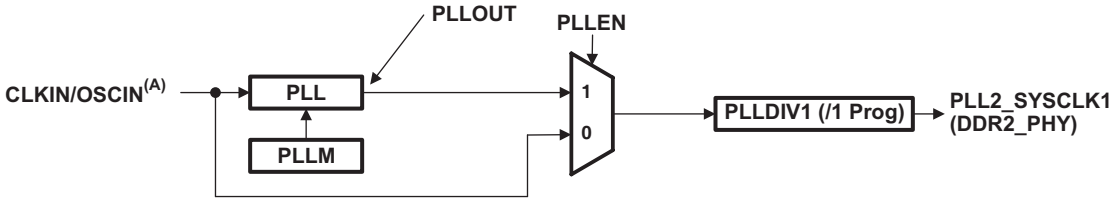


Figure 3. PLL1 Structure in the TMS320DM646x DMSoC



A. As selected by the PLL2 PLLCTL register

Figure 4. PLL2 Structure in the TMS320DM646x DMSoC

PLL3 is used to provide clock for the USB interface. Its 24 MHz input clock is multiplied by 2.5 to generate a 60 MHz clock for the USB peripheral module.

The PLLs can be bypassed in the DM6467. Bypassing the PLLs sends the PLL reference clock to post dividers of the PLLC instead of the PLL VCO output. Bypass mode can be used to reduce the core and module clock frequencies to very low maintenance levels without using the PLL during periods of very low system activity. For detailed information regarding the use of the PLL/clock generators on the DM6467, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

4.10 Universal Asynchronous Receiver/Transmitter (UART)

The DM6446 and DM6467 feature the Universal Asynchronous Receiver/Transmitter (UART) peripheral module. Each device has 3 UART peripherals, which perform serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The functionality of the peripheral modules are different, therefore changes are necessary to migrate an application from the DM6446 to the DM6467.

First, the DM6467 UART peripheral module does not utilize the same bit clock as the DM6446. The DM6446 UART bit clock is derived from a fixed on-chip 27-MHz clock which supports up to 128000 bps maximum data rate. The DM6467 UART bit clock is derived from the 24 MHz clock, AUX_CLKIN. For detailed information on the PLLs and clock distribution on the processor, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

Table 14. DM6467 UART Signal Descriptions

Signal	Pin	Type [1]	Description	Default
RX	URXD	I	Serial data input for all modes	Unknown
TX	UTXD	O	Serial data output in UART modes. In other modes, this pin is set to the reset value (inactive state)	1
IRTX	$\overline{\text{URTS}}$	O	Serial data output in IrDA modes. In other modes, this pin is set to the reset value (inactive state) Pin multiplexed with RTS at the pin-out	0
RCTX	UTXD	O	Serial data output in CIR mode. In other modes, this pin is set to the reset value (inactive state). Pin multiplexed with TX at the pin-out	0
$\overline{\text{CTS}}$	$\overline{\text{UCTS}}$	I	Clear to send. Active low modern status signal. Reading MSR[4] checks the condition of $\overline{\text{CTS}}$. Reading MSR[0] checks a change of state of $\overline{\text{CTS}}$ since the last read of MSR. $\overline{\text{CTS}}$ is used in autp-CTS mode to control the transmitter.	Unknown
$\overline{\text{RTS}}$	$\overline{\text{URTS}}$	O	Request to send. When active (low), the module is ready to receive data. Setting MCR[1] activates $\overline{\text{RTS}}$. It becomes inactive as a result of a module reset, loop back mode or by clearing MCR[1]. In auto-$\overline{\text{RTS}}$ mode, it become inactive as a result of the receiver threshold logic	1
SD	$\overline{\text{UCTS}}$	O	SD mode is used to configure the transceivers. The SD pin-out is an inverted value of ACREG[6]. Pin multiplexed with CTS and the pin-out.	1
DSR	$\overline{\text{UDSR0}}$ [2]	I	Data set ready. Active-low modem status signal. Reading MSR[5] checks the condition of DSR. Reading MSR[1] checks a change of state of DSR since the last read of MSR.	Unknown
$\overline{\text{DTR}}$	$\overline{\text{UDTR0}}$ [2]	O	Data terminal ready. When active (low), this signal informs the modem that the module is ready to communicate. It's activated by setting MCR[0].	1
$\overline{\text{DCD}}$	$\overline{\text{UDTR0}}$ [2]	I	Data carrier detect. Active-low modem status signal. The condition of $\overline{\text{DCD}}$ can be checked by reading MSR[7] and any change in its state can be detected by reading MSR[3].	Unknown
$\overline{\text{RI}}$	$\overline{\text{URIN0}}$ [2]	I	Ring Indicator. Active-low modem status signal. The condition of $\overline{\text{RI}}$ can be checked by reading MSR[6] and any change in its state can be detected by reading MSR[2].	Unknown

(1) I = Input, O = Output
(2) Only supported on UART0

In UART mode, the module uses a wired interface for serial communication with a remote device. The module can be placed in an alternate mode (FIFO mode) relieving the processor of excessive software overhead by buffering the received/transmitted characters. On the DM6467, both receiver and transmitter FIFOs can store up to 64 bytes of data (plus three additional bits of error status per byte for the receiver FIFO) and have selectable trigger levels. The DM6446 has a 16-byte FIFO.

The DM6467 UART module is also capable of performing standard infrared communication in slow infrared mode and medium infrared mode defined by the Infrared Data Association (IRDA). The module also supports consumer infrared communications that uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote control applications.

The UARTs have dedicated interrupt signals to the ARM CPU and the interrupts are not multiplexed with any other interrupt source.

The DM6446 has two DMA events in the FIFO mode: URXEVT and UTXEVT. Table 15 lists the UART EDMA events available on the DM6467

Table 15. DM6467 UART EDMA Events

Event	Acronym	Source
18	URXEVT0	UART0 Receive Event
19	UTXEVT0	UART0 Transmit Event
20	URXEVT1	UART1 Receive Event
21	UTXEVT1	UART1 Transmit Event
22	URXEVT2	UART2 Receive Event
23	UTXEVT2	UART2 Transmit Event

Both devices utilize pin multiplexing to accommodate the largest number of peripheral functions in the smallest possible package.

For detailed information regarding use of the UART peripherals on the DM6467 see the *TMS320DM646x DMSoC Universal Asynchronous Receiver/Transmitter (UART) User's Guide* (SPRUER6).

4.11 Timers

The DM6446 and DM6467 feature two 64-bit timers, each of which can also be operated as two 32-bit timers, and one 64-bit watchdog timer. The same timer peripheral modules are used on both devices, however, there are some minor differences in using these peripherals on the two devices. The following sections describe the migration of applications using these two peripherals from the DM6446 to the DM6467 device.

4.11.1 General-Purpose Timers

The DM6446 and DM6467 utilize the same timer peripheral modules; therefore, migration of an application utilizing the general-purpose timers from the DM6446 to the DM6467 requires little, if any, modification of hardware or software.

The DM6446 and DM6467 support four modes of operation: as a 64-bit general-purpose timer, as dual unchained 32-bit timers, or as dual-chained 32-bit timers. These timers can be used to generate periodic interrupts or EDMA synchronization events.

There are some slight differences in the number of off-chip I/O signals provided on each device. The DM6446 device provides one external clock input for the two timers, whereas, the DM6467 device provides three. The devices can also use an internal or external clock source for the counter period. The DM6446 uses one clock source bit in the TCR register, whereas, the DM6467 uses two. Accordingly, the DM6467 can easily support any timer functionality required in migrating a DM6446 application to the DM6467.

Table 16. DM6446/DM6467 General-Purpose Timer Comparison

Timer Feature		DM6446	DM6467
64–bit Timers		2	2
Dual 32-bit mode support		Yes	Yes
Number of possible timer events	64-bit mode	2	2
	32-bit mode	4	4
Number of External Clock Inputs		1	3
Number of Clock Source bits		1	2

For detailed information regarding the use of DM6467 general-purpose timers, see the *TMS320DM646x DMSoC 64-Bit Timer User's Guide* (SPRUER5).

4.11.2 Watchdog Timer

The DM6446 and DM6467 utilize the same watchdog timer peripheral modules; therefore, migration of an application utilizing the watchdog timers from the DM6446 to the DM6467 requires little, if any, modification of system software.

The watchdog timers can be extremely useful, especially in real time systems, to allow the capability to recover in case of unexpected events which might otherwise cause the system to stop functioning properly. The DM6446 and DM6467 watchdog timers are 64 bits long, and both allow the capability to interrupt or reset the device if the watchdog timer is not serviced at a programmable interval set up by you. Note that the watchdog timers are clocked exclusively from internal clock sources, and do not generate any outputs from the device.

For detailed information regarding the use of DM6467 watchdog timers, see the *TMS320DM646x DMSoC 64-Bit Timer User's Guide* (SPRUER5).

4.12 Ethernet Media Access Controller (EMAC)

The DM6446 and DM6467 feature an IEEE 802.3 compliant, EMAC peripheral that provides Ethernet interface capability. The Ethernet interface is comprised of the EMAC and the physical layer (PHY) device management data input/output (MDIO) module. The EMAC controls the flow of packet data from the DSP to the PHY, and the MDIO module controls PHY configuration and status monitoring.

The DM6446 and DM6467 EMAC modules feature synchronous 10/100 Mbps operation in either half-duplex or full-duplex mode with a standard media independent interface (MII) to the PHY. Additionally, the DM6467 features synchronous 1000 Mbps operation in full-duplex mode with a gigabit media independent interface (GMII) to the PHY.

The frequencies for transmit and receive clocks are fixed by the IEEE 802.3 specifications. These clocks are inputs to the EMAC module that operate at 2.5 MHz in 10-Mbps mode, 25 MHz in 100-Mbps mode and 125 MHz in 1000-Mbps mode (DM6467 only).

The EMAC and the MDIO modules interface to the DSP through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module provides a local memory space to hold EMAC packet buffer descriptors and includes the bus arbiter, and interrupts logic control.

The DM6446 and DM6467 EMAC control modules include 8K bytes of internal memory, which is essential for allowing the EMAC to operate more independently of the CPU. The bus arbiter is used to arbitrate between the CPU and EMAC buses for access to internal descriptor memory and internal EMAC buses for access to system memory.

The DM6446 EMAC control module combines multiple interrupt conditions generated by the EMAC and MDIO modules into a single interrupt signal that is mapped to a CPU interrupt via the CPU interrupt controller. The DM6467 control module has four separate interrupt signals that can be individually enabled for each channel by the Receive Threshold Interrupt Enable register (CMRXTHRESHINTEN), Receive Interrupt Enable Register (CMRXINTEM), Transmit Interrupt Enable Register (CMTXINTEN), and Miscellaneous Interrupt Enable Register (CMMISCINTEN). Table 17 shows the DM6467 control module interrupts.

Table 17. DM6467 EMAC Control Module Interrupts

ARM Event	Acronym	Source
24	MAC_RXTH	EMAC receive threshold
25	MAC_RX	EMAC receive
26	MAC_TX	EMAC transmit
27	MAC_MISC	EMAC miscellaneous

The DM6467 control module features interrupt pacing for receive and transmit pulse interrupts. The receive threshold and miscellaneous interrupts can not be paced. The interrupt pacing feature limits the number of interrupts to the CPU during a given period of time. For heavily loaded systems in which interrupts can occur at a very high rate, the performance benefit is significant due to minimizing the overhead associated with servicing each interrupt.

The DM6467 module uses the same pins for the MII and GMII modes of operation; only one mode can be used at a time. The EMAC on the DM6446 and the DM6467 can only be controlled by the ARM CPU.

For more detailed information regarding the use of the EMAC on the DM6467, see the *TMS320646x DMSoC Ethernet Media Access Controller (EMAC)/ Management Data Input/Output (MDIO) Module User's Guide* (SPRUEQ6).

4.13 Universal Serial Bus (USB) Interface

The DM6446 and DM6467 feature a USB controller. The USB peripheral modules are functionally the same; therefore, migration of an application utilizing the USB interface from the DM6446 to the DM6467 requires little, if any, modification of hardware or software.

The USB controller on the DM6446 and DM6467 can be used as either a host or a peripheral. As a host, it supports all three speeds low (1.5 Mbps), full (12 Mbps), and high (480 Mbps) in point-to-point data transfers with another peripheral or device, or multiple peripherals/devices via a HUB in a multipoint setup. As a peripheral, it supports high-speed (480 Mbps) and full-speed (12 Mbps) operations.

Table 18 presents the USB pins available on the DM6467.

Table 18. DM6467 USB Pins

Pin	Type[1]	Function
AUX_MXI/AUX_CLKIN	I	Crystal input for AUX oscillator
AUX_MXO	O	Crystal output for AUX oscillator
AUX_DV_{DD18}	S	1.8 V power supply for AUX oscillator I/O
AUX_CV_{DD}	S	1.2 V power supply for AUX oscillator
AUX_DV_{SS}	GND	Ground for AUX oscillator I/O
AUX_V_{SS}	GND	Ground for AUX oscillator. Connect to crystal load capacitors. Do not connect to board ground (V_{SS}).
USB_DP	A I/O	USB data differential signal pair (positive/negative)
USB_DN	A I/O	USB data differential signal pair (positive/negative)
USB_R1	A I/O	USB current reference. This must be connected via a 10kΩ ± 1% resistor to USB_V_{SSREF}
USB_DRVVBUS/ GPIO22	I/O	When used for USB and the USB controller is operating as a host, this signal is driven by the USB controller to enable the external VBUS charge pump.
USB_V_{SSREF}	GND	Ground for current reference
USB_V_{DDA3P3}	S	Analog 3.3 V power supply for USB
USB_V_{DD1P8}	S	1.8 V I/O power supply for USB
USB_$V_{DD1P2LDO}$	R	USB core power supply LDO regulator output. This must be connected via 1 μF capacitor to ground. Do not connect this to other supply pins.

(1) A= Analog Signal, GND = Ground, I = Input, O = Output, R = Reference Voltage, S = Supply Voltage

When the DM6467 USB controller assumes the role of a host, it is required to supply a 5 V power to an attached device through its VBUS line. To achieve this task, the DM6467 USB controller requires the use of an external logic (or charge pump) capable of sourcing a 5 V power. The USB_DRVVBUS is used as a control signal to enable/disable the external logic to either source or disable power on the VBUS line.

On the DM6467 DMSoC, there is no connection to PHY VBUS input since on-the-go (OTG) is not supported. Since the OTG feature is not supported, controller behavior as a host or peripheral is not evaluated by hardware automatically via cabling. Instead, you need to program the USBID bit of the USBTCL register in the system module to select the USB as a host or a peripheral. The USB controller is operated by ARM through the memory mapped registers.

For more detailed information on the USB interface, see the *TMS320DM646x DMSoC Universal Serial Bus (USB) Controller User's Guide* (SPRUER7).

4.14 ATA/ATAPI Interface

The DM6446 and DM6467 feature an ATA/ATAPI interface, also known as an IDE controller. This module is the traditional choice of communication medium between a portable computer (PC) and a hard-disk drive. The IDE controller complies with the ATA/ATAPI-6 and compact flash V2.0 specifications. The host controller logic supports PIO, multiword DMA and ultra DMA (ultra ATA) modes. The ATA/ATAPI modules are functionally the same; therefore, migration of an application utilizing the ATA/ATAPI interface from the DM6446 to the DM6467 requires little, if any, modification of hardware or software.

The most notable difference between the ATA peripheral modules on these two devices are signal location within the device pin outs, and pin multiplexing. Table 19 provides the supported IDE controller signals on the DM6446 and DM6467.

Table 19. DM6446 and DM6467 Supported IDE Controller Signals

Terminal Names		Direction From IDE Controller	Description
DM6446	DM6467		
$\overline{\text{ATA\_CS0}}$	$\overline{\text{ATA\_CS0}}$	Output	Chip select signals 0 and 1
$\overline{\text{ATA\_CS1}}$	$\overline{\text{ATA\_CS1}}$		
ATA0_EM_BA0	ATA_HA0	Output	Device address bits[2:0]
ATA1_EM_BA1	ATA_HA1		
ATA2_EM_A0	ATA_HA1		
EM_D[15:0]	ATA_D[15:0]	Input/Output	Host read/write data bus
DMARQ	ATA_DMARQ	Input	Device DMA request
$\overline{\text{DMACK}}$	$\overline{\text{ATA\_DMACK}}$	Output	Host DMA acknowledge
$\overline{\text{WAIT\_BSYN}}$	ATA_IORDY	Input	Device I/O ready during PIO transaction
			DMA ready during ultra-DMA write
			DMA strobe during ultra-DMA read
$\overline{\text{READ\_OE}}$	$\overline{\text{ATA\_HIOR}}$	Output	PIO read transaction indicator
			DMA ready during ultra-DMA read
			DMA data strobe during ultra-DMA write
$\overline{\text{WRITE\_OE}}$	$\overline{\text{ATA\_HIOW}}$	Output	PIO write transaction indicator
			Stop ultra-DMA data read/write bursts
INTRQ_EM_RNW	ATA_INTRQ	Input	Attached device interrupt request
HDDIR	ATA_DDIR	Output	External level shifter direction indicator

To ensure proper operation, the operating frequency of the ATA controller clock should be chosen in such a way that it is at least twice as fast as the ATA data strobe frequency in order to achieve expected throughout.

For more detailed information regarding the use of the ATA controller on the DM6467, see the *TMS320DM646x DMSoC ATA Controller User's Guide* (SPRUEQ3).

4.15 MultiMedia Card/Secure Data Memory Card (MMC/SD)

The DM6446 features an MMC/SD interface, however the DM6467 does not. Therefore, if an MMC/SD interface is required in a DM6467 system; other provisions must be made for this.

One possible approach to providing MMC/SD capability in a DM6467 system is to connect an interface device or FPGA to one of the other available interfaces on the DM6467, for example the EMIF.

4.16 I2C Interface

The DM6446 and the DM6467 feature an interface to I2C-compatible external devices. The I2C peripheral modules on these two devices are functionally the same; therefore, migration of an application utilizing the I2C interface from the DM6446 to the DM6467 requires little, if any, modification of hardware or software.

Although the DM6446 and DM6467 I2C peripheral modules are functionally the same, there are some minor differences in their usage when migrating applications between these two devices. The most notable difference in usage between the I2C peripheral modules on these two devices is the signal locations within the device pin outs.

The DM6446 and DM6467 I2C peripheral supports 2-bit to 8-bit values. Both devices also support a 7-bit and 10-bit addressing mode and a free data mode.

For more information regarding the use of the I2C peripheral module, see the *TMS320DM646x DMSoC Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUER0).

4.17 VLYNQ Interface

The DM6446 and DM6467 feature a VLYNQ interface, and the same peripheral module is used on both devices; therefore, migration of an application utilizing the VLYNQ interface from the DM6446 to the DM6467 requires little, if any, modification of hardware or software. The VLYNQ communications interface port is a low pin count, high-speed, point-to-point serial interface used for connecting to host processors and other VLYNQ compatible devices. This interface can be implemented in either a host-to-peripheral or peer-to-peer fashion.

The VLYNQ port utilizes a full-duplex serial bus where transmit and receive operations occur separately and simultaneously without interference. VLYNQ enables the extension of an internal bus segment to one or more external physical devices. The external devices are mapped to local physical address space, and appear as if they are on the internal bus of the DSP. The external devices must also have a VLYNQ interface.

VLYNQ uses a simple block code (8b/10b) packet format and supports in-band flow control so that no extra terminals are needed to indicate that overflow conditions might occur. The external device can also initiate read and write transactions.

Since the DM6446 and the DM6437 utilize the same VLYNQ interface peripheral module, the major significant differences in usage between the VLYNQ peripheral modules on these two devices are signal locations within the device pinouts, and the pin multiplexing configuration settings.

Other than the signal locations and pin multiplexing, one difference between the two VLYNQ modules are the contents of the Chip Version Register (CHIPVER). The VLYNQ module also has a single interrupt source mapped to the ARM interrupt controller (AINTC). Table 20 shows the ARM Event for the devices.

For more information on the AINTC, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

Table 20. DM6446/DM6467 VLQINT ARM Event

	DM6446	DM6467
ARM Event	38	31
Acronym	VLQINT	VLQINT

For detailed information regarding use of the VLYNQ peripheral on the DM6467, see the *TMS320DM646x DMSoC VLYNQ Port User's Guide* (SPRUER8).

4.18 Host Port Interface (HPI)

The DM6446 and DM6467 feature the HPI peripheral through which an external host can communicate with the DSP device. Using the HPI, the host can access most internal memory and memory-mapped resources, with only a few exceptions. The host functions as the master of this interface, which greatly increases flexibility of communications with the DSP device.

The HPI peripheral modules used on these two devices are functionally the same; therefore, migration of an application utilizing the HPI from the DM6446 to the DM6467 requires little, if any, modification of hardware or software. There are, however, a few differences in HPI usage between these two devices. The most basic of these differences are the signal locations within the device pinouts, and the pin multiplexing setup on the two devices.

The DM6446 HPI shares the DaVinci EMIFA 16-bit data bus pins for multiplexed address/data and supports a 16-bit multiplexed mode and dual half-word cycles. The DM6467 HPI includes a user configurable 16- or 32-bit wide data bus with configurable single full-word cycle and dual half-word cycle access modes.

Additionally the HPI clock source for the DM6467 is different from that of the DM6446. The DM6446 clock is derived from SYSCLK5, which is the PLL1 clock divided by 6. The DM6467 HPI clock is derived from SYSCLK3, which is the PLL0 clock divided by 4.

The HPI on both devices can be used by the host to access Power and Sleep Controller (PSC) registers and the HPI configuration registers. The DM6446 also has access to PLL1 and PLL2 registers, whereas, the DM6467 has access to the PLL0 and PLL1 registers.

There are also differences within the access type the host selects by driving the appropriate levels on the HCNTL[1:0] pins of the HPI. Table 21 describes the selectable access types for the two devices.

Table 21. Access Types Selectable With the HCNTL Signals

	DM6446		DM6467	
Access Type	**HCNTL1**	**HCNTL0**	**HCNTL1**	**HCNTL0**
HPIC Access	0	0	0	0
HPIA Access	1	0	0	1
HPID Access with autoincrementing	0	1	1	0
HPID Access without autoincrementing	1	1	1	1

Table 22. Cycle Types Selectable With the HCNTL and HR/W Signals

	DM6446			DM6467		
Cycle Type	**HCNTL1**	**HCNTL0**	**HR/W**	**HCNTL1**	**HCNTL0**	**HR/W**
HPIC write Cycle	0	0	0	0	0	0
HPIC read cycle	0	0	1	0	0	1
HPID write cycle with auto incrementing	0	1	0	1	0	0
HPID read cycle with auto incrementing	0	1	1	1	0	1
HPIA write Cycle	1	0	0	0	1	0
HPIA read cycle	1	0	1	0	1	1
HPID write cycle without auto incrementing	1	1	0	1	1	0
HPID read cycle without auto incrementing	1	1	1	1	1	1

For more detailed information regarding the use of the DM6467 HPI, see the *TMS320DM646x DMSoC Host Port Interface (HPI) User's Guide* (SPRUES1).

4.19 Pulse-Width Modulator (PWM) Outputs

The DM6446 and the DM6467 both feature dedicated PWM outputs. The PWM peripheral provides a way to generate a pulse periodic waveform for motor control or can act as a DAC with some external components. Each PWM output is implemented as a timer with a period counter and a first-phase duration comparator, where the bit widths of the period and first-phase duration are both programmable. The period and the first-phase duration are controlled with 32-bit counters, and each PWM output can also be used to generate an interrupt and/or EDMA sync event. There are a few key components to consider when migrating an application from the DM6446 to the DM6467.

First, notice the DM6446 peripheral module provides three PWM outputs and the DM6467 provides two PWM outputs

Additionally, the peripherals are controlled by different clock sources. The DM6446 clock is PWM peripheral is driven by the equivalent DM6446 input clock, while the DM6467 PWM input clock is derived from SYSCLK3, which is the PLL0 clock divided by 4.

The PWM module can operate in either one-shot or continuous mode. The DM6446 PWM features an 8-bit repeat counter for one-shot operation, which produces N+1 periods of the waveform, where N is the repeat counter value. The DM6467 PWM features a 32-bit repeat counter for one shot operation.

The only other difference to note between the PWM peripheral modules on these two devices are the signal locations within the device pinouts, and the pin multiplexing configuration settings.

For detailed information regarding use of the PWM output capabilities on the DM6467, see the *TMS320DM646x DMSoC Pulse-Width Modulators (PWM) User's Guide* (SPRUER3).

4.20 General Purpose Input/Output (GPIO)

The DM6446 and the DM6467 feature a selection of pins that can be configured to provide independent single-bit general-purpose digital I/O. These GPIO bits can be used to interface to external signals, and the generate interrupts and EDMA synchronization events.

Since the GPIO configuration differs between these two devices, software modifications may be necessary to migrate from the DM6446 to the DM6467. Specifically, the DM6446 features up to 54 1.8 V GPIO pins and up to 17, 3.3 V GPIO pins, while the DM6467 features up to 33, 3.3 V GPIO pins.

Note that although these two devices offer a different number of GPIO bits, the GPIO bit function is configured by similar sets of control registers located at the same base address on both devices. Therefore, software modifications required when migrating an application from the DM6446 to the DM6467 will frequently be minimal.

First, notice that the GPIO peripheral modules utilize different clock sources. The DM6446 input clock to the GPIO peripheral is the SYSCLK5 chip-level clock (PLL1/6), while the DM6446 GPIO input clock is PLL0 divided by 6. The maximum operation speed for both peripheral modules is 10 MHz.

Additionally, on both devices, many GPIO pins are multiplexed with other pin functions; therefore, GPIO pin availability depends on what other functions are used on the device.

The GPIO peripheral can send an interrupt to the ARM and/or the DSP. On the DM6467 all GPIO signals can be configured to generate interrupts, while on the DM6446 only a subset of the GPIO signals can be configured to generate interrupts. Interrupts from GPIO signals at both independent and group level is supported on both devices.

For detailed information regarding the use of GPIO on the DM6467, see the *TMS320DM646x DMSoC General-Purpose Input/Output (GPIO) User's Guide* (SPRUEQ8).

5 Interrupt Considerations

The DM6446 and DM6467 both support servicing of a wide range of interrupts from a variety of sources, both on and off chip. Each device uses its own multiplexing scheme to select the specific sources that are allowed to interrupt their processors.

Both the ARM and the C64x+ are capable of servicing these interrupts; however, all of the device interrupts are routed to the ARM interrupt controller with only a limited set routed to the C64x+ interrupt controller. The interrupts can be selectively enabled or disabled in either of the controllers. In typical applications, the ARM handles most of the peripheral interrupts and grants control to the C64x+, of interrupts that are relevant to DSP algorithms. Also, the ARM and DSP can communicated with each other through interrupts.

On the DM6446 and the DM6467, the ARM CPU core accepts two basic interrupts, a normal interrupt request (IRQ) and a fast interrupt request (FIQ). There are up to 64 possible total interrupt sources supported by the ARM interrupt architecture. There are 57 interrupt sources used on the DM6446 device and 60 interrupt sources used on the DM6467 device. These interrupt sources are multiplexed to either the IRQ and or FIQ interrupt, at eight different priority levels. This multiplexing and the interrupt priority level assignments are controlled by bits in the various interrupt controller registers.

When one of these interrupts occurs, it is prioritized against any other pending and enabled interrupts, and sent to the ARM as either an IRQ or an FIQ. The ARM CPU then reads the address of the appropriate interrupt service routine to branch to from the interrupt entry table, loaded by the processor initialization routine. In this way, any of the possible interrupts may be serviced.

On the DSP CPU core, sources that are allowed to interrupt the CPU may be chosen from a possible selection of 128 system events, in addition to three interrupts that are always selected, allocated to reset, NMI, and a hardware exception interrupt. The 128 possible system events are mapped to 12 independent interrupts using the interrupt selector, interrupt combiner, and exception combiner modules. The resultant 15 interrupt signals are sent to the CPU. Some of the possible interrupts on the DSP CPU can be generated from GPIO signals, and the polarities of these signals used to generate the interrupts are programmable through the GPIO control registers.

The 128 system event sources from which the 12 interrupts routed to the CPU are chosen are hard-wired on the DM6446 and the DM6467. The interrupts that are actually routed to the CPU in each device are chosen from this selection as described above. This interrupt selection structure allows for maximum flexibility within the system for allocation of necessary interrupt servicing. Table 22 presents a comparison of the 128 possible system events for generating interrupts available on the DM6446 and the DM6467.

Table 23. Interrupt System Event Comparison

	DM6446		DM6467	
Number	**Acronym**	**Source**	**Acronym**	**Source**
0	EVT0	C64x+ Int Ctl 0	EVT0	C64x+ Int Ctl 0
1	EVT1	C64x+ Int Ctl 1	EVT1	C64x+ Int Ctl 1
2	EVT2	C64x+ Int Ctl 2	EVT2	C64x+ Int Ctl 2
3	EVT3	C64x+ Int Ctl 3	EVT3	C64x+ Int Ctl 3
4	TINT0	Timer 0 – TINT12	TINTL0	Timer 0 lower – TINT12
5	TINT1	Timer 0 – TINT34	TINTH0	Timer 0 upper – TINT34
6	TINT2	Timer 1 –TINT12	TINTL1	Timer 1 lower – TINT12
7	TINT3	Timer 1 – TINT34	TINTH1	Timer 1 upper – TINT34
8		Reserved		Reserved
9	EMU_DTDMA	C64x+ EMC	EMU_DTDMA	C64x+ EMC
10		Reserved		Reserved
11	EMU_RTDXRX	C64x+ RTDX	EMU_RTDXRX	C64x+ RTDX
12	EMU_RTDXTX	C64x+ RTDX	EMU_RTDXTX	C64x+ RTDX
13	IDMAINT0	C64x+ EMC0	IDMAINT0	C64x+ EMC0
14	IDMAINT1	C64x+ EMC1	IDMAINT1	C64x+ EMC1
15		Reserved		Reserved
16	ARM2DSP0	ARM to DSP Controller 0	ARM2DSP0	ARM to DSP Controller 0
17	ARM2DSP1	ARM to DSP Controller 1	ARM2DSP1	ARM to DSP Controller 1
18	ARM2DSP2	ARM to DSP Controller 2	ARM2DSP2	ARM to DSP Controller 2
19	ARM2DSP3	ARM to DSP Controller 3	ARM2DSP3	ARM to DSP Controller 3
20		Reserved		Reserved
21		Reserved		Reserved
22		Reserved		Reserved
23		Reserved		Reserved
24		Reserved		Reserved
25		Reserved		Reserved
26		Reserved		Reserved
27		Reserved		Reserved
28		Reserved		Reserved
29		Reserved		Reserved
30		Reserved		Reserved
31		Reserved		Reserved
32		Reserved		Reserved
33		Reserved		Reserved
34		Reserved		Reserved

Table 23. Interrupt System Event Comparison (continued)

	DM6446		DM6467	
Number	**Acronym**	**Source**	**Acronym**	**Source**
35		Reserved		Reserved
36	EDMA3CC_INT1	EDMACC Interrupt Region 1		Reserved
37	EDMA3CC_ERRINT	EDMA CC Error		Reserved
38	EDMA3TC_ERRINT0	EDMA TC0 Error		Reserved
39	EDMA3TC_ERRINT1	EDMA TC1 Error		Reserved
40		Reserved		Reserved
41		Reserved		Reserved
42		Reserved		Reserved
43		Reserved		Reserved
44		Reserved		Reserved
45		Reserved		Reserved
46		Reserved		Reserved
47		Reserved		Reserved
48	ASPXINT	ASP Transmit		Reserved
49	ASPRINT	ASP Receive		Reserved
50		Reserved		Reserved
51		Reserved		Reserved
52		Reserved		Reserved
53		Reserved		Reserved
54		Reserved	AXINT0	McASP0 Transmit
55		Reserved	ARINT0	McASP0 Receive
56		Reserved	AXINT1	McASP1 Transmit
57		Reserved		Reserved
58		Reserved		Reserved
59		Reserved		Reserved
60		Reserved		Reserved
61		Reserved		Reserved
62		Reserved		Reserved
63		Reserved		Reserved
64		Reserved	GPIO0	GPIO
65		Reserved	GPIO1	GPIO
66		Reserved	GPIO2	GPIO
67		Reserved	GPIO3	GPIO
68		Reserved	GPIO4	GPIO
69		Reserved	GPIO5	GPIO
70		Reserved	GPIO6	GPIO
71		Reserved	GPIO7	GPIO
72		Reserved		Reserved
73		Reserved		Reserved
74		Reserved		Reserved
75		Reserved		Reserved
76		Reserved		Reserved
77		Reserved		Reserved
78		Reserved		Reserved
79		Reserved		Reserved
80		Reserved		Reserved

Table 23. Interrupt System Event Comparison (continued)

	DM6446		DM6467	
Number	Acronym	Source	Acronym	Source
81		Reserved		Reserved
82		Reserved		Reserved
83		Reserved		Reserved
84		Reserved	CCINT1	EDMA CC Region 1
85		Reserved	CCERRINT	EDMA CC Error
86		Reserved	TCERRINT0	EDMA TC0 Error
87		Reserved	TCERRINT1	EDMA TC1 Error
88		Reserved	TCERRINT2	EDMA TC2 Error
89		Reserved	TCERRINT3	EDMA TC3 Error
90		Reserved	IDEINT	ATA
91		Reserved		Reserved
92		Reserved		Reserved
93		Reserved		Reserved
94		Reserved		Reserved
95		Reserved		Reserved
96	INTERR	C64x+ Interrupt Controller Dropped CPU Interrupt Event	INTERR	C64x+ Interrupt Controller Dropped CPU Interrupt Event
97	EMC_IDMAERR	C64x+ EMC Invalid IDMA Parameters	EMC_IDMAERR	C64x+ EMC Invalid IDMA Parameters
98		Reserved		Reserved
99		Reserved		Reserved
100		Reserved		Reserved
101		Reserved		Reserved
102		Reserved		Reserved
103		Reserved		Reserved
104		Reserved		Reserved
105		Reserved		Reserved
106		Reserved		Reserved
107		Reserved		Reserved
108		Reserved		Reserved
109		Reserved		Reserved
110		Reserved		Reserved
111		Reserved		Reserved
112	PMC_ED	C64x+ PMC		Reserved
113		Reserved	PMC_ED	C64x+ PMC
114		Reserved		Reserved
115		Reserved		Reserved
116	UMCED1	C64x+ UMC 1	UMCED1	C64x+ UMC 1
117	UMCED2	C64x+ UMC 2	UMCED2	C64x+ UMC 2
118	PDCERR	C64x+ PDC	PDCINT	C64x+ PDC
119	PVCINT	C64x+ PDC	SYSCMPA	C64x+ SYS
120	PMCCMPA	C64x+ PMC	PMCCMPA	C64x+ PMC
121	PMCDMPA	C64x+ PMC	PMCDMPA	C64x+ PMC
122	DMCCMPA	C64x+ DMC	DMCCMPA	C64x+ DMC
123	DMCDMPA	C64x+ DMC	DMCDMPA	C64x+ DMC
124	UMCCMPA	C64x+ UMC	UMCCMPA	C64x+ UMC
125	UMCDMPA	C64x+ UMC	UMCDMPA	C64x+ UMC

Table 23. Interrupt System Event Comparison (continued)

	DM6446		DM6467	
Number	Acronym	Source	Acronym	Source
126	EMCCMPA	C64x+ EMC	EMCCMPA	C64x+ EMC
127	EMCDMPA	C64x+ EMC	EMCBUSERR	C64x+ EMC

For detailed information regarding the handling of interrupts on the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403), the *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8), and the *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871).

6 Bootloading Capabilities

The DM6446 and the DM6467 provide the capability to transfer code from an external location into RAM to be executed following reset. On both devices, the states of various input pins are sampled following reset, and the selected boot modes are determined based on these states.

The DM6446 and DM6467 contain two CPU cores bootloading of each of these CPU cores must be considered separately because both devices can execute their own independent code. The ARM CPU core controls the reset of the DSP CPU core; therefore, to some extent, the ARM CPU serves as the master of bootloading the DSP CPU. The DSP CPU does not contain its own dedicated bootloader program; therefore, all bootloading of code for the DSP is either performed by the ARM CPU or by an external device. This section presents the boot modes available on the DM6446 and the DM6467 ARM and DSP CPU cores.

6.1 DM6446 Bootloading

The DM6446 ARM CPU provides four bootload modes: host bootloading through the HPI, EMIF bootloading from NAND Flash, serial bootloading through UART0, and an EMIFA-boot mode. The EMIFA-boot mode does not transfer any code, but instead, branches directly to an external location (02000000h) in NOR Flash memory where it expects code.

For host bootloading through the HPI, the ARM bootloader expects that the code to be executed is loaded through the HPI by an external host and branches to this code once loading is completed. If EMIFA or serial bootloading is selected, the bootloader loads the code provided through either interface by an external device and then transfers control to this code.

The ARM-boot modes are selected by the BTSEL [1:0] pins. The configuration of the data and address bus width of the EMIF are selected by the EM_WIDTH and AEAW [4:0] pins when EMIF booting is used.

In the host-boot modes, the code is loaded into the DSP memory either by the ARM or by an external host through the HPI, and control is then transferred to this code after the DSP is released from reset by the ARM. In the other boot modes, no code is transferred, but the DSP is programmed to branch to either the fixed address of 42200000h or to an address provided by the ARM after the DSP is released from reset by the ARM.

The DSP-boot modes are selected by the DSP_BT pin, and, when EMIF booting is used, the configuration of the data and address bus width of the EMIF are selected by the EM_WIDTH and AEAW [4:0] pins.

6.1.1 DM6467 Bootloading

The DM6467 ARM CPU provides seven bootload modes: host boot loading through the HPI, EMIF bootloading from NAND Flash, serial bootloading through UART0, PCI-boot mode (with auto-initialization/ without auto-initialization), I2C master boot mode using Application Image Script (AIS) format, SPI-boot mode using AIS, and EMIFA-boot mode. The EMIFA-boot mode does not transfer any code, but instead, branches directly to an external location (0x42000000) in NOR Flash memory where it expects code.

For host bootloading through the HPI, the ARM bootloader expects that the code to be executed is loaded through the HPI by an external host and branches to this code once loading is completed. If EMIFA or serial bootloading is selected, the bootloader loads the code provided through either interface by an external device and then transfers control to this code.

The ARM-boot modes are selected by the BTMODE[3:0] pins, and when EMIF booting is used the address bus width of the EMIF are selected by the CS2BW pins.

For detailed information regarding use of the ARM bootloader see the document, *Using the TMS320DM6467 DMSoC Bootloader* (SPRAAS0).

There is one boot mode on the DSP CPU core, DSPBOOT, which determines DSP operation at reset. When DSPBOOT = 1, the DSP will boot itself. Under this scenario, DSP is released from reset without ARM intervention. The DSP boot address is set to an EMIFA address 0x4220 000h. DSP begins execution with instruction (L1P) cache enabled.

The DSPBOOT operation is overridden when ARM HPI or PCI boot is selected (BTMODE [3:0] = 001x). This is because ARM HPI/PCI boot selection forces the HPIEN or PCIEN bit in PINMUX0 to '1'. This enables UHPI/PCI functions of the EMIFA control and data pins and prevents the DSP from using EMIFA. DSPBOOT is treated as '0' internally when BTMODE [3:0] = 001x, regardless of the value at the configuration pin. The actual pin value should still be latched in the BOOTCFG register of the System module.

For more information on the DSP-boot mode, see the *TMS320DM6467 DMSoC Data Manual* (SPRS403).

Table 24. Comparison of Bootloading Capabilities on the DM6446 and DM6467

Timer Feature		DM6446		DM6467	
CPU		**ARM**	**DSP**	**ARM**	**DSP**
Number of Modes		4	4	7	1
Modes	Host	Yes	Yes	Yes	No
	Nand	Yes	No	Yes	No
	Serial	Yes	No	Yes	No
	EMIFA	Yes	Yes	Yes	Yes
	I2C	No	No	Yes	No
	SPI	No	No	Yes	No
	PCI	No	No	Yes	No
Selected by		BTSEL[1:0] EM_WIDTH AEAW[4:0]	DSP_BT EM_WIDTH AEAW[4:0]	BTMODE[3:0] CS2BW	DSP_BT

7 Power Management

In most DSP systems, power management is an important concern to allow DSP functions to perform with the lowest power cost and minimal battery drain possible. The DM6446 and DM6467 offer numerous options for power management. The devices provide several basic categories of power management options with variations.

The DM6446 DMSoC includes two separate power domains, *Always On* and *DSP*, while the DM6467 DMSoC system has a single power domain, the *Always On* power domain. The *Always On* power domain is always in the ON state when the chip is powered-on. The *Always On* domain is powered by the CV_{DD} pins of the DM6446 and DM6467 DMSoC. All of the DM6467 DMSoC modules reside within the *Always On* power domain.

On the DM6446, a separate domain called the *DSP* domain houses the C64x+ and VICP. The DM6446 DSP domain is not always on. The DSP power domain is powered by the CV_{DDDSP} pins of the DM6446.

Within the *Always On* power domain, the PSC on the DM6446 and DM6467 controls device power by gating off clocks to individual peripherals/modules. The PSC is composed of the global PSC (GPSC) module that contains memory-mapped registers, PSC interrupt control, and a state machine for each peripheral/module. A local PSC (LPSC) is associated with each peripheral/module and provides clock and reset control. The GPSC controls all of the LPSCs. The ARM subsystem does not have an LPSC module. ARM sleep mode is accomplished through the wait for interrupt instruction. Table 25 presents a comparison of the possible LPSC peripheral/module allocation assignments on the DM6446 and the DM6467.

Table 25. LPSC Peripheral/Module Allocation Assignment Comparison

LPSC Number	DM6446	DM6467
0	VPSS DMA	Reserved
1	VPSS MMR	C64x+ CPU
2	EDMACC	HDVICP0
3	EDMATC0	HDVICP1
4	EDMATC1	EDMACC
5	EMAC	EDMATC0
6	EMAC Memory Controller	EDMATC1
7	MDIO	EDMATC2
8	Reserved	EDMATC3
9	USB	USB
10	ATA/CF	ATA
11	VLYNQ	VLYNQ
12	HPI	HPI
13	DDR2 Memory Controller	PCI
14	EMIFA	EMAC/MDIO
15	MMC/SD/SDIO	VDCE
16	Reserved	Video Port
17	ASP	Video Port
18	I2C	TSIF0
19	UART0	TSIF1
20	UART1	DDR2 Memory Controller
21	UART2	EMIFA
22	SPI	McASP0
23	PWM0	McASP1
24	PWM1	CRGEN0
25	PWM2	CRGEN1
26	GPIO	UART0
27	TIMER0	UART1
28	TIMER1	UART2
29	Reserved	PWM0
30	Reserved	PWM1
31	Reserved	I2C
32	Reserved	SPI
33	Reserved	SPI
34	Reserved	GPIO
35	Reserved	TIMER0
36	Reserved	TIMER1
37	Reserved	Reserved
38	Reserved	Reserved
39	C64x+	Reserved
40	VICP	Reserved
41	-	Reserved
42	-	Reserved
43	-	Reserved
44	-	Reserved
45	-	Reserved

To manage power due to I/O buffers on the device, the DM6446 and DM6467 also provide the capability to power up or down groups of I/O pin buffers. This feature is controlled by writing to bits in the VDD3PDV_PWDN register. Note that this register controls only the power supply to the 3.3 V I/O buffers for each designated group of pins. The PSC determines the clock/power state of the peripheral.

The USB PHY can be powered down when not in use. The USB PHY is powered down via the DM6467 PHYDWN bit in the USBCTL register of the control module. USBCTL is described in the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403). Table 26 summarizes the power management features on the DM6446 and the DM6467.

Table 26. DM6446 and DM6467 Power Management Features

Power Management Features	Description
Clock Management	
PLL power-down	The PLLs can be powered down when not in use to reduce switching power
Module clock ON/OFF	Module clocks can be turned on/off to reduce switching power
Module clock frequency scaling	Module clock frequency can be selected to reduce switching power
ARM and DSP Sleep Management	
ARM wait-for-interrupt sleep mode	Disable ARM clock to reduce active power
DSP sleep modes	The DSP can be put into sleep mode to reduce switching power
3.3 V I/O power-down	The 3.3 V I/Os can be powered down to reduce I/O cell power
I/O Management	
USB Phy power-down	The USB Phy can be powered down to reduce USM I/O power
DAC power-down (DM6446 only)	The DAC's can be powered down to reduce DAC power

For more details on the DM6467 Power Management, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

8 PLL/Clock Modes at Reset

The DM6446 and DM6467 feature flexible clock generators that provide clocking to satisfy a wide variety of system requirements. To properly start up and initialize a DSP system, the clock generator must be able to provide appropriate clock signals to the device even before the device is released from reset. The DM6446 and DM6467 clock generators are designed to provide this capability.

Both of these devices can be clocked either by an external oscillator, or by using a crystal with the internal oscillator. The internal oscillator is enabled by default when reset is asserted, but can be disabled through software by writing to the PLL Controller 1 PLL Control Register (PLLCTL), if desired. The default clock mode for both devices at reset is a multiply by 1 of the input clock. Once the device is released from reset, the clock frequency can be changed through software by writing to registers in the PLL module. For additional information regarding considerations of PLL operation, see Section 4.9 of this document. The input clock frequency range on both devices is 20 MHz - 30 MHz.

Table 27 presents a summary of the DM6446 and DM6467 PLL and clock mode initialization.

Table 27. DM6446 and DM6467 PLL/Clock Modes at Reset

Feature	DM6446	DM6467
Input clock Frequency Range	20 MHz - 30 MHz	20 MHz - 30 MHz
On-chip Oscillator	Yes(1)	Yes(1)
Clock Mode at Reset	X1, oscillator enabled	x1, oscillator enabled
Clock Mode at Reset Determined by	Not Variable(2)	Not Variable(2)
S/W can change clock rate after reset	Yes	Yes

(1) (1) Oscillator is on by default. Turn it off in software after reset, if desired.
(2) (2) Bootloader may change clock frequency after resets, see Section 6

For detailed information regarding PLL and clock mode initialization, see the *TMS320DM6467 Digital Media System-on-chip Data Manual* (SPRS403), and the *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8).

9 Pin Multiplexing

The DM6446 and the DM6467 use multiplexing of functions on various pins to maximize device features and flexibility, while minimizing pin count, and package size and cost. Pin multiplexing is accomplished in a similar fashion on both devices, however, the actual implementation on each is different, therefore, software changes may be necessary. Consult the DM6467 documentation for operational details.

Functionally, on both devices, the default pin multiplexing configuration is determined by the state of various input pins at reset, and the reset state of various register bits. Following reset, the pin multiplexing configuration can be modified through software using two dedicated memory-mapped registers: Pin Multiplexing Control 0 Register (PINMUX0) and Pin Multiplexing Control 1 Register (PINMUX1). Writing to these two registers can be used to modify the pin multiplexing configuration to suit a wide variety of system applications. Note, however, that since pin-out and pin multiplexing configurations are different on these two devices, bit assignments and programming of the PINMUX0 and PINMUX1 registers on these two devices is different.

The following peripherals have multiplexed pins on the DM6467: VPIF, TSIF0, TSIF1, clock recovery generator (CRGEN0, CRGEN1), EMIFA, PCI, HPI, ATA, PWM0, PWM1, UART0, UART1, UART2, Audio Clock Selector, the USB USB_DRVVBUS pin, and GPIO.

For detailed information regarding pin multiplexing and its control on the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403) and the device-specific user's guides for the specific peripherals being used.

10 Power Supplies

The DM6446 and the DM6467 utilize multiple power supplies to maximize flexibility, performance, and minimize power dissipation, as well as to adhere to industry standards for various external interfaces.

The DM6446 device utilizes a 1.2 V supply for the DSP and ARM core CPUs and internal logic, and 3.3 V and 1.8 V power supply for its I/O pins. On the DM6446, the 1.8 V power supply is used by all of the I/O circuitry except the EMAC, MDIO, MMC, SDIO interfaces, and GPIOV33 [16:0]; The EMAC, MDIO, MMC, SDIO interfaces, and GPIOV33 [16:0] utilize the 3.3 V power supply.

The DM6446 device utilizes a 1.2 V supply for the DSP and ARM core CPUs and internal logic, and 3.3 V and 1.8 V power supply for its I/O pins. On the DM6446, the 1.8 V power supply is used by all of the I/O circuitry except the EMAC, MDIO, MMC, SDIO interfaces, and GPIOV33 [16:0]. The EMAC, MDIO, MMC, SDIO interfaces and the GPIOV33 [16:0] utilize the 3.3 V power supply. The DM6467 utilizes a 3.3 V supply for its I/O pins, and either a 1.2 V core supply for 594 MHz or 729 MHz operation or a 1.05 V core supply for 594 MHz operation only. Additionally, the DM6467 also requires a 1.8 V supply for the DDR2 interface, and for the device PLLs. Table 28 summarizes the power supply requirements for the DM6446 and the DM6467.

Table 28. Power Supply Requirements at Reset

Supply		DM6446	DM6467
Core	Voltage	1.2 V (all)	1.2 V (594/729 MHz) , 1.05 (594 MHz)
I/O 1	Voltage	3.3 V	3.3 V
I/O 2	Voltage	1.8 V	1.8 V

For detailed information regarding power supply requirements on the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403).

11 Package and Pin Count Comparisons

The DM6446 and the DM6467 are provided in cost-efficient, high-density BGA packages. The DM6446 device has a 361-pin ZWT package, while the DM6467 device has a 529-pin ZUT package. Since the two devices have different pin-outs, the pin connections and locations are different between the two devices; therefore, PC board layout and signal connection modifications are necessary when migrating from a DM6446 to a DM6467 device. Table 29 shows a comparison of the packages and pin counts for the DM6446 and the DM6467.

Table 29. DM6446/DM6467 Package and Pin Count

Characteristic	DM6446	DM6467
Designator	361 pin ZWT (Pb-free)	529 pin ZUT (Pb-Free)
Ball Pitch	0.8 mm	0.8 mm
Dimensions	16 x 16 mm	19 x 19 mm
Maximum Case Temperature	85°C	85°C -40°C - 105°C (A version)

For detailed information regarding pin-out and mechanical dimensions of the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip* (SPRS403).

12 References

- *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403)
- *TMS32064x+ DSP Cache User's Guide* (SPRU862)
- *TMS320DM646x DMSoC Video Port Interface (VPIF) User's Guide* (SPRUER9)
- *TMS320DM646x DMSoC Video Data Conversion Engine (VDCE) User's Guide* (SPRUEQ9)
- *TMS320DM646x DMSoC Transport Stream Interface (TSIF) Module User's Guide* (SPRUEQ2)
- *TMS320DM646x DMSoC DDR2 Memory Controller User's Guide* (SPRUEQ4)
- *TMS320DM646x DMSoC Asynchronous External Memory Interface (EMIF) User's Guide* (SPRUEQ7)
- *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA3) Controller User's Guide* (SPRUEQ5)
- *TMS320DM646x DMSoC Peripheral Component Interconnect (PCI) User's Guide* (SPRUER2)
- *TMS320DM646x DMSoC Multi-channel Audio Serial Port (McASP) User's Guide* (SPRUER1)
- *TMS320DM646x DMSoC Serial Peripheral Interface (SPI) User's Guide* (SPRUER4)
- *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9)
- *TMS320DM646x DMSoC Universal Asynchronous Receiver/Transmitter (UART) User's Guide* (SPRUER6)
- *TMS320DM646x DMSoC 64-Bit Timer User's Guide* (SPRUER5)
- *TMS320646x DMSoC Ethernet Media Access Controller (EMAC)/ Management Data Input/Output (MDIO) Module User's Guide* (SPRUEQ6)
- *TMS320DM646x DMSoC Universal Serial Bus (USB) Controller User's Guide* (SPRUER7)
- *TMS320DM646x DMSoC ATA Controller User's Guide* (SPRUEQ3)
- *TMS320DM646x DMSoC Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUER0)
- *TMS320DM646x DMSoC VLYNQ Port User's Guide* (SPRUER8)
- *TMS320DM646x DMSoC Host Port Interface (HPI) User's Guide* (SPRUES1)
- *TMS320DM646x DMSoC Pulse-Width Modulators (PWM) User's Guide* (SPRUER3)
- *TMS320DM646x DMSoC General-Purpose Input/Output (GPIO) User's Guide* (SPRUEQ8)
- *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8)
- *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871)
- *Using the TMS320DM6467 DMSoC Bootloader* (SPRAAS0)

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