Application Report
SPRAAV0A–July 2008

Understanding TI's PCB Routing Rule-Based DDR Timing Specification

Mike Shust and Jeffrey Cobb

ABSTRACT

This application report motivates the way the DDR high-speed timing requirements are now going to be communicated to system designers. The traditional method of using data sheet parameters and simulation models is tedious. The system designer uses this information to evaluate whether timing specifications are met and can be expected to operate reliably.

Ultimately, the real question the hardware designer wants answered is "How do I hook it up?" The method used here is different: TI solves the system timing problem once, and then a solution is communicated via direct PCB routing rules. This approach is particularly well suited to the embedded JEDEC DDR memory interface because of the naturally constrained system solution set and industry standard components.

Contents

1 Classical High-Speed Design Flow

The classical high-speed design flow is a complex, labor intensive affair. It requires personnel with a wide skill set and comprehensive simulation tools. It requires the silicon manufacturer to supply lengthy timing data and accurate simulation models that are tedious to develop and maintain.

In just about each and every system, the PCB must be designed from scratch. Designing the PCB for a high-speed peripheral involves the following tasks:

- Determine the bus peripherals
- Obtain the device data sheets
- Obtain simulation models
- Obtain test load models
- Simulate the test load
- Design the preliminary bus topology/stackup
- Run simulations
- Evaluate the simulations for signal integrity and timings
- Design the PCB

- Run simulations
- Evaluate the simulations for signal integrity and timings
- Test for EMI compliance
- Iterate, as necessary

The iterative nature of the process is a particular challenge. Highly experienced high-speed designers can usually limit the number of iterations, but less experienced engineers usually go through several iterations to satisfy all the design requirements. In many cases, the newer engineers are the ones involved with PCB design as the more experienced personnel are usually tasked with additional responsibilities beyond product design.

Designing for electromagnetic interference (EMI) compliance is particularly troublesome as simulation for EMI is not as accurate as it is for flight times and signal integrity. Many times, EMI compliance only results after PCB spins.

2 The Perils of Simulation

Proper simulation of a high-speed DDR interface is not a trivial task. Accurate simulation is a laborious and tedious process. Errors creep in from inaccurate models, bugs in tools, using incorrect environmental conditions, and errors in collating the large amount of data generated by a full up PCB simulation.

Traditional timing specifications consist of timing data that is assured to a test load. One of the steps required in PCB design is translating the data sheet from the test load to the actual PCB. Therefore, the system designer must spend time and resources simulating the silicon manufacturer's test load.

DDR memory requires more simulation accuracy than earlier technologies. Traditional simulation corners are defined as strong (fast) and weak (slow). The strong corner is strong silicon process, high voltage, and low temp. The weak corner is weak silicon process, low voltage, and high temp. The DDR interface is source synchronous, therefore, the clock for any data transfer is sourced from the same device that is providing the data. The result is a horse race between the clock and each of the data bits, making it possible for the strong or the weak corner to be the limiting factor on timing margin.

One way to be more accurate is to use appropriate environmental corners. Weak and strong are not sufficient – one cannot assume a weak input/output (I/O) buffer and strong I/O buffer exist at the same time on a PCB. It is not realistic to expect that the devices at one end of a bus will be at high voltage, low temp (*strong*), while at the other end, the devices will be at low voltage, high temp (*weak*). The assumption often leads to a failure to close timings.

What is needed are additional simulation corners, such as not so strong and not so weak. Not so strong is a weak silicon buffer at the environmentally strong corner of high voltage and low temp. Not so weak is a strong silicon buffer at the environmentally weak corner of low voltage and high temp. I/O buffer models, such as the I/O Buffer Information Specification (IBIS), have no facility for such corners [1]. IBIS and other simulation platforms can be coerced into modeling these corners, but the process is awkward at best.

Many smaller companies do not have the resources to perform full-up simulation; tools and personnel are expensive.

3 Real World Results of System Designer Simulation

Regardless of the simulation platform used, utilizing the results still requires a very skilled individual or team. In practice, the response of a system designer to a simulation result depends on whether the result is *positive* or *negative*.

A *positive* result is one in which the simulation says the system will work. There is a tendency to simply believe the result because it looks good and people are busy. Confirmation of simulation results is a very monotonous process; therefore, if things look good, they may be, or it might be blissful ignorance.

A *negative* result is one in which the simulation indicates a problem. This is usually not ignored and results with the system designer contacting the silicon manufacturer to ask why his part will not work in his system. Many times a negative result is created when an inexperienced person applies the models in error. The resolution is usually a time consuming process in which much time is spent just educating the designer. This designer education may be a great academic exercise, but don't forget that in the end, the system designer's employer wants to ship their product.

Another particularly nasty *negative* result is one which reflects that the system designer's attempt was to design an inappropriate application. The customer has now gone through significant time and effort only to find out their grand idea will not work. This can occur because the parameters of what is realistic and what is not are often buried in the timing specification and timing models.

Often, the best way to solve this problem is to avoid system design simulations altogether. The semiconductor manufacturer already uses extensive circuit simulation. Circuit simulation is an integral part to modern semiconductor design. However, there is potential to eliminate the simulation need for the PCB system designer if the right choices are made in the system specification. With these choices, it is possible to communicate the system timing specification without simulation models or timing numbers.

The concept is simple: why have each system designer reinvent the wheel when the silicon manufacturer can do it once?

4 Advantages to Specifying Timing Specifications via PCB Routing Rules

There are many benefits to using PCB routing rules as a timing specification.

- There is no need to obtain or use simulation models or simulation tools
- There is no need to design the PCB topology
- The number of PCB design iterations is dramatically reduced or eliminated
- TI can provide better support, since customers are following the same rules
- The critical PCB design parameters are ready for review at a PCB shop at the beginning of a project.
- Leverages knowledge learned from hundreds of working customer board designs which were based on TI's DDR recommendations

This new approach does not enable a completely inexperienced person to design a high-speed PCB; it is intended to communicate the information required to an experienced high-speed designer or to a less experienced team supervised by a high-speed experienced designer. The need for the experienced designer is to ensure that good high-speed PCB design practices are followed. The assumption of good high-speed PCB design rules allows the minutia of high-speed design practice to be left out of the specification, as brevity is a key feature to the approach.

5 Solutions to High-Speed Design Issues

High-speed PCB design involves controlling the following tasks:

- Flight time delay and skew
- Signal integrity and impedance matching
- Crosstalk
- Power supply bypassing
- EMI

In the classical high-speed flow, timing specifications and simulation modeling are performed to determine constraints required for the tasks listed above. In this case, Texas Instruments has evaluated the simulations and timing specifications and communicated the rules for these tasks directly to PCB designers. The next sections describe the ways these items can be constrained by generic PCB rules.

5.1 Flight Delay and Skew

The fundamental high-speed PCB issues are flight time delay and skews. The overall constraint for this is the placement of the components. The maximum placement refers to the placement in which the distances between the devices are the furthest permitted. Controlling the maximum placement of devices, combined with the assumption that good practices are followed, limits maximum trace delay to about the longest Manhattan distance of the signals contained in a clock domain. The reason it is the longest Manhattan distance is due to skew matching requirements: all of the shorter nets in a clock domain must be lengthened to skew match to the longest one. Therefore, flight time delay and flight time delay skew are controlled by the maximum placement and routing rules that constrain the matching of the trace lengths.

5.2 Signal Integrity and Impedance Matching

Signal integrity refers to controlling overshoot, ring back, and transition edges. As described in Section 5.1, the placement controls the maximum trace lengths. Given a constrained length, one can control signal integrity by controlling the PCB trace topology of the various parts of an interface. Included in this topology are any terminations. It is quite possible to make these terminations optional, if not for EMI considerations discussed later.

Effective signal integrity control on high-speed designs requires that the impedance of the PCB traces be controlled. Trace impedance is governed by the trace width as well as the thickness and dielectric constant of the PCB insulating material (usually FR-4). Fortunately for the PCB designer, this aspect can often be left to the PCB fabrication contractor by specifying the desired single ended impedance for the PCB traces.

Differential impedance can also be handled this way, however, implementation is a little trickier because the spacing between the differential traces influences differential impedance as well. Proper differential impedance is ensured via cooperation between the PCB layout designer and the PCB fabrication contractor.

Therefore, signal integrity is controlled by the allowed PCB signal trace topology. Termination schemes are considered part of that topology. Indirectly, stackup and trace widths control signal integrity as well by controlling impedance mismatch.

5.3 Crosstalk

Crosstalk is fundamentally controlled by the PCB stackup and minimum trace spacing. While improvements have been made, good crosstalk simulation can be quite difficult. The best approach to avoiding a crosstalk problem is to ensure all the signals have high-quality signal return paths and to spread the signal traces out.

Control of current return paths, one of the large contributors to crosstalk, can be done in the PCB stackup. Each signal routing layer should have an adjacent full ground plane to provide the shortest return current path.

The other aspect of crosstalk control is signal separation. It is well known that spreading signal traces out beyond the PCB minimum spacing dramatically lowers crosstalk to the adjacent signal [5]. The minimum separation is purely a mechanical specification controlled by the PCB technology used to manufacture the board. The PCB technology is chosen such that the densest circuitry can be routed (usually BGAs); therefore, some minimum spaced signal routing must occur near the dense devices. Since the amount of coupling between two parallel traces is also dependant on the length for which they are parallel, it is advantageous to spread these traces out wherever possible. Spacing them at two to three times the minimum trace spacing results in a very sizable reduction in crosstalk.

Crosstalk is controlled by the stackup, which provides quality ground return paths and trace spacing rules, which spread the signals out on the PCB. Typically, there is a provision in the specification that allows for the relaxation of trace spacing rules near dense component escapes.

5.4 Power Supply Bypassing

Precise power supply bypassing is essential for a properly functioning high-speed PCB. It is fundamental to control the power supply high-frequency impedance parameter which means controlling power supply inductance. Power supply high-frequency impedance is beaten down by utilizing many physically small capacitors connected between the power and ground planes. Using many capacitors, rather than one large one, results in their parasitic inductances being placed in parallel, thereby, reduced. The parasitic inductance of a capacitor is dependant upon its size.

The practical limit for the number of bypass capacitors is the geography of the PCB. The bypass capacitors need to be placed very close to the device they are bypassing. Once the semiconductor devices are chosen, you can determine from the placement how many capacitors will fit. The high-speed specification communicates how many are required and gives guidelines for placement. It also provides rules about how the capacitors are connected to the planes. Wrong via choices can increase parasitic inductance significantly.

It is best to use the largest capacitance value easily obtainable in the smallest package. However, differing values can help when power supply EMI issues are created due to power supply resonances. Fortunately, it is usually easy to tune these values after prototypes are built during EMI testing. Adding bypass capacitance mounting locations after PCB manufacture is almost impossible without a PCB spin due to the inductance issue, therefore, placing as many as possible is recommended.

5.5 EMI

EMI simulation can be particularly difficult, and as in crosstalk control, it is a problem best avoided by following good high-speed design practice. EMI is also addressed in the same way as crosstalk – good signal return paths limit loop area which limits crosstalk and EMI.

Ringing and overshoot aggravate EMI as well as crosstalk. Ringing in high-speed systems occurs at the natural frequency of the system. These higher frequencies can propagate more easily. Termination that reduces this ringing also reduces EMI, but the terminations comes at a cost of increased BOM count and PCB space.

The cost-benefit equation of EMI versus termination has different results for different silicon customers. Laying out the benefits and the risks of termination options and letting the designer make the choice is a reasonable alternative.

For example, leaving optional terminations off a design may result in an EMI certification failure. Addressing this may require adding terminations. However, a terminator-less design will likely not have room to add the needed components. This could mean an entire design has to be redone almost from scratch. Therefore, the trade off is a smaller, lower parts count design versus a risk of failing EMI.

A middle of the road approach is to design with terminators and populate them with zero Ohm resistors. The design is then checked for EMI compliance and only those terminations that are required are added back. It is easy to remove the zero Ohm terminators in a board spin.

Customers for which board space is at such a premium that they must do without terminators need to place room in their schedules for board spins in case of EMI issues.

The final component to EMI control is providing a reference design that follows the PCB specification and passes EMI compliance testing. It is less risky making small incremental changes from a design that is known to pass EMI than to design something new from scratch.

6 Application

The high-speed DDR design issues outlined in Section 2 have been solved by TI and are included in the data sheet or application report for the individual devices. The PCB design rules control issues such as flight time delay, signal integrity and impedance matching, skew matching, crosstalk, power supply bypassing, and EMI.

Flight delay is addressed in the Placement section of the data sheet. Specifications for the device orientation and maximum distances keep the flight delay within acceptable limits. It is also important to note that only maximum distances are given, which allows for smaller designs if desired.

The issues of signal integrity and impedance matching are controlled in the routing and topology sections of the data sheet. Since the trace lengths have been constrained by the placement, the topology controls the signal integrity. Topologies for routing VREF, clock and address control, DQS and DQ, and DQGATE (if used) are all specified in those sections. Termination schemes are also provided in the DDR Signal Termination section, although they are not required outside of EMI considerations.

Skew matching is also controlled in the Routing Rules section of the data sheet. The maximum trace delay is limited to the longest Manhattan distance of the signals in a clock domain. The rest of the signals in the domain have to be lengthened.

The most important component in controlling crosstalk is providing good return current paths, and these are controlled by the PCB stackup. The PCB Stackup section in the data sheet provides a minimum six layer board stackup that effectively minimizes signal crosstalk between layers. By requiring ground reference planes adjacent to every DDR routing layer, the specification provides a path for return currents. While the data sheet shows only a minimum six layer stackup, more layers can be added to accommodate larger systems, provided that the stackup specification is followed.

Power supply bypassing specifications are detailed in the Bypass Capacitor sections of the data sheet. The tables give the minimum number of bypass capacitors needed to bypass the specific devices as well as the minimum amount of capacitance needed. In addition, for the high-speed bypass capacitors, maximum distances from the capacitors to the devices are given. These values, along with rules restricting via sharing, work to control the power supply inductance, which controls the power supply high-frequency impedance.

EMI is treated several ways. The DDR Signal Termination section addresses how to terminate the various net classes to reduce ringing, a primary source of EMI. The PCB Stackup section also addresses EMI by reducing crosstalk via return current paths as mentioned earlier. The TI evaluation module (EVM) provides a design example that passes EMI tests.

7 Summary

The alternative method for specifying DDR high-speed timing requirements explained here has some distinct advantages over the traditional methods:

- The system designer does not have to run simulations nor have access to simulation tools.
- The silicon manufacturer does not have to provide and support silicon models.
- The system designer does not have to close timing.
- The silicon manufacturer does not have to provide discrete timing data nor test loads.
- The system designer knows the PCB challenges up front.
- The silicon manufacture can target their device for a very specific PCB use condition.
- The concise specification is easy for the system designer to follow.
- The concise specification is easy for the silicon manufacturer to verify.

8 Frequently Asked Questions

What background is expected of the PCB system designer?

While the goal of the DDR specification in the data sheet is to make system implementation easier for the customer by providing the system solution, it is still expected that the PCB design work be supervised by a knowledgeable high-speed PCB designer using established high-speed design rules. Avoid ground plane cuts, if at all possible, as they are tricky to do correctly. Evaluate crosstalk and EMI impacts due to PCB design as the design progresses; it can be difficult to go back and fix issues later. Thorough planning will aid in the design cycle.

How is DDR package size determined?

Use caution when determining the DDR component keep out as the JEDEC specification generally calls out only maximums for package sizing. Some manufacturers' JEDEC compliant DDR parts are narrower than these maximums and this can cause assembly interference issues if the part is later changed to another manufacturer with a wider package width. It is best to follow MO-207J and the manufacturer's documentation to determine overall package sizing. Pay close attention to the limits allowed by MO-207J, as these will likely be more restrictive than a specific manufacturer's part specification. This allows physical placement compatibility with all JEDEC DDR parts supported by this device.

Is the DDR design for embedded applications similar to designing for typical PC applications?

There are some subtle differences between the embedded DDR application and the typical PC motherboard/DDR DIMM application. The embedded DDR interface does not use stub series termination (the SST in SSTL). Stub series terminators are parallel terminators and they are not used in this case due to their high power consumption. Consequently, the termination voltage, Vtt, is also not used nor is it required in this case.

Should signal terminations be implemented?

Terminations on the PCB allow the DDR signals to be tuned to meet EMI certification requirements. A PCB which fails EMI certification without terminations will likely have to be re-spun in order to address the EMI shortcomings. It can take multiple PCB spins to correct EMI issues. Note that re-spinning a dense non-terminated PCB layout to include terminators can be a very difficult effort because physical room must be made for the terminations. This means an entire PCB design may have to be redone. It is much easier to remove terminations rather than adding them after the PCB has been found to fail EMI.

Customers who are sensitive to the cost/schedule issues with respect to EMI may wish to include terminations on their boards even though they plan not to have terminations on the final product. This way, the terminations can easily be replaced with zero Ohm resistors and checked for EMI compliance. If the PCB fails EMI, it is then straightforward to install the necessary terminations without re-spinning the PCB. Once the termination scheme has been verified to pass EMI, the remaining zero Ohm terminations can be carefully removed from the PCB layout in a single PCB design spin.

Termination resistors can be either discrete resistors or resistor packs and they are placed in between the DDR memories and the device. The VREF divider resistors are placed somewhere in between the DDR devices and the device.

How can the PCB area be minimized?

The maximum placement and minimum PCB stackup uses the lowest cost PCB technology and generally results in the lowest unit cost PCB at the penalty of the largest footprint for the DDR interface. Customers need to evaluate the cost/benefit tradeoffs of smaller feature sizes and additional signal layers for their systems. Note that the minimum feature size and stackup may be limited by other circuitry on the PCB. Using more advanced PCB technology will allow reductions of the PCB footprint of the DDR interface.

What are the recommended PCB feature sizes?

The minimum PCB feature sizes referenced in the data sheets are the largest that can be accommodated in order to physically route the PCB due to the size of the BGA packages. Smaller feature sizes can also be used as well to improve PCB density, as long as all routing rules are followed.

It is also a good idea to maximize the size of the vias used for bypass capacitors and power pins. This is done to minimize via inductance. It is the via and bypass capacitor stray inductance that limits the performance of the bypass capacitors. Use care to ensure that vias are not sized so large as to cut off a portion of a plane.

What are the recommended BGA feature sizes?

PCB BGA feature size selection is critical for PCB yield and reliability. Generally, it is best if the pad on the PCB has the same area as the pad on the BGA package. Before layout begins, the device manufacturer, PCB fabricator, and PCB assembler should be consulted with respect to BGA pad stacks and other critical BGA PCB mechanical details. As a general warning, the recommended BGA pad size is generally not equal to the BGA ball size.

9 References

1. I/O Buffer Information Specification (IBIS), Version 4.1, ANSI/EIA-656-A, January 30, 2004
2. *Implementing DDR2 PCB Layout on the TMS320C6455/TMS320C6454* (SPRAAA7)
3. *Implementing Serial Rapid I/O PCB Layout on a TMS320C6455 Hardware Design* (SPRAAA8)
4. *High-Speed Digital Design, A Handbook of Black Magic*, Howard W. Johnson and Martin Graham, Upper Saddle River, NJ: Prentice Hall PTR, pp. 190-1, 1993
5. *High-Speed Digital Design, A Handbook of Black Magic*, Howard W. Johnson and Martin Graham, Upper Saddle River, NJ: Prentice Hall PTR, pp. 191-4, 1993
6. *Implementing DDR2 PCB Layout on the TMS320DM644x DMSoC* (SPRAAC5)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265