Migrating From TMS320DM35x to TMS320DM36x Devices

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ABSTRACT

For purposes of comparison, this application report describes the key features of the TMS320DM36x (DM36x) and the TMS320DM35x (DM35x) digital media processors.

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1 Introduction

Some of the device features presented in this document are not necessarily available to every customers or not supported by TI. An NDA might be required to get access to some detailed information

Migration issues from the DM35x to the DM36x are indicated with the following symbols. These symbols are included at the beginning of each section.

S Means software modification is required.

H Means hardware modification is required.

D Means the DM35x and DM36x devices are different (usually due to added features or enhancements on the DM36x device) but no modification is necessary for migration (i.e., different but compatible).

DM35x:

Throughout the rest of this document, DM35x refers to DM350 and DM355. Unless otherwise noted, the information contained in the DM35x data manuals (see Section 9) should be considered Production Data defined as follows:

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

DM36x:

Unless otherwise noted the information contained in the DM36x data sheet (see Section 9) should be considered Production Data defined as follows:

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

2 Differences Between DM36x and DM35x

2.1 System

- 13mm × 13mm device package
- Clock speeds (refer to the device-specific data manual for details)
  - DM35x:
    - External clock input or crystal (24 or 36 MHz)
    - ARM: 135, 216 and 270 MHz
    - ARM and co-processors clocks synchronized
  - DM36x:
    - External clock input or crystal (19.2 MHz, 24 MHz, 27 MHz or 36 MHz)
    - ARM: 216, 270 & 300 MHz. DM368 also supports 432 MHz
    - ARM and co-processors clocks independent

2.2 ARM

- On-chip 297 MHz ARM926EJ-S 32 bit RISC microprocessor
- Increased on-chip ROM to 16 Kbytes

2.3 Co-Processors

The DM35x and DM36x devices have a Motion and still JPEG coprocessor (MJCP). The DM36x also has a HD Video and Imaging coprocessor. Those coprocessors allow low power, low MIPS codecs with the flexibility to select the right video codec for most applications. The independent coprocessors (HDVICP and MJCP) offload all compression and decompression needs from the main ARM core, leaving room for the application and user interface. TI provides free codecs optimized for those accelerators.

- 243 MHz programmable 2 × 4MAC SIMD image processing engine (iMX) for programmable image processing, with 8-way parallel motion estimation accelerator
- 121 MHz sequencer, a 16-bit microprocessor optimized for synchronization and control of coprocessor and DMA. Sequencer is equipped with 4 Kbytes of program and 1 Kbytes of data memory
- 20 KBytes (5x4 Kbytes) of shared image processing buffer for iMX, sequencer, compression engine and DMA to collaborate.
- Significantly enhanced co-processor subsystem for image and video processing
- Hardwired video accelerator for H.264 and WMV-9/VC-1, including ARM968
- There is an over-drive mode that achieves >300 MHz on the ARM968
- Added noise filter hardware module in order to reduce/remove noise in images

2.4 Video Processing Subsystem (VPSS)

- Significantly enhanced hardware image processing and resizing capabilities via video processing front end (VPFE)
- Updated on-screen display (OSD) and VENC
- VPFE and video processing back end (VPBE) digital I/O's operate at 3.3 V or 1.8 V
- Three channels digital analog converter (DAC)

3 Peripheral Differences [H D]

Table 1 shows the peripheral differences between the DM36x and the DM35x devices.

Table 1. Peripheral Differences

Peripheral	DM36x	DM35x
Microprocessor Unit (MPU)	ARM926EJS_Z8	ARM926EJS_Z8
MPU L1 Cache	16 KBytes I Cache, 8 KBytes D Cache	16 KBytes I Cache, 8 KBytes D Cache
MPU ROM	16 KBytes	8 Kbytes
MPU TCM	32 KBytes	32 Kbytes
VPFE	Yes	Yes
VPBE	Yes	Yes
Power Management and Real-Time-Clock Sub-System (PRTCSS)	Yes	No
Low Core Voltage Mode	Yes	No
Direct Memory Access (DMA)	EDMA3.0	EDMA3.0
External Memory Interface (EMI)	DDR2-16b, 216 MHz clock overdrive mode up to 243 MHz mDDR: 16b, 168 MHz	DDR2-16b, 171 MHz clock overdrive mode up to 216 MHz mDDR: 16b, 133 MHz
Multimedia Card(MMC)/Secure Digital(SD)(SDIO)	2x	2x
AEMIF 16 bit	1x	1x
Multi-Channel Buffered Serial Port (McBSP)	1x	2x
Universal Asynchronous Receiver/Transmitter (UART)	2x	3x
Serial Peripheral Interface (SPI)	5x	3x
Inter-Integrated Circuit (I2C)	1x	1x
Analog-to-Digital Converter (ADC)	Yes - 6 channel	No

Table 1. Peripheral Differences (continued)

Peripheral	DM36x	DM35x
Key Scan	Yes – 4x4/5x3 Marix	No
Voice Codecs	1x	No
Coprocessor	1x	1x
Timers	8x32-bit timer + 1xWDT	6x32-bit timer + 1xWDT
Universal Host Port Interface (UHPI)	1x	No
Ethernet Media Access Controller (EMAC)	1x	No
HD-VICP	1x	No
Real Time Out (RTO)	4x	4x
Pulse Width Modulator (PWM)	4x	4x
Universal Serial Bus (USB)	1x	1x
Power Management and Real-Time-Clock Sub-System (PRTCSS)	Yes - 1x	No

3.1 Ethernet MAC (EMAC) [H]

The EMAC module has been added to the DM36x device and is used to move data between the DM36x device and another host connected to the same network, in compliance with the Ethernet protocol. It provides 100/10 Mbps operation using the MII operation in full duplex and half duplex mode.

The EMAC controls the flow of packet data from the system to the PHY. The management data input/output (MDIO) module controls PHY configuration and status monitoring.

The EMAC module is multiplexed with general-purpose input/output (GPIO) peripherals.

In addition, the DM36x can boot over the EMAC subsystem. For more details, see Section 8 of this document.

3.2 External Memory Interface (EMI) [H]

3.2.1 System Memory

The DM36x utilizes standard DDR2-mDDR as its main system memory. The DDR2 memory controller interface can be clocked up to 243 MHz, yielding a data frequency of 486 MHz. The interface bus is 16-bits wide, providing a theoretical data rate of 972 MBps. There is also a second memory interface that allows connectivity to both synchronous and asynchronous interfaces.

For more information regarding tolerances that must be adhered to in order to assure correct DDR2 operation, see *Implementing DDR2/mDDR PCB Layout on the TMS320 DMSoC* (SPRAAR3).

3.2.2 Secondary Memory [D]

The DM36x provides a secondary external memory interface (EMIFA) which can be operated either synchronously or asynchronously, allowing connectivity to various devices such as NOR flash, FGPAs, CPLDs, or other such devices. The interface is 16-bits wide and can be clocked up to 60 MHz, providing a theoretical throughput of 120 MBps.

The secondary interface is used for booting NOR/NAND Flash. For more details, see Section 8 of this document.

3.3 Universal Host Port Interface (UHPI) [H]

A universal host port interface peripheral has been added to the DM36x device. The HPI module used in the DM36x device is similar to the HPI module in the TMS320DM6467 system-on-chip (SoC). The HPI can be used for general-purpose communications and control in various applications. On the DM36x device, this peripheral is multiplexed with the EMIF peripheral and uses 16-bit EMIF data bus in multiplexed address/data mode only.

It is possible to boot the DM36x over the UHPI peripheral. For more details, see Section 8 of this document.

3.4 Video Processing Front-End (VPFE) [H]

The video processing front-end (VPFE) contains interface to CCD/CMOS sensors (ISIF), and provides parameterizable image processing for still capture, video capture, and live preview. Various resolutions of image resizing is done in hardware for digital zoom and image/video capture at speeds of up to 100Mpix/sec.

Table 2 compares the features of the VPFE for DM36x and DM35x.

Table 2. VPFE Differences for DM36x and DM35x

Feature	DM35x	DM36x
CCDC	CCDC includes: Data formatter on input to handle VGA movie mode sensors Modified control interface for VGA movie mode to make processing more extensible Operation at up to 75/100 MHz with external clock Supports up to 14-bit AFE Fault pixel correction from internal table Lens shading correction and color space conversion functions DM355 CCDC is the same as the DM350 CCDC	CCDC function has been moved to ISIF module
Resizer	Resizer functionality is part of IPIPE	Upsampling has equivalent processing of std bi-cubic interpolation Supports upsampling on the fly Maximum output width of 2176 pixels for image-A and 1088 for image-B Resizing of either YUV422/YUV420 packed data (16-bits) or color separate data Up/down sampling ratios: 256/N, with N ranging from 32-4096
LDC	Not in DM35x	Radius-to-magnification factor table Correct barrel distortion Configure center point and horizontal/vertical adjustment Multiply mask in 8x8 down sampled format 8-bit mask 16-bit data input/ouput Support chromatic aberration in Bayer domain Support distortion correction in YUYV domain
H3A	**DM350 Hardware 3A:** AE AWB AF (horizontal, green only) Can process data from either CCDC or DDR2 Supports up to 192 windows **DM355 Hardware 3A:** Support for up to 36 horizontal windows Support for up to 128 vertical windows	Similar to DM355 Support for up to 36 horizontal windows Support for up to 128 vertical windows

Table 2. VPFE Differences for DM36x and DM35x (continued)

Feature	DM35x	DM36x
IPIPE	Image Pipe includes: Can process data from either CCDC or DDR2 2D noise filter, 2D profiler, 2D edge enhance White balance module CFA interpolation RGB2YCbCr conversion YUV422 conversion Chroma suppression Histogram (up to 4 areas, 256 bins) Boxcar function Boundary signal calculator Maximum output width of 1280 pixels with simple 2,4,8 pixel averaging added since Resizer is no longer integrated Dark frame capture (to DDR2) Dark frame subtraction (from DDR2) Supports either dark frame subtract or lens shading compensation, but not both simultaneously Programmable gamma correction table (512 entries for each color) Programmable 2D noise filter Programmable 5x5 CFA interpolation with separate CFA filters depending on directional H/V gradients	Similar to DM35x: Resizer function has been moved to Resizer module Programmable 4x4 CFA interpolation with separate CFA filters depending on directional H/V gradients Lens shading compensation (each pixel multiplied by 8-bit gain array and right shifted 0-7 bits) 2D prefilter is now called GIC (Green Imbalance Correction) Programmable 4x4 CFA interpolation with separate CFA filters depending on directional H/V gradients
HSSI	**This feature is supported in DM350** The high-speed serial imager interface (HSSI) provides a high-speed, low pin-count serial imager interface into the DM35x. Supports multiple input formats (YUV,RAW) Supports embedded Supports CRC Includes integrated Phy **This feature is not supported in DM355**	**This feature is not supported in DM36x**
CFALD	This is used to perform lens distortion correction and CFA multiply mask Correct barrel distortion Radius-to-magnification factor table Configure center point and horizontal/vertical adjustment Separate lookup table for each color for chromatic aberration Multiply mask in 8x8 down sampled format 8-bit mask 14-bit data input/ouput	This feature has been move to LDC

Table 2. VPFE Differences for DM36x and DM35x (continued)

Feature	DM35x	DM36x
ISIF	Not in DM35x There is no DM355 ISIF	Supports linearization (16 bit IN to 12 bit OUT) Data formatter on input to handle VGA movie mode sensors Can synchronize on externally provided HD/VD signals Supports progressive and interlaced scan sensors Modified control interface for VGA movie mode to make processing more extensible Operation at up to 120 MHz with external clock Fault pixel correction from internal table for vertical line defects

3.5 Video Processing Back-End (VPBE) [H]

The DM36x video processing back-end consists of VENC and OSD. The back-end provides OSD capability for graphical user interface (GUI), and interfaces to National Television System Committee (NTSC)/phase alternating line (PAL) video, digital LCD output (can interface with HDMI), or standard CCIR 601/656 output, as well as 720p/1080i analog output (HD DAC).

Table 3 compares the different features of the VPBE for DM36x and DM35x.

Table 3. VPBE Differences for DM36x and DM35x

Feature	DM35x	DM36x
VENC	Supports analog 480p/576p Supports 1 DAC for NTSC/PAL composite video Supports 720p (HDTV digital 74.25 MHz) support w/external VPBE clock Supports RGB666 output mode requires GIOs for extra data bits	Supports 720p/1080i analog HD Supports 3 channel DAC for NTSC/PAL composite video Supports RGB888 output mode requires GIOs for extra data bits
OSD	 OSD windows support bitmap, RGB565, GB888, and YUYV Transparent background color in RGB565, GB888, and YUYV window Additional expansion modes	Similar to DM35x with the following modifications: SDRAM interface address width changed from 24 to 27 bit SDRAM interface data width changed from 32 to 64 bit Bitmap blend factor through mode Input buffer size changed according to change in SDRAM data interface width (64-bit width) Supports YUV420 format

3.6 MJCP

The MJPEG / JPEG co-processor (MJCP) is available on all DM35x and DM36x devices. This hardware accelerator is a dedicated JPEG and MJPEG codec. The free codecs provided by TI for both platforms obfuscate the hardware differences from the programmers.

3.7 HD-Video and Imaging Co-Processor (HD-VICP) [H]

The HD video and imaging co-processor (HD VICP), is new to the DM36x device. The HD VICP is a dedicated multi-standard HD video encode/decode engine used for H.264 and WMV-9/VC-1. HD VICP also includes ARM968.

The DM36x HD-VICP is similar to the HD-VICP in the DM6467 SoC.

3.8 Key Scan [H]

The key scan module is new to the DM36x device. This module supports 4 × 4 or 5 × 3 key scan function.

This module support two scan modes:

- Channel interval mode
- Scan Interval mode

3.9 A/D Convertor (ADC) [H]

The ADC module is new to the DM36x device. The ADC supports the successive approximation type 10-bit A/D converter. In the DM36x device, the ADC module has six analog inputs selected for configurable analog input (from 1 to 6 inputs).

3.10 Voice Codecs [H]

The VOICE CODECs module is new to the DM36x device. The VOICE CODEC module includes the interface module that can access ADC/DAC data with internal first-in-first-out (FIFO) (read FIFO/write FIFO).

3.11 Power Management and Real-Time-Clock Sub-System (PRTCSS) [H]

The power management and real-time-clock sub-system (PRTCSS) is new to the DM36x devices. This block consists of power management and real-time-clock sub-system (PRTCSS) in the DM36x and the PRTC interface (PRTCIF). The PRTCSS is used for calendar applications and to manage the DM36x power supply. It has an independent power supply and can remain ON even while the rest of the DM36x's power supply is turned OFF; therefore, PRTCSS can be operated without supplying power to the whole device. PRTCSS has a real-time-clock, Timers, general-purpose-I/Os and a simple sequencer that can access the PRTCSS peripherals.

4 Power Supply Differences [H]

The core voltage of the DM36x is 1.2 V with ± 5% tolerance for normal mode and 1.35 V with ± 5% tolerance for overdrive mode. Table 4 shows the relationship between operating voltages and frequencies. The I/O voltage of the DM36x is 1.8 V and 3.3 V compared to 3.3 V ± 5% on the DM35x. The DDR peripheral require an additional supply rail (1.8 V ± 5% tolerance).

Table 4. Power Supplies for DM36x

	Power Supplies			
Device	**Core**	**I/O**	**DDR I/O**	**Maximum Frequency**
DM35x	1.3 V ± 5%	3.3 V ± 5%	1.8 V ± 5%	270 MHz
DM36x	1.2 V ± 5% 1.35 V ± 5%	1.8 V ± 5% and 3.3 V ± 5%	1.8 V ± 5%	270 MHz 432 MHz

5 Device Identification [H]

The DM36x device is a new product. The JTAG (BSDL) ID and Silicon revision ID are different than the DM35x device. Table 5 identifies the JTAG (BSDL) ID differences between the DM35x and the DM36x.

Table 5. JTAG (BSDL) ID for DM36x

	JTAG (BSDL) ID				
Device	**Memory Address**	**Variant**	**Part Number**	**Manufacturer**	**LSB**
DM36x	0x01C40028	0000	1011 1000 0011 1110	000 0001 0111	1
DM35x	0x01C4 0028	0000	1011 011100111 011	000 0000 1111	1

6 Package and Pins [H, D]

The DM36x and the DM35x devices use different mechanical packages, therefore, the physical dimensions and pinout of the packages are also different. Table 6 lists the variations between the DM36x and the DM35x devices.

Table 6. Package Differences Between DM36x and DM35x

Device	Package Characteristics			
	Size (mm)	Pitch (mm)	No. of Pins	Package Designator
DM36x	13x13 mm	0.65 mm	338	ZCE
DM350	12x12 mm 13x13 mm	0.5 mm 0.65mm	329	ZWK
DM355	13x13 mm	0.65mm	337	ZCE

7 PLL/CPU Clock [H]

The phase-locked loop (PLL) on the DM36x device is different from the one used on the DM35x. The DM36x incorporates two on-chip PLLs: one for device clock generation (including video encoder clock) and one for DDR and VPSS clock generation. The device also makes use of the PLL and reset controller module for controlling the PLLs and in generating the system clocks required by various modules.

In DM35x, clocks are derived by one crystal (24 MHz (typical) or 36 MHz), whereas, in DM36x, the system clock may be driven from either an external clock (CLKIN) or a crystal (MXI/MXO). Alternatively, a fundamental frequency crystal can be used which drives the on-chip oscillator to produce the internal clock OSCIN. On DM36x, these sources are merged onto a single pin (MXI). The nominal frequency of either the external crystal or oscillator is 19.2/24/27/36 MHz.

The DM36x PLL multiply modes are programmed through register accesses. The DM36x has more flexibility with clocks to modules from the PLL by using variable dividers in DM36x instead of fixed in DM35x.

8 Reset and Boot [H, D]

The reset controller for the DM36x has several enhancements that allow the application to control peripherals on an individual basis. Once the ARM comes out of Master Reset, the individual peripherals must be enabled through the reset controller.

The DM36x has additional bootmodes that are not available on the DM35x. Table 7 lists the available bootmodes and their associated description.

For more information regarding reset and boot mode, see *TMS320DM365 DMSoC DMP ARM Subsystem Reference Guide* (SPRUFG5).

Table 7. Description of Available Bootmodes on DM36x and DM35x

Device			
DM35x	DM36x	Boot Type	Description
X	X	Emulation	
	X	UHPI	This mode allows booting the device over the universal Host port interface.
X	X	AEMIF	This mode allows booting over the asynchronous interface. ARM pulls data from a memory device such as a NOR flash.
X	X	NAND	This mode starts downloading code from an NAND memory.
	X	SPI	This mode starts downloading code from an SPI EEPROM on CS0. The code must be stored in an AIS format.
X	X	UART	This mode must be booted using a 24-MHz clock for UART boot type. This forces the baud rate to 115200. The UART sends a BOOTME request to the UART peripheral and waits for a response along with code from a host processor
X	X	MMCSD	This mode starts downloading code from an MMC/SD Controller MMCSD0.
	X	USB	This mode must be booted using a 24-MHz clock.
	X	EMAC	This mode allows booting over the Ethernet. The Ethernet port starts out by sending a BOOTP request. Once acknowledged by a BOOTP server, the ARM can be booted.

9 References

- *TMS320DM365 Digital Media System-on-Chip (DMSoC) Data Manual* (SPRS457
- *TMS320DM355 Digital Media System-on-Chip (DMSoC) Data Manual* (SPRS463)
- *Implementing DDR2/mDDR PCB Layout on the TMS320 DMSoC* (SPRAAR3)
- *TMS320DM365 DMSoC DMP ARM Subsystem Reference Guide* (SPRUFG5)

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