Application Report
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TMS320x281x to TMS320x2833x or 2823x Migration Overview

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ABSTRACT

This application report describes differences between the Texas Instruments TMS320x281x and the TMS320x2833x and TMS320x2823x device families to assist in application migration. While the main focus of this document is migration from 281x to 2833x/2823x, you will also find this document useful if you are considering migrating in the reverse direction. Functions that are identical in both devices are not necessarily included. All efforts have been made to provide a comprehensive list of the differences between the two device groups in the 28x generation.

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1 Introduction

The TMS320x281x, TMS320x2833x, and TMS320x2823x devices are members of the C2000™ microcontroller family for use within embedded control applications. The TMS320x2833x and TMS320x2823x devices feature enhanced peripherals, a DMA module, and an external interface (XINTF) with 32-bit data bus capabilities. In addition, the 2833x includes the 28x plus floating-point-unit central processing unit (CPU). These new peripherals enable the firmware engineer to effectively solve challenging control problems.

For purposes of migration, these devices can be thought of in two groups:

- TMS320x281x
- TMS320x2833x and TMS320x2823x

As the focus of this document is to describe the differences between the two device groups, the descriptions are explained only to the extent of highlighting areas that require attention when moving an application from one device to the other. For a detailed description of features specific to each device, see the device-specific data manuals and user guides available on the TI website at http://www.ti.com. This application report does not cover the silicon exceptions or advisories that may be present on each device. Consult the following silicon errata for specific advisories and workarounds:

- *TMS320F2810\F2811\F2812\TMS320C2810\C2811\C2812 DSP Silicon Errata* (SPRZ193)
- *TMS320R2811 and TMS320R2812 DSP Silicon Errata* (SPRZ226)
- *TMS320F280x, TMS320C280x, and TMS320F2801x DSP Silicon Errata Silicon Errata* (SPRZ171)

Note: For information regarding any electrical specifications, always refer to the TMS data manual.

1.1 Abbreviations

The following abbreviations are used in this document:

- 281x: Refers to the TMS320x281x devices. For example, TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812, TMS320R2811 and TMS320R2812.
- 2833x: Refers to the TMS320x2833x devices. For example, TMS320F28335, TMS320F28334 and TMS320F28332.
- 2823x: Refers to the TMS320x2823x devices. For example, TMS328F28235, TMS320F28234 and TMS320F28232.
- C28x+FPU refers to the C28x™ plus floating-point unit.
- CCS refers to Code Composer Studio™ software.

For a full list of devices currently available within the 281x and 2833x/2823x families, see the TI website.

2 Central Processing Unit (CPU)

The 2833x devices are the first devices to include the C28x plus the floating-point unit CPU (C28x+FPU). C28x+FPU based controllers have the same 32-bit fixed-point architecture as TI's existing C28x DSCs, but also include a single-precision (32-bit) IEEE 754 floating-point unit (FPU). It is a very efficient C/C++ engine, enabling you to develop system control software and math algorithms using C/C++.

No changes have been made to the existing:

- C28x Instructions
- C28x Pipeline
- C28x Emulation
- Memory Bus Architecture

New instructions to support floating-point operations have been added as an extension to the standard C28x instruction set. This means code written for the C28x fixed-point CPU is 100% compatible with the C28x+FPU. The C28x+FPU latched overflow and underflow (LVF, LUF) flags are connected to the peripheral interrupt expansion (PIE) block. This makes debugging overflow and underflow issues much easier. For an introduction to the C28x+FPU, see the *C28x FPU Primer* (SPRAAN9) and the *TMS320C28x Digital Signal Controller Plus Floating-Point Unit* online training from the TI website.

The C28x+FPU architecture and instruction set are documented in the following two reference guides:

- *TMS320C28x DSP CPU and Instruction Set Reference Guide* (SPRU430). This document also applies to the C28x+FPU.
- *TMS320C28x Floating Point Unit and Instruction Set Reference Guide* (SPRUEO2). This is a supplement to the *TMS320C28x DSP CPU and Instruction Set Reference Guide* (SPRU430).

3 Development Tools

A new set of header files and peripheral examples are available for the 2833x and 2823x with the same structure as the 280x/2801x/2804x header files. For more information, see *C2833x/C2823x C/C++ Header Files and Peripheral Examples* (SPRC530). Since the peripherals on the 2833x and 2823x are identical, the header files are shared by the two devices. In the header file package, the examples have been duplicated with one set enabling the native floating point (2833x) and the other group setup to only generate fixed point code (2823x).

The C28x+FPU on the 2833x is supported with a patch to Code Composer Studio 3.3. Currently the FPU registers can be viewed within a Code Composer Studio watch window only. The 2833x GEL files include a function to automatically populate the watch window with the FPU registers. In future updates to Code Composer Studio, the FPU registers will be added to a register window. Current C2000 emulation pods work with the C28x+FPU.

The compiler, assembler, and linker must be V5.0 or greater to take advantage of the 2833x hardware FPU resources. As of this writing, the latest compiler is V5.2.1. Check the Code Composer Studio update advisor for future updates. When building for native floating point, you must use the correct run-time support library. When compiling with --float_support=fpu32, use the *C28x FAST RTS Library* (SPRC664) in combination with the standard rts2800_fpu32.lib or rts2800_fpu32_eh.lib supplied with the compiler.

Note: To get the best native floating-point performance for math routines on the 2833x, use the *C28x FPU Fast RTS Library* (SPRC664). The C28x Fast RTS is a collection of optimized floating-point math functions for C programmers of the C28x with floating-point unit. Designers of computationally intensive real-time applications can achieve execution speeds considerably faster than what are currently available without having to rewrite existing code. The functions listed in the features section are specifically optimized for the C28x + FPU controllers.

Note: To enable the compiler to generate native FPU instructions, you must tell it that you have a C28x device with a floating-point unit. To do this, use the following compiler switches:
-v28 --float_support=fpu32
In Code Composer Studio, the fpu32 switch is under the advanced compiler options.

You can not mix code built without the --float_support=fpu32 switch and code built with it because the compiler calling conventions changed for floating-point numbers. The linker will issue an error indicating the object files are not compatible If you try to mix the two. If you receive this error, first check that all libraries have been built with the same switch. In particular the runtime support library that comes with the compiler must be correct. Use the rts2800_fpu32.lib or rts2800_fpu32_eh.lib when compiling with --float_support=fpu32 .

3.1 Migrating From IQMath to Native Floating Point

If you want to convert a project written in the IQmath format to native floating point, the following steps need to be taken:

1. Select FLOAT_MATH in the IQmath header file. The header file converts all IQmath function calls to their floating point equivalent.
2. Convert the floating-point number to an integer when writing a floating-point number into a device register. Likewise, when reading a value from a register; it needs to be converted to float. In both cases, this is done by multiplying the number by a conversion factor. For example, to convert a floating-point number to IQ15, multiply by 32768.0 as shown below.

```
#if MATH_TYPE == IQ_MATH
    PwmReg = (int16)_IQtoIQ15(Var1);
#else // MATH_TYPE is FLOAT_MATH
    PwmReg = (int16)(32768.0L*Var1);
#endif
```

   Likewise, to convert from an IQ15 value to a floating-point value, multiply by 1/32768.0 or 0.000030518.0.
3. Do the following to take advantage of the on-chip floating-point unit:
   - Use C28x codegen tools version 5.0.2 or later.
   - Tell the compiler it can generate native C28x floating-point code. To do this, use the –v28 --float_support=fpu32 compiler switches. In Code Composer Studio, the float_support switch is on the advanced tab of the compiler options.
   - Use the correct run-time support library for native 32-bit floating point. For C code, this is rts2800_fpu32.lib. For C++ code with exception handling, use rts2800_fpu32_eh.lib.
   - Consider using the C28x FPU Fast RTS library (SPRC664) to get a performance boost from math functions such as sin, cos, div, sqrt, and atan. The Fast RTS library should be linked in before the normal run-time support library.

4 Package and Pinout

The 281x and 2833x/2823x are neither package nor pin-compatible. Any application being moved from 281x to the 2833x or 2823x requires a new board layout to accommodate the changes in pinout and package.

5 Operating Frequency and Power Supply

The required core voltage supply for the 281x devices depends on the operating frequency of the device. The 281x devices can operate up to 150 MHz with a core voltage of 1.9-V. A 1.8-V core voltage is required at 135 MHz and below. The 150 MHz 2833x/2823x devices require a 1.9-V core voltage and the 100 MHz devices require a 1.8-V core voltage. Both the 281x and 2833x devices require a 3.3-V I/O supply.

Note: For information regarding any electrical specifications, always refer to the TMS data manual.

See the following data manuals for the most recent detailed electrical specifications:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811,TMS320C2812 Digital Signal Processors Data Manual* (SPRS174)
- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers Data Manual* (SPRS439)

6 Power Sequencing

The restrictions placed on power sequencing have been relaxed.

For the 281x devices, the power sequencing requirements dictate that the V_{DDIO} rail must begin its ramp prior to the V_{DD} rail. For 2833x/2823x devices, the V_{DDIO} and V_{DD} rail can instead ramp together. For customers migrating their design from the 281x, the sequencing scheme used for the 281x devices can still be applied to a 2833x/2823x device.

See the appropriate data manual for each device for details related to power sequencing:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811,TMS320C2812 Digital Signal Processors Data Manual* (SPRS174)
- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers Data Manual* (SPRS439)

7 SARAM

This section highlights the major differences in the SARAM memory subsystem.

- **Increased amount of SARAM**

  On the 281x 18K x 16 words of SARAM were available. On the 2833x/2823x up to 34K x 16 are available.
- **Maximum SARAM block size 4K x 16**

  The H0 SARAM block at 0x3F8000 was split into two smaller memory blocks: L0 and L1. The maximum size of an SARAM block is now 4K x 16. The smaller memory blocks on the 2833x/2823x make it easier to partition code and data. If your code uses multiply and accumulate operations (MAC), for example, partition the opcode and two operands into three different memory blocks. This allows for maximum efficiency.
- **SARAM blocks are dual-memory mapped**

  Memory blocks L0, L1, L2 and L3 are all dual mapped into both high memory and low memory. The dual mapping of the memory gives flexibility when partitioning code as required by the application. The memory region in the upper 64K range is required when running 24x compatible code while the stack pointer (SP) can only access memory in the lower 64K. If the application is not porting 24x code, then either memory map location can be used for either data or code. Keep in mind that the stack pointer can still only access the lower 64K range.

Table 1. SARAM Addresses

Memory Address	281x Memory Block	2833x/2823x Memory Block (1)
0x00 8000 – 0x00 8FFF	L0	L0
0x00 9000 – 0x00 9FFF	L1	L1
0x00 A000 – 0x00 AFFF	N/A	L2
0x00 B000 – 0x00 BFFF	N/A	L3
0x00 C000 – 0x00 CFFF	N/A	L4 (2)
0x00 D000 – 0x00 DFFF	N/A	L5 (2)
0x00 E000 – 0x00 EFFF	N/A	L6 (2)
0x00 F000 – 0x00 FFFF	N/A	L7 (2)
0x3F 8000 – 0x3F 8FFF	H0	L0 Mirror
0x3F 9000 – 0x3F 9FFF		L1 Mirror
0x3F A000 – 0x3F AFFF	N/A	L2 Mirror
0x3F B000 – 0x3F BFFF	N/A	L3 Mirror

(1) Note that not all of the SARAM blocks are available on all family derivatives. Refer to the device-specific data sheets.
(2) DMA accessible block. 1 wait state in program space.

Note: The H0 memory block of the 281x now has L0 and L1 dual mapped in its place. Therefore, if code compiled for 281x is loaded without changing the memory map, data, or code that was originally in the H0 memory region, 0x3F 8000 – 0x3F 9FFF may be overwritten by the data or code from the L0 and L1 memory blocks.

- **Wait states**

  On 281x devices, all SARAM blocks are 0 wait state in both program and data space. On the 2833x/2823x devices, blocks L4, L5, L6 and L7 are 0 wait for accesses that use the data bus and 1 wait for accesses that use the program bus. A program bus access occurs when an instruction opcode is fetched or when program-space indirect or direct addressing is used. Instructions that use program-space addressing to access an operand include MAC, DMAC, QMACL, IMACL, PREAD and PWRITE. For example, MAC uses program-space addressing via the XAR7 register. This instruction sees a decrease in performance if the operand pointed to by XAR7 is in L4-L7. L4-L7 should be allocated for data space accesses before they are used for program code or data accessed via program-space addressing.

- **DMA accessible SARAM**

  The L4-L7 memory blocks can be used as a source and/or destination for each of the six channels. On the 281x, DMA was not available.

8 Flash and OTP

8.1 Size and Number of Sectors

The size and number of sectors has changed and code must be rebuilt accordingly. The exact Flash size as well as sector configuration varies from device to device as shown in Table 2.

Table 2. Sector Configuration Per Device

	F2812 F2811	F2810	F28235 F28335	F28234 F28334	F28232 F28332
	6 Sectors 16K X 16 + 4 sectors 8K X 16	3 Sectors 16K X 16 + 2 sectors 8K X 16	8 Sectors 32K X 16	8 Sectors 16K X 16	4 Sectors 16K X 16
Total	128K X 16	64K X 16	256K X 16	128K X 16	64K X 16

8.2 Flash Access Time

The access time of the Flash has increased by 1 ns. Depending on your CPU speed, you may need to update the wait states accordingly. For an operation at 150 MHz, the number of required wait states remains the same.

Note: To confirm timing information, always refer to the device-specific data manual .

8.3 Entry Point Into Flash and CSM Password Locations

On both the 281x and 2833x/2823x, the boot ROM entry point and code security module password locations are located at the highest addresses of Flash sector A. This address has shifted on the 2833x/2823x as the entire Flash array moved; they are still located at the end of sector A. To keep the CSM unlocked during debug, you can open a memory window to the new password locations at 0x33 FFF8 - 0x33 FFFF. If you use a Code Composer Studio GEL file to unlock then CSM, then the GEL function needs to be modified with the new addresses. Table 4 in Section 9 shows a summary of the boot ROM entry point locations.

8.4 Entry Point Into OTP

On both the 281x and 2833x/2823x devices, the boot ROM entry point into OTP is the first address within the OTP. This location has shifted as the memory mapping of the OTP has moved. Table 4 in Section 9 shows a summary of the boot ROM entry point locations.

8.5 Flash Programming

The method for programming the device remains the same. TI supplies a Flash application program interface (API) per device that is used as the basis of all programming solutions. The Flash API and programming algorithms for the F281x devices cannot be used on the F2833x/F2823x. New Flash APIs are required to program these devices; however, the Flash API function prototypes remain compatible.

Note: The Flash API includes timing critical delay loops. These loops should always be run from 0 wait memory to be timing accurate. On the 2833x/2823x, the L4-L7 SARAM blocks have 1 wait state in program space so they are not suited for running the Flash API.

9 Boot ROM

9.1 Enhancements

The following enhancements have been made to the boot ROM:

- Added boot loaders for the inter-integrated circuit (I2C-A), multichannel buffered serial port (McBSP-A) and enhanced controller area network (eCAN-A) modules
- Boot to XINTF is done through the boot ROM as the 2833x and 2823x do not have MP/$\overline{\text{MC}}$. Refer to Section 11.2.3.
- The SPI-A bootloader has been updated to support both serial 16-bit addressable EEPROMs and 24-bit addressable serial peripheral interface (SPI) Flash.
- A parallel bootloader for the XINTF has been added. This is similar to the general-purpose input/output (GPIO) parallel loader except the XINTF data lines are used to import data.
- The IQMath tables have been updated to include an exponent table
- Floating-point tables for sin, cos and atan have been added
- The boot ROM calibrates the ADC as described in Section 11.2.1

Note: The boot ROM locations of the IQMath tables has shifted. Make sure to use the new addresses in your linker command file as shown in the *C2833x/C2823x C/C++ Header Files and Peripheral Examples* (SPRC530).

9.2 Boot-Mode Selection

The boot-mode pin configuration has changed to enable the different bootloaders and is shown in Table 3. For the bootloader to properly start, you must configure each of the four pins before reset. The data stream format used is identical to that used on the 281x devices.

Table 3. Boot Mode Selection

Mode	GPIO87 XA15	GPIO86 XA14	GPIO85 XA13	GPIO84 XA12	Description
F	1	1	1	1	Jump to Flash
E	1	1	1	0	SCI-A
D	1	1	0	1	SPI-A
C	1	1	0	0	I2C-A
B	1	0	1	1	eCAN-A
A	1	0	1	0	McBSP-A
9	1	0	0	1	Jump to XINTF x16
8	1	0	0	0	Jump to XINTF x32
7	0	1	1	1	Jump to OTP
6	0	1	1	0	Parallel I/O
5	0	1	0	1	Parallel XINTF
4	0	1	0	0	Jump to SARAM
3	0	0	1	1	Branch to check boot mode
2	0	0	1	0	Jump to Flash, skip ADC calibration
1	0	0	0	1	Jump to SARAM, skip ADC calibration
0	0	0	0	0	SCI-A, skip ADC calibration

Note: Modes 0, 1 and 2 in Table 3 are for TI debug only. Skipping the ADC calibration function in an application causes the ADC to operate outside of specification. For more detailed information on the ADC_cal() function, see the *TMS320x2833x, 2823x Analog-to-Digital Converter (ADC) Module Reference Guide* (SPRU812)

9.3 Entry Points to Memory

The location of the *boot to SARAM* entry point location has moved from the H0 memory block to the starting address of M0. The entry point into the Flash memory block is still the two words right before the password locations. The address has changed to 0x33 FFF6 to reflect the new memory mapping of the Flash. The entry point into the one-time programmable (OTP) is still the first word of the OTP block but the address has changed to reflect the new location of the OTP. Table 4 summarizes the changes to the memory entry point locations.

Table 4. Boot Loader Entry Points

	281x Entry Point	2833x/2823x Entry Point	Notes
Jump to Flash	0x3F 7FF6	0x33 FFF6	Two words before the password locations
Jump to SARAM	0x3F 8000	0x00 0000	Moved from H0 to M0
Jump to OTP	0x3D 7800	0x38 0400	First word of the OTP
Jump to XINTF (x16 or x32)	N/A	0x10 0000	Boot to XINTF is now through the boot ROM

9.4 Reserved Memory

The M0 memory block address range 0x0002 - 0x004E is reserved for the stack and .ebss code sections during the boot-load process. If code is bootloaded into this region there is no error checking to prevent it from corrupting the boot ROM stack. Address 0x0000-0x0001 is the boot to M0 entry point. This should be loaded with a branch instruction to the start of the main application when using *boot to SARAM* mode. The 281x boot ROM uses M1 for stack.

See the following reference guides for more information on boot ROM:

- *TMS320x281x DSP Boot ROM Reference Guide* (SPRU095)
- *TMS320x2833x, 2823x Boot ROM Reference Guide* (SPRU963)

10 Clocks and System Control

This section describes changes that affect device clocking and system control. This includes new and renamed registers, pin functionality, new logic, and other enhancements. For more information on system control, see the following reference guides:

- *TMS320x281x DSP System Control and Interrupts Reference Guide* (SPRU078)
- *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0)

10.1 Register Changes

Table 5 shows a summary of registers that were added, renamed, or modified from the 281x devices. The sections that follow describe changes that were made. This section does not include the new GPIO, ePWM, eCAP, and enhanced quadrature encoded pulse (eQEP) registers as they can be considered as all new.

Table 5. New, Renamed, and Removed Registers

Register	Change	Description
PLLSTS	New	PLL Status Register. This register includes the PLL lock status bit and information from the missing oscillator-detect logic.
PCLKCR0	Renamed Updated	This register is named PCLKCR on the 281x devices. Bits have been added to enable clocks to new peripherals.
PCLKCR1	New	New register used to enable/disable clocks to the ePWM, eCAP, and eQEP modules.
PCLKCR3	New	New register to add clock enables for the XINTF, CPU Timers, DMA and input qualification.

Table 5. New, Renamed, and Removed Registers (continued)

Register	Change	Description
LPMCR0	Updated	Updated so you can enable the watchdog interrupt to wake the device from STANDBY mode. On 281x this bit is in the LPMCR1 register.
LPMCR1	Removed	This register is replaced by the GPIOLPMSEL register located in the GPIO register file.
GPIOPLMSEL	New	Selects the GPIO signal that can wake the device from HALT and STANDBY.
MAPCNF	New	Selects the register mapping for the ePWM/HRPWM modules. If this bit is 0, then the modules are mapped as on 280x/2801x/28044x. If this bit is 1, then the modules are remapped to peripheral frame 3 where they can be accessed by the DMA module.

10.2 Input Oscillator

10.2.1 Separate XCLKIN and X1 Pins

The pins X1 and X2 are specified at the V_{DD} core voltage on both the 281x and 2833x/2823x devices. If an external 3.3-V oscillator is used on the 281x devices, the input clock has to be level shifted before it can be sent into the device. This requirement has been removed by providing a separate 3.3-V XCLKIN pin. If a crystal is not used, an external oscillator can be connected to the XCLKIN pin and the X2 pin can be left unconnected.

Note: **External clock on the XCLKIN pin:** When using XCLKIN as the external clock source, you must tie X1 low and leave X2 disconnected. In this case, an external oscillator clock is connected to the XCLKIN pin, which allows for a 3.3-V clock source to be used.

Note: **External clock on the X1 pin:** When using X1 as the clock source, you must tie XCLKIN low and leave X2 disconnected. In this case, an external oscillator clock is connected to the X1 pin, which allows for a clock source at the V_{DD} core voltage to be used.

10.2.2 Oscillator Missing Detect Logic

Logic has been added to detect whether the main oscillator clock is missing. If neither XCLKIN or X1 has a clock and the oscillator clock is missing, the device switches to a *limp mode* frequency output by the phase-locked loop (PLL) and resets.

10.3 Phase Locked Loop (PLL)

10.3.1 CLKIN Input Divider

On 281x, the output from the PLL is always divided by two (multiplied by one-half), unless the PLL is disabled. On the 2833x/2823x, the divider is instead controlled by the DIVSEL bits in the PLLSTS register. This divider can be set to /1, one-half or 1/4. By default, after reset, the divider is set for 1/4. The boot ROM changes DIVSEL so that the loaders run at one-half the input clock. Note that the boot ROM leaves the divider in this state which is compatible with 281x.

10.3.2 PLL Lock Status Bit

When a new PLL ratio is selected in the PLL control register (PLLCR), there is a required number of cycles that must pass before the PLL locks at the new frequency. A PLL lock status bit has been added to the PLL status register (PLLSTS) to indicate when the PLL has locked. On the 281x devices, a software delay is used to wait for these cycles to pass.

10.3.3 PLL Disable and PLL OFF

On the 281x devices, the XF_PLLDIS signal is sampled at reset and, if found to be low, the PLL on the device is disabled. On the 2833x/2823x devices, the XF_PLLDIS signal is no longer available. Instead, to disable the PLL, a bit has been added to turn off the PLL for system noise and low power operation when the PLL is not required. To use this feature, the PLL must first be in bypass mode (PLLCR = 0x0000).

10.3.4 Procedure to Change PLLCR

With the introduction of oscillator-missing-detect logic, the procedure to change the PLLCR register has changed slightly. On the 2833x/2823x, the missing clock status must be checked before changing the PLLCR register. If the status bit is set (missing clock detected) appropriate action must be taken by the firmware. If a missing clock has not been detected, then the PLLCR can be modified by the following sequence:

1. Disable oscillator missing detect logic.
2. Set PLLSTS[DIVSEL] = 0 for SYSCLKOUT = 1/4 input clock
3. Modify PLLCR register.
4. Wait for PLL lock status (PLLSTS[PLLLOCKS]) to indicate that the PLL has locked.
5. Re-enable the oscillator-missing-detect logic and modify PLLSTS[DIVSEL] as desired.

10.4 Peripheral Clock Enable Registers

Due to new peripherals and additional instances of old peripherals, the registers to enable and disable the clocks to individual peripherals have been updated. There is one peripheral clock control register named PCLKCR on the 281x devices. There are now additional registers (PCLKCR0, PCLKCR1, and PCLKCR3) that enable and disable the clocks to the individual peripheral modules. PCLKCR2 is reserved but not used on the 2833x/2823x devices.

10.5 Low Power Modes and STANDBY and HALT Wake Up Signal Selection

On 2833x/2823x devices, you can enable any input signal corresponding to pins GPIO0 through GPIO31 to wake up the device from the STANDBY and HALT low-power modes. The selected pin or pins can be configured either as general-purpose inputs (GPIO) or as peripheral inputs. While more than one signal can be specified, typically only one is used. The signal selection is made in the LPM GPIO Select Register (GPIOLPMSEL). On the 281x, only a select few signals can wake the device from STANDBY and only the XNMI and $\overline{\text{XRS}}$ signals can wake the device from HALT mode.

To save power, clock enable/disable control has been added to the CPU Timers, XINTF and GPIO input logic. The clock enable/disable control for these peripherals is in the Peripheral Clock Control Register 3 (PCLKCR3). By default, clocks are enabled to the CPU Timers and GPIO input logic; this is compatible with 281x. The XINTF clock is disabled by default and must be enabled before writing to the XINTF registers. The GPIO input logic enable/disable control can be used to disable input logic when the respective pin is configured as an output. This is to reduce power consumption when a pin is configured as an output.

10.6 General-Purpose I/O (GPIO)

The GPIO ports have been completely redesigned to allow for a larger number of peripherals to be MUXed per pin. This allows you to pick and choose which peripherals to enable for your particular application. Changes to the GPIO module include:

10.6.1 GPIO Ports

On the 281x devices, GPIO signals are divided into 16-bit ports. On the 2833x/2823x devices, the GPIO signals are assigned to 32-bit ports. Port A consists of GPIO0-GPIO31, port B consists of GPIO32-GPIO63, and port C consists of GPIO64-GPIO87. The GPIO control and data registers have been moved from peripheral frame 2 (16-bit access only) to peripheral frame 1, which allows for 32-bit as well as 16-bit operations on the registers.

10.6.2 GPIO MUX Registers

The GPIO MUX logic has been redesigned to allow for a higher level of peripheral multiplexing. The 2833x/2823x GPIO MUX can multiplex up to three independent peripheral signals into a signal GPIO pin, in addition to providing individual pin toggling I/O capability. There are two MUX registers for each GPIO port.

10.6.3 GPIO Qualification

On 2833x/2823x devices, the type of qualification required for input signals on GPIO0-GPIO63 can be specified by you. This qualification applies whether the pin is configured as a GPIO or peripheral. GPIO64-GPIO87 do not have input qualification to reduce delays on the XINTF signals.

For GPIO0-GPIO63, the three qualification options are:

- Synchronization to the system clock (SYSCLKOUT) only. This is the default mode of all pins at reset.
- Qualified using a sampling window specified by window size and sampling period. The sampling window size is the number of times the signal must be sampled at the same level to be qualified. You can specify a sampling window size of either six samples or three samples for each of the GPIO signals. On the 281x device, the sampling window size is fixed to six samples only.

  The qualification sampling period is how often the signal is sampled within the sampling window. The sampling period is specified for each group of eight signals. For example, GPIO0-GPIO7 all use the same qualification sampling period. On the 281x device, the sampling period is specified per 16-bit port.
- No synchronization applied. This mode is only valid when the pin is configured as an input to a peripheral.

On the 281x devices, the type of input qualification available depends on the function of the pin in its peripheral mode:

- In 281x, Type 1 qualification allows the signal to be qualified via a sampling window or synchronized to SYSCLKOUT. This applies to pins connected to the event manager (EV).
- In 281x, Type 2 pins, the asynchronous signal is fed to the peripheral without qualification. This applies to pins that are connected to communications ports such as serial communications interface (SCI), SPI, and eCAN. If these pins are used as GPIO, the input qualification defaults to synchronize to SYSCLKOUT only.

The 2833x/2823x input qualification is much more flexible then on the 281x. Take care, however, to select their input qualification. The default mode, synchronize to SYSCLKOUT, may not be desired for communication peripherals such as SCI, SPI, I2C, McBSP, and eCAN.

10.6.4 Internal Pullup Configuration

For each of the GPIO pins, you can enable or disable an internal pullup resistor through software.

On the 281x devices, internal pullup resistors are included by default for specific input signals while other signals do not have an internal pullup. This is not configurable on the 281x devices.

10.6.5 GPIO Data Registers (GPIODAT)

On the 281x, when a GPIO pin is configured as an output, reading the GPIODAT register reflects the state of the GPIODAT output latch. On the 2833x/2823x, reading the GPIODAT register actually reflects the value on the pin. The advantage of the 2833x/2823x implementation is that you can detect if a pin is actually driving the output value written into the GPIODAT register. The down side is that there is a lag between writing to the GPIODAT and then reading the GPIODAT input. Therefore, back-to-back read-modify-write operations may pick up a stale value of the pin. For more information, see the *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0).

10.7 XF Functionality

The 281x devices include an XF function on a general-purpose output pin. This pin, when configured as XF, could be managed using the assembly instructions "SETC XF" and "CLRC XF". On 2833x/2823x, the alternative is to use the GPIO SET and CLEAR registers to toggle pins. A write to these registers takes 1 cycle so the performance and function is the same.

11 Peripherals

New peripherals have been added and others have been updated. This section briefly describes the changes. For an overview of all peripherals available, see the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (SPRU566).

11.1 New Peripherals

The 2833x/2823x devices include new peripherals that are not available on the 281x devices.

11.1.1 Control Peripherals

The EV module on the 281x devices was originally developed for the 240x DSPs. This module has been removed on 2833x/2823x devices and the functionality has been replaced by three new peripherals: ePWM, eCAP and eQEP. The peripherals available per device are shown in Table 6. Each of the 2833x/2823x control peripherals are described in the following section.

Table 6. Available Control Peripherals

Device	Event Manager	ePWM With High Resolution (HRPWM)	ePWM	eCAP	eQEP
281x	EV-A, EV-B	-	-	-	-
28335, 28235	-	ePWM1 - ePWM6	ePWM1-ePWM6	eCAP1 - eCAP6	eQEP1, eQEP2
28334, 28234	-	ePWM1 - ePWM6	ePWM1 - ePWM6	eCAP1 - eCAP4	eQEP1, eQEP2
28332, 28232	-	ePWM1 - ePWM4	ePWM1- ePWM6	eCAP1 - eCAP4	eQEP1, eQEP2

- **Enhanced Pulse Width Modulator (ePWM) Module**

  The ePWM peripheral is used to control many power-related systems in both commercial and industrial equipment. The main systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS) and other forms of power conversion. The ePWM can perform a digital-to-analog converter (DAC) function where the duty cycle is equivalent to a DAC analog value sometimes referred to as a power DAC.

  Each ePWM module on a device is daisy-chained together via a synchronization scheme that allows them to operate as a either individual units or as a single system if required. For more detailed information on the ePWM module, see the *TMS320x2833x, 2823x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (SPRUG04).

  Table 7 shows an overview of the ePWM resources available on the 28335 as compared to that of the 281x event manager (EV).

  Some ePWM instances on the 2833x/2823x include a high-resolution extension. The high-resolution PWM (HRPWM) module extends the time resolution capabilities of the conventionally derived digital pulse width modulator (PWM). HRPWM is typically used when PWM resolution falls below ~ 9-10 bits. This occurs at PWM frequencies greater than ~200 kHz when using a CPU/system clock of 100-150 MHz. For more detailed information on the HRPWM module, see the *TMS320x2833x, 2823x High-Resolution Pulse Width Modulator (HRPWM) Reference Guide* (SPRUG02).

  The key features of HRPWM are:

  – Extended time resolution capability
  – Used in both duty cycle and phase-shift control methods
  – Finer time granularity control or edge positioning using extensions to the compare and phase registers
  – Implemented using the *A* signal path of the ePWM, i.e., on the EPWMxA output. The EPWMxB output has conventional PWM capabilities.
  – Self-check diagnostics software mode to check whether the micro edge positioner (MEP) logic is running optimally.

Table 7. 28335 ePWM Compared to 281x Event Manager

	28335 ePWM	281x EV-A + EV-B
Timers	16-bit x 6	16-bit – x2 (EV-A), x2 (EV-B) (shared with PWM, CAP, QEP)
PWM	12 independent 16-bit + 6 independent (eCAP in APWM mode)	10 independent 16-bit
High-Resolution PWM Control	6 EPWM × A Channel Outputs	No
Compare	2 per time-base	1 per time-base
Time-Base Sync	Yes	No
Phase Control	Yes	No
Dead-Band	10-bit Independent falling edge delay Independent rising edge delay	~7-bit Rising edge = falling edge delay
Chopper	Yes	No
Trip (Fault) Zones	6 Assign to any ePWM module Cycle-by-cycle or one-shot Can force ePWM pins high, low, or high-impedance on trip	6 Hard-wired to a specific PWM Forces high-impedance on trip
Interrupts	6 Can be pre-scaled to all, second, or third event	24 no pre-scaling
ADC Start of Conversion	Counter = zero, period, compare A, compare B	Counter = zero, period, and compare of TxPWM only

- **Enhanced Capture (eCAP) Module**

  The eCAP module is essential in systems where the accurate timing of external events is important. When not being used to capture external events, the eCAP peripheral can be used to implement a single channel PWM generator. Table 8 shows a comparison of eCAP with the event manager (EV).

Table 8. 28335 eCAP Compared to 281x Event Manager

	28335 eCAP	281x EV-A + EV-B
Timers	32-bit X 4	16-bit - X2 (EV-A), X2 (EV-B) (shared among PWM, CAP, QEP)
Channels	6 channels	3 channels shared with QEP
Timestamp	32-bit	16-bit
Capture buffers per channel	4 memory-mapped registers	2-level FIFO
Edge qualifier	4 total, one per buffer	1
Sequencer	Yes	No
Delta time mode	Yes	No
Absolute time mode	Yes	Yes
APWM mode	Yes	No
Event pre-scaler	Yes	No
Interrupts	4 Can be pre-scaled to all, second, or third event	6 No pre-scaling

For more detailed informaiton on the eCAP module, see the *TMS320x2833x, 2823x Enhanced Capture (eCAP) Module Reference Guide* (SPRUFG4).

- **Enhanced Quadrature Encoded Pulse (eQEP) Module**

  The eQEP module is used for interfacing to a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in a high-performance motion and position control system. Table 9 shows a comparison of 28335 eQEP and 281x EV.

Table 9. 28335 eQEP Compared to 281x Event Manager

	28335 eQEP	281x EV-A + EV-B
Timers	32-bit X 2	16-bit - X2 (EV-A), X2 (EV-B) (shared among PWM, CAP, QEP)
Channels	2 channels 32-bit position counter	2 channels 16-bit shared counter
Speed measurement support	Yes Frequency and period based	No
Frequency measurement	Yes Unit timer	No
Position compare	Yes Position compare register	No
Shaft stall detect	Yes Built-in watchdog	No
Error checking	Yes Phase and count errors	No
External strobes	Index and home	Index
Interrupts	2 Can be pre-scaled to all, second, or third event	0

Details of the eQEP module can be found in the *TMS320x2833x, 2823x Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide* (SPRUG05).

11.1.2 Direct Memory Access (DMA)

The direct memory access module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as *ping-pong* data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine requiring a peripheral interrupt trigger to start a transfer. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfers has either started or completed. Major features of the DMA are:

- Six channels. Each channel has its own interrupt in the PIE vector table.
- Trigger sources include:
  - ADC sequencer 1 and 2
  - McBSP transmit and receive
  - External interrupts 1-7 and 13
  - CPU timers
  - ePWM1-6 start of conversion (SOCA, SOCB)
  - Software
- Data sources and destinations: L4-L7 SARAM, all XINTF zones, ADC result registers, McBSP transmit and receive registers, ePWM registers.
- Word size can be configured for x16 or x32 bits.

For more information, see the *TMS320x2833x, 2823x Direct Memory Access (DMA) Reference Guide* (SPRUFB8) .

11.1.3 Inter-IC (I2C) Bus

An I2C bus has been added to the 2833x/2823x devices. This module is not available on the 281x. For more information, see the *TMS320x28xx, 28xxx Inter-Integrated Circuit (I2C) Reference Guide* (SPRU721).

11.2 Updated Peripherals

The following peripherals have been updated and are documented in new 2833x/2823x specific reference guides:

- *TMS320x2833x, 2823x Analog-to-Digital Converter (ADC) Module Reference Guide* (SPRU812)
- *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0)
- *TMS320x2833x, 2823x Boot ROM Reference Guide* (SPRU963)
- *TMS320x2833x, 2823x Multichannel Buffered Serial Port (McBSP) Reference Guide* (SPRUFB7)

The 281x guides should be replaced with these guides if you are using a 2833x/2823x device. This section contains a highlight of the changes.

11.2.1 Analog-to-Digital Converter (ADC)

- **ADC Differences on 2833x/2823x**
  - RefP/RefM capacitors reduced from 10 µF on 281x to 2.2 µF on 2833x/2823x, resulting in lower cost/smaller body size.
  - RESEXT resistor reduced from 24.9 kΩ on 281x to a standard 22 kΩ 5% resistor
  - External reference option reduced to one pin, 2.048 V standard reference
  - Main power pins moved from 3.3-V node to 1.8-V, cutting power consumption for the analog block
  - Reduced gain error
  - Added offset correction register (OFFTRIM) dynamically removes offset from ADC results.
  - Result registers are dual mapped to data space and are right justified for continuous run applications.

- Two new interrupts have been defined for the ADC to handle SEQ1 and SEQ2 interrupt conditions separately. The existing 281x ADCINT has been retained. Therefore, you can choose to use either the ADC interrupt or the new SEQ1 and SEQ2 interrupts.

– DMA accessible result registers

Note: For the latest specifications, see the device-specific data manual .

Table 10. New ADC Registers

Register	Change	Description
RESULT0 - RESULT15	Dual Mapped	Additional mapping starting at 0xB00. This mapping is right justified and can be accessed by the DMA.

- **ADC Calibration**
  On the 2833x/2823x, the ADC is calibrated by the boot ROM software at boot time. The ADC_cal() routine is programmed into TI reserved OTP memory by the factory. The boot ROM automatically calls the ADC_cal() routine to initialize the ADC Reference Select Register (ADCREFSEL) and ADC Offset Trim Register (ADCOFFTRIM) with device-specific calibration data. During normal operation, this process occurs automatically and no action is required by you. If the boot ROM is bypassed by Code Composer Studio during the development process, then ADCREFSEL and ADCOFFTRIM must be initialized by the application. For working examples, see the ADC initialization in the *C2833x/C2823x C/C++ Header Files and Peripheral Examples* (SPRC530). For more detailed information on the ADC_cal() function, see the *TMS320x2833x, 2823x Analog-to-Digital Converter (ADC) Module Reference Guide* (SPRU812)

11.2.2 Code Security Module (CSM)

This module protects the Flash, OTP, and L0/L1 SARAM blocks as it did on the 281x devices. On the 2833x/2823x, the module was extended to protect both mappings of the L0 and L1 as well as L2 and L3.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to Flash, user OTP, L0, L1, L2 or L3 memory while the emulator is connected will trip the ECSL and break the emulation connection. To allow emulation of secure code, while maintaining the CSM protection against secure memory reads, you must write the correct value into the lower 64 bits of the KEY register, which matches the value stored in the lower 64 bits of the password locations within the Flash. Note that dummy reads of all 128 bits of the password in the Flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match. When initially debugging a device with the password locations in Flash programmed (i.e., secured), the emulator takes some time to take control of the CPU. During this time, the CPU starts running and may execute an instruction that performs an access to a protected ECSL area. If this happens, the ECSL trips and causes the emulator connection to be cut. Two solutions to this problem exist:

- Use the wait-in-reset emulation mode that holds the device in reset until the emulator takes control. The emulator must support this mode for this option.
- Use the *Branch to check boot mode* boot option. This sits in a loop and continuously polls the boot-mode select pins. You can select and then exit this boot mode once the emulator is connected by re-mapping the PC to another address or by changing the boot-mode selection pins to the desired boot mode.

The CSM password is still the last 128-bits within sector A of the Flash. On the 281x, the password was at 0x3F 7FF8 - 0x3F 7FFF; on 2833x, it is at 0x33 FFF8 - 0x33 FFFF. If you have any Code Composer Studio GEL scripts that unlock the CSM during debug, they need to be modified to reflect the new password address. An alternative is to keep a memory window open to the password locations at 0x33 FFF8 during debug.

CSM detailed information is included in the appropriate System Control and Interrupts Reference Guides:

- *TMS320x281x DSP System Control and Interrupts Reference Guide* (SPRU078)
- *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0)

11.2.3 External Memory Interface (XINTF)

The XINTF on the 2833x/2823x devices is very similar to the TMS320x281x XINTF. The main differences are described in this section.

- **Data Bus Width Support for x16 and x32**

  Each XINTF zone can be configured individually to use a 16-bit or 32-bit data bus. Using the 32-bit mode improves performance since 32 bits of data can be read or written in a single access. The data bus width does not change the size of the XINTF zones or memory reach. In 32-bit mode, the lowest address line XA0 becomes a second write enable. The 281x XINTF is limited to a 16-bit data bus.
- **Address Bus Reach Increase**

  The address reach has been extended to 20 address lines. Zone 6 and Zone 7 both use the full address reach of 1M x 16 words each. The 281x address reach is 512k x 16 words.
- **Direct Memory Access (DMA) Availability**

  All three XINTF zones are connected to the on-chip DMA module. The DMA can be used to copy code and data to or from the XINTF while the CPU is processing other data. The 281x devices do not include a DMA.
- **XINTF Clock (XTIMCLK) Enable/Disable**

  The XINTF clock (XTIMCLK) is disabled by default to save power. XTIMCLK can be enabled by writing a 1 to bit 12 of the PCLKCR3 register. PCLKCR3 is documented in the device-specific system control and interrupts user's guide. For the 2833x/2823x devices, it is *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (literature number SPRUFB0). Turning off XTIMCLK does not turn off XCLKOUT. There is a separate control to turn off XCLKOUT. On the 281x, XTIMCLK is always enabled.
- **XINTF Pins MUXed with GPIO**

  Many of the XINTF pins are MUXed with general purpose I/O. The GPIO mux registers must be configured for XINTF operation before you can use the XINTF. This is done by the boot ROM code when boot to XINTF mode is select. On the 281x, the XINTF has dedicated pins.
- **Number of Zones and Chip Select Signals**

  The number of XINTF zones has been reduced to 3: Zone 0, Zone 6 and Zone 7. Each of these zones has a dedicated chip select signal. Zone 0 is still read-followed-by-write protected and best suited for peripherals. On the 2812 devices, some zone chip select signals are shared between zones. Zone 0 and Zone 1 share XZCS0AND1 and Zone 6 and Zone 7 share XZCS6AND7.
- **Zone 7 Memory Mapping (no MP/$\overline{\text{MC}}$ pin)**

  All zones on the 2833x/2823x, including Zone 7, are always mapped. To boot to XINTF, you select boot mode 8 or 9 shown in Table 3. This configures Zone 6 for either x16 or x32 operation and jumps to the first address in Zone 6 at 0x10 0000. On the 281x devices, the MPNMC input signal determines if Zone 7 is mapped.

  In addition, on 2833x/2823x, Zone 6 and 7 do not share any locations. On 281x, Zone 7 is mirrored within Zone 6.
- **Zone Memory Map Locations**

  Zone 0 starts at address 0x4000 and is 4K x 16. On 281x, Zone 0 starts at address 0x2000 and is 8K x 16. Zone 6 and 7 are both 1M x 16 and start at 0x100000 and 0x200000, respectively. On 281x, these two zones are 512K x 16 and 16K x 16.

- **EALLOW Protection and Other Register Changes**
  The XINTF registers are now EALLOW protected. On 281x, the XINTF registers were not EALLOW protected. Other changes are summarized in Table 11.

Table 11. New, Updated, and Removed XINTF Registers

Register	Change	Description
XTIMING0	Updated	XSIZE can now be x16 or x32 and the register is EALLOW protected.
XTIMING1	Removed	Not used
XTIMING2	Removed	Not used
XTIMING6	Updated	XSIZE can now be x16 or x32 and the register is EALLOW protected.
XTIMING7	Updated	XSIZE can now be x16 or x32 and the register is EALLOW protected.
XINTCNF2	Updated	MP/$\overline{MC}$ mode bit is now reserved and the register is EALLOW protected.
XRESET	New	A hard reset may be used in cases where the CPU detects the XREADY signal is stuck low during a DMA transfer.

For the most recent XINTF timing information, see the appropriate data manual:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811,TMS320C2812 Digital Signal Controllers Data Manual* (SPRS174)
- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers Data Manual* (SPRS439)

11.2.4 Multichannel Buffered Serial Port (McBSP)

The FIFOs on the McBSP have been removed and replaced with an interface to the DMA. To reflect this change, the register set has been moved from Peripheral Frame 2 to Peripheral Frame 3. In addition, the changes shown in Table 12 have been made to the register set. The McBSP on 2833x/2823x does not support ABIS mode.

Table 12. New, Updated, and Removed McBSP Registers

Register	Change	Description
MFFTX	Removed	No longer needed without FIFOs
MFFRX	Removed	No longer needed without FIFOs
MFFCT	Removed	No longer needed without FIFOs
MFFINT	Updated	Renamed the McBSP Interrupt Enable Register.
MFFST	Removed	No longer needed without FIFOs

11.2.5 Enhanced Controller Area Network (eCAN)

The 2833x/2823x eCAN is now clocked at one-half the SYSCLKOUT frequency, unlike 281x which clocks the eCAN module at SYSCLKOUT. Code written for the eCAN needs to take this timing change into account. Otherwise, the eCAN module is functionally the same and the register sets are identical on the two device groups.

11.3 Communication Peripherals

The SPI and the Serial Communications Interface (SCI) remain functionally the same as on the 281x devices. The Enhanced Controller Area Network (eCAN) remains the same with the exception of the fixed errata mentioned in Section 13.

More instances of the communication peripherals are available on the 2833x/2823x devices (see Table 13) than on the 281x. On 281x, two SCIs were available while the 2833x/2823x offers up to three. For the eCAN module, the 281x offers one instance while the 2833x/2823x offers up to two.

Table 13. Communication Peripherals

Device	SCI Modules	SPI Modules	eCAN Modules
281x	SCI-A, SCI-B	SPI-A	eCAN-A
28335/28235	SCI-A, SCI-B, SCI-C	SPI-A	eCAN-A, eCAN-B
28334/28234	SCI-A, SCI-B, SCI-C	SPI-A	eCAN-A, eCAN-B
28332/28232	SCI-A, SCI-B	SPI-A	eCAN-A, eCAN-B

The register set for the SCI, SPI, and eCAN peripherals are identical on the 281x and the 2833x/2823x. The memory addresses of the registers for each instance of peripheral are also identical. For example, SCI-A registers on 281x are at the same location as SCI-A registers on 2833x/2823x. In addition, the interrupt vector location in the PIE vector table is identical to that on the 281x for SCI-A, SCI-B, SPI-A and eCAN-A. New interrupt vectors have been added to the PIE vector table for the additional peripheral instances (ISCI-C and eCAN-B).

Code that is written for the SCI, SPI, and eCAN on the 281x can be directly targeted for the 2833x/2823x with two exceptions:

- The 2833x/2823x eCAN is clocked at one-half the SYSCLKOUT frequency. The 281x clocks the eCAN module at SYSCLKOUT.
- The GPIO setup for the peripheral must be updated to accommodate the new GPIO MUXing scheme.

11.4 Removed Peripherals

The following peripherals are available on the 281x devices but are not available on 2833x/2823x derivatives:

- Event manager (EV) - The event manager functionality has been replaced on 2833x/2823x devices with three newly designed peripherals: ePWM, eCAP and eQEP.

12 Interrupts

Changes to interrupts include updates to the PIE module and handling of external interrupts.

12.1 Peripheral Interrupt Expansion (PIE) Module

The functionality of the PIE module and of the PIE configuration registers (PIE, Acknowledge Register (PIEACK), PIE, INTx Group Flag Register (PIEIFRx), PIE, INTx Group Enable Register (PIEIERx) etc.) are identical to the 281x devices. The PIE vector table has been updated to support:

- Interrupts issued by the new peripheral blocks such as DMA, ePWM, eCAP, eQEP, I2C
- Interrupts for the additional instances of existing peripheral blocks such as SCI-C and eCAN-B
- Two new interrupts for the ADC to handle SEQ1 and SEQ2 interrupt conditions separately. SEQ1 has been assigned to INT1.1 and SEQ2 to INT1.2. The existing ADCINT has been retained. You can choose to use the ADC interrupt or the new SEQ1 and SEQ2 interrupts.
- New interrupts have been added for the five new additional external interrupts: XINT3 - XINT7
- The floating-point unit latched overflow and latched underflow flags are connected to the PIE for debugging overflow and underflow conditions in your application.

12.2 External Interrupts

12.2.1 Selecting Interrupt Polarity

The polarity of the XINT1, XINT2, and XNMI interrupts can be configured three ways on the 2833x/2823x devices:

- Positive edge-triggered
- Negative edge-triggered
- Both positive and negative edge-triggered

On the 281x devices, configuring the polarity as both positive and negative edge-triggered is not supported. This configuration is done in the XINT1 Configuration Register (XINT1CR), XINT2 Configuration Register (XINT2CR), and the XNMI Configuration Register (XNMICR).

12.2.2 XNMI Interrupt Configuration

For the XNMICR register, the functionality for ENABLE = 1 and SELECT = 1 has been changed slightly. On the 281x devices, this configuration setting enables both the NMI and the INT13 interrupts to the CPU on 281x devices. This configuration has been changed to be more useful; when ENABLE = 1 and SELECT = 1, the following functionality occurs:

- NMI interrupt is disabled
- INT13 connected to a GPIO Port A signal selected as the XNMI interrupt
- Time stamp counter is enabled

12.2.3 Five Additional Interrupts

Five additional interrupts have been added: XINT3 - XINT7. Each interrupt has its own vector within the PIE vector table. You select the source for each of these five interrupts from GPIO32-GPIO63.

12.2.4 External Interrupt Signal Selection

You can now assign a GPIO signal from port A (GPIO0 – GPIO31) to be the interrupt source for XINT1, XINT2, and XNMI. Likewise, GPIO signals from port B (GPIO32 - GPIO63) can be assigned to be the interrupt source for XINT3 - XINT7. This selection is made in the XINT1 GPIO Input Select Register (GPIOXINT1SEL), XINT2 GPIO Input Select Register (GPIOXINT2SEL), XINT3 GPIO Input Select Register (GPIOXINT3SEL), XINT4 GPIO Input Select Register (GPIOXINT4SEL), XINT4 GPIO Input Select Register (GPIOXINT5SEL), XINT6 GPIO Input Select Register (GPIOXINT6SEL), XINT7 GPIO Input Select Register (GPIOXINT7SEL) and the XNMI GPIO Input Select Register (GPIOXNMISEL).

On the 281x devices, only XINT1, XINT2, and XNMI are available. The inputs to the interrupts on 281x are dedicated signals.

13 Errata Fixes

For more information on the various advisories, see the TI website for the most recent device-specific silicon errata. This includes:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 DSP Silicon Errata* (SPRZ193)
- *TMS320R2811, TMS320R2812 Digital Signal Processor Silicon Errata* (SPRZ226)
- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 DSC Silicon Errata* (SPRZ272)

The following 281x errata have been fixed:

- **Analog-to-Digital Converter (ADC)**
  - ADC - EOS BUF1/2 bits in ADCST corrupted at the end of conversion of sequencer when INT MOD SEQ1/2 is enabled
  - ADC - Reserved bits in autosequence status register (ADCASEQSR)
  - ADC - Result register update
  - ADC - Sequencer reset while dual sequencers are running
- **Enhanced Controller Area Network (eCAN)**

  If contention existed between the CPU and the eCAN controller for access to certain eCAN register areas, then a CPU read may erroneously read all zeros (0x00000000) and a CPU write may fail to execute.

- **Logic Level for XCLKIN Pin**

  On 281x devices, when using an external oscillator to clock the device, the input level of the clock could not exceed V_{DD} rather than the 3.3-V I/O voltage. On the 2833x/2823x devices, a separate XCLKIN pin has been provided to allow for a 3.3-V external input clock. The X1 pin remains as is and can be used along with X2 to connect a crystal.
- **Serial Peripheral Interface (SPI) Slave Mode**

  On the 281x, when in slave mode, the SPI does not synchronize received words based on $\overline{\text{SPISTE}}$; therefore, a spurious clock pulse on SPICLK could throw the data stream out of sync. This has been corrected and when the SPI port is configured for slave mode, a high-to-low transition on the $\overline{\text{SPISTE}}$ signal always resets the bit counter state machine so that it is re-synchronized on every word transfer.
- **Watchdog Timer Reset Flag**

  The watchdog flag (WDFLAG) is used to determine if a reset is caused by the watchdog or an external reset. On the 281x devices, this flag is not reliable since the sampling window for the reset line is too short. On the 2833x/2823x devices, the sampling interval has been increased to allow more time for the reset line to go high after a watchdog reset occurs.
- **SCI - Bootloader Does Not Clear the ABD Bit After Auto-Baud Lock**

14 References

- http://www.ti.com
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- TMS320F280x, TMS320C280x, and TMS320F2801x DSC Silicon Errata (SPRZ171)
- *C28x FPU Primer* (SPRAAN9)
- *TMS320C28x CPU and Instruction Set Reference Guide* (SPRU430)
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- *C2833x/C2823x C/C++ Header Files and Peripheral Examples* (SPRC530)
- *C28x FPU Fast RTS Library* (SPRC664)
- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811,TMS320C2812 Digital Signal Processors Data Manual* (SPRS174)
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- *TMS320x281x DSP System Control and Interrupts Reference Guide* (SPRU078)
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- *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (SPRU566)
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- *TMS320x2833x, 2823x Direct Memory Access (DMA) Reference Guide* (SPRUFB8)
- *TMS320x28xx, 28xxx Inter-Integrated Circuit (I2C) Reference Guide* (SPRU721)
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- *TMS320x2833x Multichannel Buffered Serial Port (McBSP) Reference Guide* (SPRUFB7)
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