Application Report
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TMS320DM642 to TMS320DM6437 Migration Guide

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ABSTRACT

This document describes device considerations for migrating a design based on a TI TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor (DSP) to one based on a TI TMS320DM6437 Digital Media Processor (DMP). These two devices are based on similar DSP CPU cores, and feature video front- and back-end processing capability, and a similar mixture of memory and other peripherals useful in a system environment. This document describes the details of the considerations of concern for performing this migration.

Note that since this document describes migration from a TMS320DM642 device to a TMS320DM6437, familiarity with the TMS320DM642 device and its documentation is assumed.

Also note that all of the documentation referenced in this migration guide can be found on the TI website located in the two devices' respective product folders. The device product folders are found at the following two web pages:

- http://focus.ti.com/docs/prod/folders/print/tms320dm6437.html
- http://focus.ti.com/docs/prod/folders/print/tms320dm642.html

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1 Basic Feature Comparison

Table 1 shows a comparison of the basic features of the TMS320DM642 and the TMS320DM6437. The remainder of this document presents a comparison of these features in greater detail, and also provides references to the appropriate documentation for further information.

Table 1. Basic DM642/DM6437 Feature Comparison

Feature		DM642	DM6437
DSP CPU Core		C64x™	C64x+
Speeds		500/600/720 MHz	400/500/600 MHz
Endianness		Big/Little	Little
Memory	Cache: L1P	16K bytes	32K bytes
	Cache: L1D	16K bytes	80K bytes
	Cache: L2	256K bytes	128K bytes
	ROM		64K bytes
Peripherals	Video Ports	3 x input or output	1 front end, 1 back end
	VIC Port	1	
	Parallel EMIF	1	1
	DDR2 EMIF		1
	EDMA	EDMA 2.0 - 64 ch	EDMA 3.0 - 64 ch
	PCI	32 bits, v2.2	32 bits, v2.3
	Serial Ports	McASP	McASP
		McBSP x 2	McBSP x 2
	PLL	1	2
	UARTs		2
	Timers	3 × 32-bits	2 × 64 bits
	Watchdog Timer		1 × 64 bits
	EMAC	1	1
	I2C	1	1
	HECC		1
	VLYNQ		1
	HPI	16/32 bit	16 bit
	PWM		3
	GPIO	16	111
Power Supplies		2	3
Packages		548-pin BGA	361/376-pin BGA

2 DSP CPU Considerations

2.1 DSP CPU Core

Both the TMS320DM642 and the TMS320DM6437 utilize a TMS320C64x™ core DSP CPU, therefore, they both offer similar features and architecture. However, the DM6437 utilizes an enhanced version of the DSP CPU core, designated the TMS320C64x+, which implements numerous additional features not found in the earlier DSP CPU. Accordingly, the DM6437 offers capabilities beyond those found on the DM642. In particular, the C64x+ architecture adds several new instructions and features giving you improved performance for operations used in video applications and other general purpose algorithms.

The C64x+ DSP core is based on the C64x DSP core, and most C64x software executes properly on the C64x+ after being recompiled for the enhanced core and after being adjusted for memory map differences. For detailed information regarding the differences between the two DSP cores, see the *TMS320C64x to TMS320C64x+ CPU Migration Guide* (SPRAA84). For additional information, see the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732).

Note that differences between the two core CPUs exist in the following areas that may affect existing code:

- Instruction Set
- Registers
- Interrupts
- DMA Operations
- Timing Changes
- Circular Addressing

The following are among the new enhancements added to the C64x+ DSP core CPU in order to realize performance improvements on this new architecture:

- New instructions to support increased code efficiency and speed
- New 16-bit compact instructions to support increased code density
- New SPLOOP facility to provide improved code compactness and interruptibility for pipelined loops
- Changes to internal memory to increase the flexibility of internal memory usage
- New privilege modes to support secure operating systems
- New support for exceptions to provide improved error handling capabilities

2.2 DSP CPU Clock Speeds

The DM642 and DM6437 both offer a variety of different speed versions to accommodate a range of different performance requirements.

Table 2 shows a summary of the different speed versions of the DM642 and DM6437.

Table 2. Available Performance Versions of the DM642 and DM6437

DM642	DM6437
500 MHz (2.00 ns cycle time)	400 MHz (2.50 ns cycle time)
600 MHz (1.67 ns cycle time)	500 MHz (2.00 ns cycle time)
720 MHz (1.39 ns cycle time) (1)	600 MHz (1.67 ns cycle time)

(1) Commercial temperature range only

Note that power supply voltage requirements are different on these devices for some of the different speed versions. See Section 10 of this document for detailed information regarding power supply voltage requirements for the DM642 and DM6437.

For additional detailed information regarding performance, timing requirements and characteristics for the DM6437, see the *TMS320DM6437 Digital Media Processor Data Manual* (SPRS345).

2.3 Endianness Considerations

The DM642 is capable of functioning in either big-endian or little-endian operating mode. The DM6437, on the other hand, functions only in little-endian operating mode. Accordingly, software running in big-endian mode on the DM642 that is to be ported to the DM6437 frequently needs to be modified and recompiled in little-endian mode. Also, some peripheral modules have their own unique endianness considerations; therefore, for each peripheral used in a DM6437 application, the peripheral user's guide should be consulted for any specific endianness considerations for that peripheral.

3 Internal Memory Comparisons

Both the DM642 and the DM6437 feature on-chip internal memories, allowing efficient handling of varied partitions of internal program and data information. Both devices feature several different types of cache memory, allowing significant flexibility in using this memory to enhance algorithm performance. In addition, the DM6437 offers an on-chip ROM, which contains the bootloader program. Since there are some differences between the memory architectures on the two devices, some software modifications are required when migrating from the DM642 to the DM6437.

Table 3 shows a comparison of the DM642 and the DM6437 internal memory.

Table 3. Internal Memory Comparison

Memory Type	DM642	DM6437
L1P Program Memory	16K-bytes cache (direct mapped)	32K-bytes RAM/cache (direct mapped), flexible allocation
L1D Data Memory	16K-bytes cache (2-way set associative)	80K-bytes RAM/cache (2-way set associative), flexible allocation
L2 RAM Memory	256K-bytes unified mapped RAM/cache (4-way set associative), flexible allocation	128K-bytes unified mapped RAM/cache (4-way set associative), flexible allocation
ROM	Not implemented	64K-bytes

For additional detailed information regarding use of the DM6437's internal memory, see the *TMS320C64x+ DSP Cache User's Guide* (SPRU862).

4 Peripherals

The TMS320DM642 and TMS320DM6437 both feature a wide variety of peripheral modules which are useful in many different system environments. This section presents a comparison of the peripheral offerings on these two devices.

4.1 Video Ports and VIC (VCXO Interpolated Control) Port

The DM642 and DM6437 both feature video processing peripherals which can accept video input, and can generate video output. The DM642 has three video ports, each of which can be programmed for either video input or video output. The DM642 also features a VCXO Interpolated Control (VIC) port. The DM6437 provides a video processing subsystem consisting of an input video processing front end (VPFE), and an output video processing back end (VPBE). Therefore, each device can, functionally, accept a video input stream, and generate a video output stream.

In addition, the DM642 has the capability to accept up to three video input streams, or to generate up to three video output streams, or a combination thereof, depending on how each of its three video ports is programmed. Since the DM6437 has only one video front end and one video back end, this device can only process one video input stream and one video output stream. Accordingly, if simultaneous processing of more than one video input or output stream is necessary with a DM6437, additional external hardware is generally required.

The VIC port on the DM642 provides an output which can be used to adjust the frequency of the system clock to establish clock synchronization in TSI capture mode video applications. The DM6437 does not feature a dedicated VIC port; however, this function can be implemented in a DM6437 system using a pulse-width modulator (PWM) output and a timer input.

Since the video ports on the DM642 and the DM6437 are significantly different in functionality and capabilities, system hardware and software modifications are necessary when migrating the video processing aspects of an application from the DM642 to the DM6437.

For detailed information regarding use of the video ports on the DM6437, see the *TMS320DM643x DMP Video Processing Front End (VPFE) User's Guide* (SPRU977) and the *TMS320DM643x DMP Video Processing Back End (VPBE) User's Guide* (SPRU952).

4.2 External Memory Interface (EMIF)

Both the DM642 and the DM6437 feature flexible external interfaces which support accessing various types of memory devices. The specific external memory interfaces used by the two devices are implemented differently, however. On the DM642, a single 64-bit external memory interface is used for all types of memory supported. On the DM6437, two separate external memory interfaces are used – one dedicated to DDR2 memory, and a second interface for asynchronous memories.

Therefore, when architecting an external memory interface for a DM6437 system, a different approach is generally used than with the DM642. Instead of having only one external memory interface bus for all devices, the DM6437 can partition accesses on two separate memory interfaces, allowing for improved efficiency and throughput.

On the DM6437, the DDR2 interface utilizes a 32-bit data bus, and is optimized for use with high-speed, high-density DDR2 memory for storage of programs and large blocks of data. The asynchronous memory interface uses an 8-bit data bus, and is designed for slower special-purpose memory such as SRAM and flash memory.

Table 4 summarizes the characteristics of the DM642 and DM6437 external memory interfaces.

Table 4. External Memory Interface Features

	Features	DM642	DM6437
1	Data Width	64 bits	32 bits
	Memory Types	Sync/Async	DDR2
	Address Range	1024 Mbytes	256 Mbytes
2	Data Width	Not implemented	8 bits
	Memory Types	Not implemented	Async (1)
	Address Range	Not implemented	64 Mbytes

(1) Memory types include SRAM, flash, etc.

For detailed information regarding use of the DDR2 and asynchronous memory interfaces on the DM6437, see the *TMS320DM643x DMP DDR2 Memory Controller User's Guide* (SPRU986) and the *TMS320DM643x DMP Asynchronous External Memory Interface (EMIF) User's Guide* (SPRU984).

4.3 EDMA Controllers

The DM642 and the DM6437 both feature enhanced direct memory access (EDMA) controllers which can be used to transfer data to and from numerous locations, both on- and off-chip. Both devices support 64 independent channels of EDMA transfers.

The DMA controllers used on these two devices are functionally similar, however, the DM642 uses version 2.0 of the EDMA controller, and the DM6437 uses version 3.0 of the EDMA controller. Migration from EDMA 2.0 to EDMA 3.0 is discussed in detail in the *EDMA v3.0 (EDMA3) Migration Guide for TMS320DM644x DMSoC* (SPRAAA6).

For detailed information regarding the use of EDMA on the DM6437, see the *TMS320DM643x DMP Enhanced DMA (EDMA) Controller User's Guide* (SPRU987).

4.4 Peripheral Component Interconnect (PCI) Interface

Both the DM642 and the DM6437 feature an integrated peripheral which is compatible with the industry-standard peripheral component interconnect (PCI) interface. The PCI interfaces on these two devices are similar in function and pinout; however, the DM642 PCI interface complies with version 2.2 of the PCI specification, and the DM6437 PCI interface complies with version 2.3 of the PCI specification. Also, the DM642 PCI runs at a maximum of 66 MHz, and the DM6437 PCI runs at a maximum of 33 MHz. Accordingly, use of these two peripherals is different, and therefore, migrating an application from a DM642 to a DM6437 requires software and hardware interconnection changes.

For detailed information regarding the use of the PCI interface on the DM6437, see the *TMS320DM643x DMP Peripheral Component Interconnect (PCI) User's Guide* (SPRU985).

4.5 Serial Ports

The DM642 and DM6437 each feature one McASP serial port and two McBSP serial ports. These serial ports can be used to interface to a variety of external devices including codecs, communications peripherals, and other processors.

4.5.1 McASP Serial Port

The McASP serial port on the DM642 and the DM6437 is the same peripheral module on both of these devices. The only functional difference between the two McASP modules is that there are eight serializer on the DM642 and four on the DM6437. The only other differences in usage between these devices are the base addresses of the memory mapped registers, signal locations within the device pinouts, and pin multiplexing selection. Otherwise, use of these peripherals translates directly between these two devices. For detailed information regarding the use of the McASP on the DM6437, see the *TMS320DM643x DMP Multichannel Audio Serial Port (McASP) User's Guide* (SPRU980).

4.5.2 McBSP Serial Ports

The DM642 and DM6437 both feature two McBSP serial ports. The McBSP peripheral modules on these two devices are different versions of this peripheral, hence some differences exist in their functionality. These differences, however, are somewhat subtle, and, other than differences in signal locations within the device pinouts, and pin multiplexing selection, the basic high-level functionality of these peripherals is quite similar. Both modules have the same basic memory mapped control registers and base address offsets, and both modules have the same I/O pins. Note that the base addresses of the memory mapped control registers are different on these two devices.

For detailed information regarding the use of the McBSP on the DM6437, see the *TMS320DM643x DMP Multichannel Buffered Serial Port (McBSP) User's Guide* (SPRU943).

4.6 Phased-Locked Loop (PLL)/Clock Generators

Both the DM642 and the DM6437 feature clock generators with PLLs that are used to generate clocks for these devices.

The DM642 clock generator has one PLL which can be used to generate a variety of different clocks from the device input clock. The PLL can multiply the input clock by 1, 6 or 12, based on the state of two input pins, and the resultant clock is then divided by 1, 2, 4, and 8. These clocks are then used to satisfy the clocking requirements for the different parts of the DM642 device. Additionally, on the DM642, there is the option to use a separate external input signal to provide clock for the EMIF.

On the DM6437, the clock generator has two PLLs - PLL1 and PLL2. Each of these PLLs also supports a number of multiply and divide configurations, allowing the device to generate a number of different clock frequencies to satisfy a wide variety of system requirements.

With PLL1, the input clock may be multiplied by 1 or any value from 14 to 30, programmable through software, and the resultant clock is then divided by programmable values between 1 and 32 to produce three system clocks. These three clocks are then used to clock the DSP, the DMA and the VPFE.

PLL2 can also multiply the input clock by 1 or any value from 14 to 32, and the resultant clock is then divided by programmable values between 1 and 32 to produce two output clocks. These two clocks are then used to satisfy the clocking requirements of the DDR2 interface and the VPBE on the device.

Table 5 summarizes the PLL/clock generator features on the DM642 and the DM6437.

Table 5. PLL/Clock Generator Comparison

PLL	Feature	DM642	DM6437
PLL1	Multipliers	1,6,12	1,14-30
	Dividers	1,2,4,8	1-32, default 1,3,6 (1)
	Destinations	All(2)	DSP, DMA, VPFE
PLL2	Multipliers	Not implemented	1,14-32
	Dividers	Not implemented	1-32, default 2,10
	Destinations	Not implemented	DDR2, VPBE

(1) Programmed values must maintain 1:3:6 frequency ratio.
(2) An optional external clock may be supplied for the EMIF.

For information regarding initialization of the PLL/clock generators, see Section 8 of this document. For additional detailed information regarding use of the PLL/clock generator on the DM6437, see the *TMS320DM643x DMP DSP Subsystem Reference Guide* (SPRU978) and the *TMS320DM6437 Digital Media Processor* (SPRS345).

4.7 UARTs

While the DM642 does not feature the universal asynchronous receiver/transmitter (UART) peripheral, the DM6437 has two, therefore this added capability can be utilized in DM6437 systems. The UART peripherals can be used for serial asynchronous communication between the DM6437 and other devices in the system. On the DM6437, the first UART, UART0, features flow control capability using the RTS and CTS signals, whereas the second UART, UART1, does not implement this capability. For detailed information regarding use of the UART peripherals on the DM6437, see the *TMS320DM643x DMP Universal Asynchronous Receiver/Transmitter (UART) User's Guide* (SPRU997).

4.8 Timers

The DM642 and DM6437 both feature several timers. The DM642 includes three 32-bit general purpose timers. The DM6437 includes two 64-bit general purpose timers, and one watchdog timer. Additionally, the two 64-bit timers on the DM6437 can also be used as four 32-bit timers.

4.8.1 General-Purpose Timers

Since capability of the general-purpose (GP) timers on the DM642 and DM6437 is somewhat different, migrating an application to the DM6437 requires some software modifications; however, because the DM6437 timers can be operated as four 32-bit timers, timer requirements of a DM642 application can easily be supported by the DM6437.

The DM6437 general-purpose timers actually support three modes of operation: a 64-bit general-purpose timer, dual unchained 32-bit GP timers, or dual chained 32-bit timers. The GP timer modes can be used to generate periodic interrupts, EDMA synchronization events, or external clock output.

Configuring the DM6437 timers in 32-bit unchained mode allows straightforward migration of DM642 timer requirements to this device. Although configuration and pinouts differ, the timer capabilities of the DM6437 map well to support the timer requirements of a DM642 application.

Table 6 presents a comparison between the timers on the DM642 and the DM6437, when the DM6437 timers are partitioned in 32-bit mode.

Table 6. DM642 and DM6437 Timer Comparison

Timer Feature	DM642	DM6437
Number of 32-bit timers	3	4
Number of possible timer events	3	4
Number of separate clock inputs	2	2
Number of separate timer outputs	2	2

For detailed information regarding use of the DM6437 general purpose timers, see the *TMS320DM643x DMP 64-Bit Timer User's Guide* (SPRU989).

4.8.2 Watchdog Timer

The DM6437 features a watchdog timer, while the DM642 does not, therefore, the DM6437 systems may benefit from this added functionality. The watchdog timer can be extremely useful, especially in real-time systems, to allow the capability recover in case of unexpected events which might otherwise cause the system to stop functioning properly.

The DM6437 watchdog timer is 64 bits long, and allows the capability to interrupt or reset the device if the watchdog timer is not serviced at a programmable interval set up by you. For detailed information regarding use of the DM6437 watchdog timer, see the *TMS320DM643x DMP 64-Bit Timer User's Guide* (SPRU989).

4.9 Ethernet MAC

The DM642 and the DM6437 both feature peripherals which provide Ethernet interface capability. Both of these devices provide support for the IEEE 802.3 compliant 10/100 Mb/s Ethernet interface.

The Ethernet interface on these devices is comprised of the Ethernet media access controller (EMAC) and the physical layer (PHY) device management data input/output (MDIO) module.

The EMAC controls the flow of packet data from the DSP to the PHY while the MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the DSP through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to control device reset, interrupts, and system priority.

On the DM642 and the DM6437, the Ethernet interface pins are functionally the same, however, there are differences between the two EMAC and MDIO peripheral modules. The control registers of each are similar but not identical; therefore, software changes are required in order to migrate from a DM642 to a DM6437.

For detailed information regarding use of the DM6437 Ethernet interface, see the *TMS320DM643x DMP EMAC/MDIO User's Guide* (SPRU941).

4.10 Inter-Integrated Circuit (I2C) Interface

Both the DM642 and the DM6437 feature an interface to I2C-compatible external devices. The basic I2C functionality provided by the DM642 and the DM6437 is the same, however, the actual I2C peripheral module and register set are different between these two devices. Therefore, you should refer to the DM6437 I2C documentation for information about using this peripheral.

Use of the DM6437 I2C peripheral is described in detail in the *TMS320DM643x DMP Inter-Integrated Circuit (I2C) Module User's Guide* (SPRU991).

4.11 High-End CAN Controller (HECC)

While the DM642 does not feature the HECC peripheral, the DM6437 does, therefore this added capability can be utilized in DM6437 systems. The HECC peripheral uses a serial multimaster communication protocol that efficiently supports distributed real-time control, with a very high-level of security, and a communication rate of up to 1 Mbps. The HECC bus is ideal for applications operating in noisy and harsh environments, such as in the automotive and other industrial fields that require reliable communication or multiplexed wiring. For detailed information regarding use of the HECC peripheral on the DM6437, see the *TMS320DM643x DMP High-End CAN Controller (HECC) User's Guide* (SPRU981).

4.12 VLYNQ Interface

The DM6437 features a VLYNQ interface, while the DM642 does not, therefore, DM6437 systems may benefit from this added functionality. The VLYNQ communications interface port is a low pin count, high-speed, point-to-point serial interface used for connecting to host processors and other VLYNQ compatible devices. This interface can be implemented in either a host-to-peripheral or peer-to-peer fashion.

The VLYNQ port is a full-duplex serial bus where transmit and receive operations occur separately and simultaneously without interference. VLYNQ enables the extension of an internal bus segment to one or more external physical devices. The external devices are mapped to local physical address space and appear as if they are on the internal bus of the DM6437. The external devices must also have a VLYNQ interface.

VLYNQ uses a simple block code (8b/10b) packet format and supports in-band flow control so that no extra terminals are needed to indicate that overflow conditions might occur. The external device can also initiate read and write transactions.

For detailed information regarding use of the VLYNQ peripheral on the DM6437, see the *TMS320DM643x DMP VLYNQ Port User's Guide* (SPRU938).

4.13 HPI Interface

Both the DM642 and the DM6437 feature the host port interface (HPI) peripheral through which an external host can communicate with the DSP device. Through the HPI, the host can access most internal memory and memory mapped resources, with only a few exceptions. The host functions as the master of this interface, which greatly increases flexibility of communications with the DSP device.

The HPI interfaces used on these two devices are similar in function and pinout, however, the DM642 and the DM6437 contain different versions of the HPI module. Because of this, use of these two peripherals is different, and therefore, migrating an application from a DM642 to a DM6437 requires software and hardware interconnection changes.

Specifically, between these two HPI modules, control registers and their bit assignments are different, and the DM642 supports 16- or 32-bit data transfers, while the DM6437 supports only 16-bit transfers. In addition, the DM6437 provides FIFOs in the data path, while the DM642 does not, and the HCNTL bit decoding is different on the two devices, which is extremely critical in properly implementing communications with the host device.

One other difference between these two HPI modules is in the way the two LSBs of the HPIA register are handled. On the DM642, these two bits are always zero, no matter what value is loaded. On the DM6437, these two bits must be explicitly loaded with zero for the address to be correctly interpreted.

Table 7 below summarizes some of the most significant differences between these two HPI modules.

Table 7. HPI Interface Feature Comparison

Feature		DM642	DM6437
Data Bus Width		16 or 32 bits	16 bits
DMA Data Transfer		Yes	Yes
FIFOs		No	Yes - 8 x 32-bits
Two LSBs of HPIA		Always zero	Must be loaded with zeros
HCNTL Bit Decoding[1]	HCNTL[1:0]=01	HPIA access	HPID access, autoincrement
	HCNTL[1:0]=10	HPID access, autoincrement	HPIA access

(1) Other states of HCNTL bits are the same between devices.

For detailed information regarding the use of the HPI interface on the DM6437, see the *TMS320DM643x DMP Host Port Interface (HPI) User's Guide* (SPRU998).

4.14 Pulse-Width Modulator (PWM) Outputs

While the DM642 does not feature dedicated PWM outputs, the DM6437 does, therefore this added capability can be utilized in DM6437 systems. Three programmable PWM outputs are provided.

The DM6437 PWM outputs provide the capability to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. Each PWM output is implemented as a timer with a period counter and a first-phase duration comparator, where the bit width of the period and first-phase duration are both programmable. The period and the first-phase duration are controlled with 32-bit counters, and each PWM output can also be used to generate an interrupt and/or EDMA sync event.

For detailed information regarding use of the PWM output capabilities on the DM6437, see the *TMS320DM643x DMP Pulse-Width Modulator (PWM) User's Guide* (SPRU995).

4.15 General Purpose I/O (GPIO)

Both the DM642 and the DM6437 feature a selection of pins that can be configured to provide independent single-bit general-purpose digital I/O. Since the GPIO configuration differs between these two devices, software modifications are necessary in order to migrate from the DM642 to the DM6437.

Specifically, the DM642 features 16 GPIO bits, while the DM6437 features 111 GPIO bits. These GPIO bits can be used to interface to external signals, and to generate interrupts.

On both devices, many GPIO pins are multiplexed with other pin functions; therefore, GPIO pin availability depends on what other functions are used on the device. See Section 9 of this document for additional information regarding pin multiplexing on the DM6437.

For detailed information regarding the use of GPIO on the DM6437, see the *TMS320DM643x DMP General-Purpose Input-Output User's Guide* (SPRU988).

5 Interrupt Considerations

The DM642 and the DM6437 both support servicing of a wide range of interrupts from a variety of sources, both on- and off-chip. Each device uses its own multiplexing scheme to select the specific sources that will actually be allowed to interrupt the CPU.

The DM642 accepts a total of 16 independent interrupt inputs to the CPU, but allows these interrupts to be chosen from a possible selection of 32 sources in addition to four interrupts which are always selected, allocated to reset, NMI, and two reserved interrupts. The 32 possible interrupt sources are mapped to 12 independent interrupts using the MUXH and MUXL registers. The resultant 16 interrupt signals are sent to the CPU. The polarities of the selected input signals which will actually generate interrupts are programmable through the EXTPOL register.

The DM6437 also accepts a total of 16 possible independent interrupt inputs to the CPU, although some of these are not used. On this device, sources that are allowed to interrupt the CPU may be chosen from a possible selection of 128 system events, in addition to three interrupts which are always selected, allocated to reset, NMI, and a hardware exception interrupt. The 128 possible system events are mapped to 12 independent interrupts using the interrupt selector, interrupt combiner, and exception combiner modules. The resultant 15 interrupt signals are sent to the CPU. Some of the possible interrupts on the DM6437 can be generated from GPIO signals, and the polarities of these signals used to generate the interrupts are programmable through the GPIO control registers.

Table 8 presents a comparison of the interrupt capabilities of the DM642 and the DM6437 devices.

Table 8. Interrupt Capability Comparison

Feature	DM642	DM6437
Total interrupts to CPU	16	15
Fixed	4: Reset, NMI, 2 reserved	3: Reset, NMI, H/W exception
Programmable	12	12
Total number of sources	32	128
Source selected by	MUXH, MUXL register bits	Interrupt selector, interrupt/exception combiners
Programmable polarity	Yes, through EXTPOL register	GPIO only, through GPIO control registers

For detailed information regarding handling of interrupts on the DM6437, see the *DM6437 Digital Media Processor* (SPRS345), the *TMS320DM643x DMP DSP Subsystem Reference Guide* (SPRU978) and the *TMS320C64x+ Megamodule Reference Guide* (SPRU871).

6 Bootloading Capabilities

The DM642 and the DM6437 both provide the capability to transfer code from an external location into RAM to be executed following reset.

On both devices, the states of various input pins are sampled following reset, and the selected boot modes are determined based on these states.

The DM642 provides three boot modes – host boot through PCI or HPI, EMIF boot, and no boot. These boot modes are selected by the state of the AEA[22:21] and PCI_EN pins following reset. In the host boot mode, the host device serves as the master for the bootload operation. In the EMIF boot mode, the DMA controller automatically copies 1 K of data from the CE1 space to internal memory starting at location zero. The DM642 does not contain a bootloader program.

The DM6437 provides four basic bootloading capabilities – host boot through PCI or HPI, asynchronous EMIF boot, serial boot through I2C, serial peripheral interface (SPI) or UART, and EMU or no boot. In addition, the DM6437 offers a *fast boot* selection which allows for various options for speeding up the DSP clock frequency during the bootload process, allowing for faster bootload times. The fast boot option can use either fixed or user-selected PLL multipliers for determining clock frequency. On the DM6437, the bootloading function is performed by the bootloader program located in internal ROM on the device.

Table 9 below shows a comparison of the bootloading capabilities of the DM642 and the DM6437.

Table 9. Bootloading Capabilities

Feature		DM642	DM6437
Number of Modes		3	Many: 4 basic types + fast boot options
Modes	Host (HPI/PCI)	Yes	Yes
	EMIF	Yes	Yes
	No boot	Yes	Yes ("EMU boot")
	Serial	No	Yes - I2C, SPI, UART
Selected by		AEA[22:21]	BOOTMODE[3:0]
		PCI_EN	PCIEN
			AEM[2:0]
			PLLMS[2:0]
			FASTBOOT

For detailed information regarding use of the bootloader on the DM6437, see the *Using the TMS320DM643x Bootloader Application Report* (SPRAAG0).

7 Power Management

In most DSP systems, power management is an important concern to allow DSP functions to be performed with the lowest power cost and minimal battery drain possible. The DM642 and the DM6437 both offer several options for power management.

On the DM642, there are three basic options for power management. The first involves peripherals that are enabled and disabled depending on the state of external input pins. These peripherals are the PCI, the HPI and the EMAC. The state of the PCI_EN, MAC_EN and HD5 pins determines which of these peripherals is enabled.

The second power management option is controlled by the bits in the peripheral configuration (PERCFG) register. This register contains bits which can be used to enable or disable the McASP, McBSP, video port, and I2C peripherals. The third power management option on the DM642 is controlled by bits in the control status register (CSR). These bits can be used to selectively enable or disable the CPU, peripherals, or PLL.

On the DM6437, there are five basic categories of power management options, and many different variations of these options within these basic categories.

To manage power in the circuitry of the various peripherals and functional modules within the DM6437, the dedicated power and sleep controller (PSC) module implements the capability to turn on or off the clock to each module, therefore controlling power usage on a module by module basis. The PSC is made up of the global PSC (GPSC) module, which contains memory mapped registers, PSC interrupt control, and a state machine for each peripheral/module, and the local PSCs (LPSCs) for each peripheral/module controlled.

In order to efficiently manage power due to I/O buffers on the device, the DM6437 also provides the capability to power up or down various groups of I/O pin buffers. This feature is controlled by writing to bits in the VDD3P3V_PWDN register. Note that the VDD3P3V_PWDN register controls only the power supply to the 3.3 V I/O buffers for each designated group of pins. The PSC controls enabling or disabling of the clock for each module.

In addition, the DM6437 also offers several options for managing power within the C64x+ DSP CPU core. These capabilities are implemented by various instructions and control registers within the DSP CPU, and control power within the CPU and internal memories.

Finally, the DM6437 provides the capability to enable or disable the PLL in software through the PLLCTL register, and to enable or disable the video DACs through the video port VPBE VENC VMOD and DACTST registers.

Table 10 and Table 11 summarize the power management options available on the DM642 and the DM6437.

Table 10. DM642 Power Management Options

Option	Controlled By	Controls
A	Input pins PCI_EN, HD5, MAC_EN	PCI, HPI, EMAC
B	PERCFG register bit settings	McASP, McBSP, VP0-2, I2C
C	CSR register bit settings	CPU and/or peripherals and/or PLL

Table 11. DM6437 Power Management Options

Option	Controlled By	Controls
A	GPSC/LPSC registers	Individual peripherals/modules
B	VDD3P3V_PWDN register	3.3 V I/O pin group buffers
C	Various instructions/control registers	DSP CPU core + memory
D	PLLCTL register	PLL
E	VMOD/DACTST registers	Video DACs

For detailed information regarding power management on the DM6437, see the *TMS320DM6437 Digital Media Processor* (SPRS345), the TMS320DM643x DMP DSP Subsystem Reference Guide (SPRU978), and the *TMS320C64x+ Megamodule Reference Guide* (SPRU871).

8 PLL/Clock Mode at Reset

Both the DM642 and DM6437 feature flexible clock generators which provide clocking to satisfy a wide variety of system requirements. In order to properly start up and initialize a DSP system, the clock generator must be able to provide appropriate clock signals to the device even before the device is released from reset. Both the DM642 and DM6437 clock generators are designed to provide this capability.

The DM642 has two clock mode pins (CLKMODE[1:0]) that are used to select the clock mode at reset. These two pins select between a multiply by 1, 6, or 12 of the device input clock, the result of which is then used to provide clocks to the device until this selection is changed and the device is reset again. On the DM642, the input clock frequency range is 30-75 MHz.

The DM6437 can be clocked either by an external oscillator, or using a crystal with the internal oscillator. The internal oscillator is enabled by default when reset is asserted, but can be disabled through software by writing to the PLLCTL register, if desired. The default clock mode for the DM6437 at reset is a multiply by 1 of the input clock. Once the device is released from reset, the clock frequency can be changed through software by writing to registers in the PLL module. See Section 4.8 of this document for additional information regarding considerations of PLL operation. The input clock frequency range on the DM6437 is 20-30 MHz.

Table 12 presents a comparison of the DM642 and DM6437 PLL and clock mode initialization.

Table 12. Comparison of PLL/Clock Modes at Reset

Features	DM642	DM6437
Input clock frequency range	30-75 MHz	20-30 MHz
On-chip oscillator	No	Yes (1)
Clock mode at reset	x1, x6 or x12	x1, oscillator enabled
Clock mode at reset determined by	CLKMODE[1:0] pins	Not variable (2)
S/W can change clock rate after reset	No	Yes

(1) Oscillator is on by default. Can be turned off in S/W after reset if desired.
(2) Bootloader may change clock frequency after reset. See Section 6.

For detailed information regarding PLL and clock mode initialization, see the *TMS320DM6437 Digital Media Processor* (SPRS345) and the *TMS320DM643x DMP DSP Subsystem Reference Guide* (SPRU978).

9 Pin Multiplexing

The DM642 and the DM6437 both use multiplexing of functions on various pins in order to maximize device features and flexibility, while minimizing pin count, and therefore package size and cost. Pin multiplexing is accomplished in a similar fashion on both devices, however, the actual implementation on each is different, therefore, software changes may be necessary, and the DM6437 documentation should be consulted for operational details.

Functionally, on both devices, the default pin multiplexing configuration is determined by the state of various input pins at reset, and the reset state of various register bits. Following reset, the pin multiplexing configuration can be modified through software by writing to various registers.

On the DM6437, the pin multiplexing configuration following reset is controlled through software using two dedicated registers called PINMUX0 and PINMUX1. Writing to these two registers can be used to modify the pin multiplexing configuration to suit a wide variety of system applications.

For detailed information regarding pin multiplexing and its control on the DM6437, see the *TMS320DM6437 Digital Media Processor* (SPRS345) and the device-specific User's Guides for the peripherals being used in the particular application in question.

In addition to the available device documentation, an interactive software utility is available to assist in determining the correct values to load into the PINMUX0 and PINMUX1 registers. Using the graphical user interface of this software utility, the desired peripheral mix can be selected from the possible configuration options on the device, and the software utility generates the PINMUX0 and PINMUX1 register settings. This software utility is available with the *TMS320DM643x Pin Multiplexing Utility* (SPRAAN3).

10 Power Supplies

The DM642 and the DM6437 both utilize multiple power supplies in order maximize flexibility and performance and minimize power dissipation, as well as to adhere to industry standards for various external interfaces. Additionally, the different clock speed versions of each device have different power supply voltage level requirements.

The DM642 utilizes an industry standard 3.3 V power supply for its I/O pins, and either a 1.2 V supply for the 500 MHz operation, or a 1.4 V supply for the DM642A and for the 600 and 720 MHz versions of the DM642.

The DM6437 also utilizes a 3.3 V supply for its I/O pins, and either a 1.2 V supply for 400, 500 or 600 MHz operation, or a 1.05 V supply for 400 MHz operation only. Additionally, the DM6437 also requires a 1.8 V supply for the DDR2 interface, and for the device PLLs.

Table 13 summarizes the power supply requirements for the DM642 and the DM6437.

Table 13. Power Supply Requirements

Supply		DM642			DM6437
Core	Speed (MHz)	500	A500/A600/600/720 (1)	400	400/500/600
	Voltage	1.2 V	1.4 V	1.05 V	1.2 V
I/O	Voltage	3.3 V	3.3 V	3.3 V	3.3 V
DDR2/PLLs	Voltage	N/A	N/A	1.8 V	1.8 V

(1) Axxx versions of the DM642 are extended temperature versions.

For additional detailed information regarding power supply requirements on the DM6437, see the *TMS320DM6437 Digital Media Processor* (SPRS345).

11 Package and Pin Count Comparisons

The DM642 and the DM6437 are both provided in cost-efficient, high density BGA packages. Since the two devices are provided in different packages, however, pin connections and locations are different between the two devices. Therefore, PC board layout and signal connection modifications are necessary when migrating from a DM642 to a DM6437 device.

Table 14 shows a comparison of the packages and pin counts for the DM642 and the DM6437.

Table 14. Package and Pin Count Comparison

Ball Pitch	DM642	DM6437
0.8 mm	548 pin ZDK (Pb-free) 548 pin GDK	361 pin ZWT (Pb-free)
1.0 mm	548 pin ZNZ (Pb-free) 548 pin GNZ	376 pin ZDU (Pb-free)

For additional detailed information regarding power supply requirements on the DM6437, see the *TMS320DM6437 Digital Media Processor* (SPRS345).

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