Application Report
SPRAAA7E–July 2008

Implementing DDR2 PCB Layout on the TMS320C6454/5

Michael Shust and Jeff Cobb — *High Speed HW Productization*

ABSTRACT

This application report contains implementation instructions for the DDR2 interface contained on the TMS320C6454/5 digital signal processor (DSP) device. The approach to specifying interface timing for the DDR2 interface is quite different than on previous devices.

The previous approach specified device timing in terms of data sheet specifications and simulation models. The system designer was required to obtain compatible memory devices, as well as the device-specific data sheets and simulation models. This information would then be used to design the printed circuit board (PCB) using high-speed simulation to close system timing.

For the C6454/5 DDR2 interface, the approach is to specify compatible DDR2 devices and provide the PCB routing rule solution directly. TI has performed the simulation and system design work to ensure DDR2 interface timings are met. This document describes the required routing rules.

The C6454/5 EVM provides an example of a PCB layout following these routing rules that passes FCC EMI requirements. You may copy the DDR2 portion of this layout directly, but the intent is to allow enough flexibility in the routing rules to meet other PCB requirements.

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1.1 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding guidelines for using this DDR2 specification, *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0).

1.1.1 DDR2 Interface Schematic

Figure 1 shows the DDR2 interface schematic for a x32 DDR2 memory system. The x16 DDR2 system schematic is identical except that the high word DDR2 device is deleted. Pin numbers for the C6454/5 can be obtained from the pin description section of the *TMS320C6454 Fixed-Point Digital Signal Processor Data Manual* (SPRS311) and the *TMS320C6455 Fixed-Point Digital Signal Processor Data Manual* (SPRS276). The DDR2 device pin numbers can be obtained from their device-specific data sheets.

1.1.2 Compatible JEDEC DDR2 Devices

Table 1 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-533 speed grade DDR2 devices.

Table 1. Compatible JEDEC DDR2 Devices

No.	Parameter	Min	Max	Unit	Notes
1	JEDEC DDR2 Device Speed Grade	DDR2-533			See Note (1)
2	JEDEC DDR2 Device Bit Width	x16	x16	Bits	
3	JEDEC DDR2 Device Count	1	2	Devices	See Note (2)
4	JEDEC DDR2 Device Ball Count	84	92	Balls	See Note (3)

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
(2) 1 DDR2 device is used for 16 bit DDR2 memory system. 2 DDR2 devices are used for 32 bit DDR2 memory system.
(3) 92 ball devices retained for legacy support. New designs will migrate to 84 ball DDR2 devices. Electrrically the 92 and 84 ball DDR2 devices are the same.

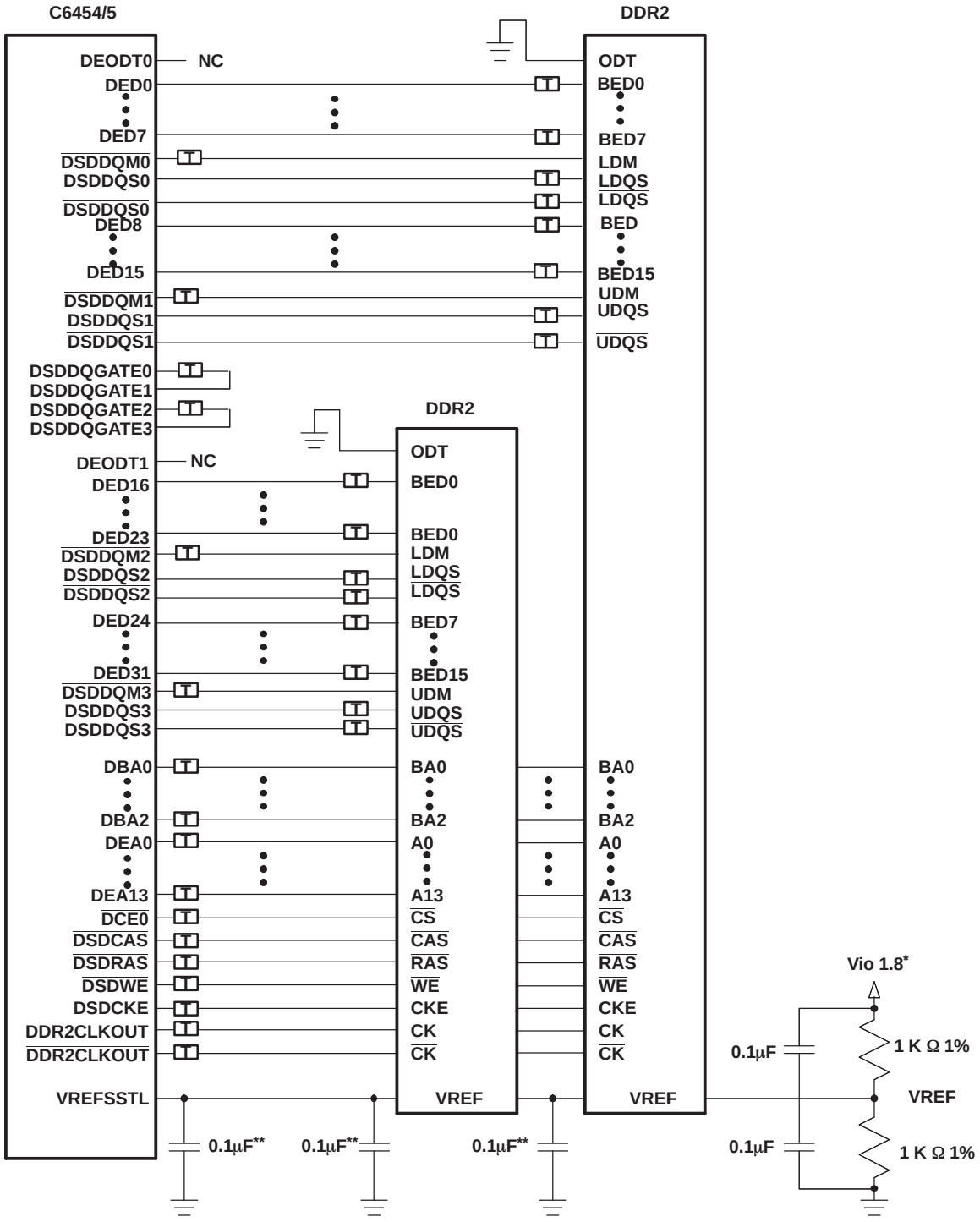
1.1.3 PCB Stackup

The minimum stackup required for routing the C6454/5 is a six layer stack as shown in Table 2. Additional layers may be added to the PCB stack up to accommodate other circuity or to reduce the size of the PCB footprint.

Table 2. C6454/5 Minimum PCB Stack Up

Layer	Type	Description
1	Signal	Top Routing Mostly Horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing Mostly Vertical

Complete stack up specifications are provided in Table 3.

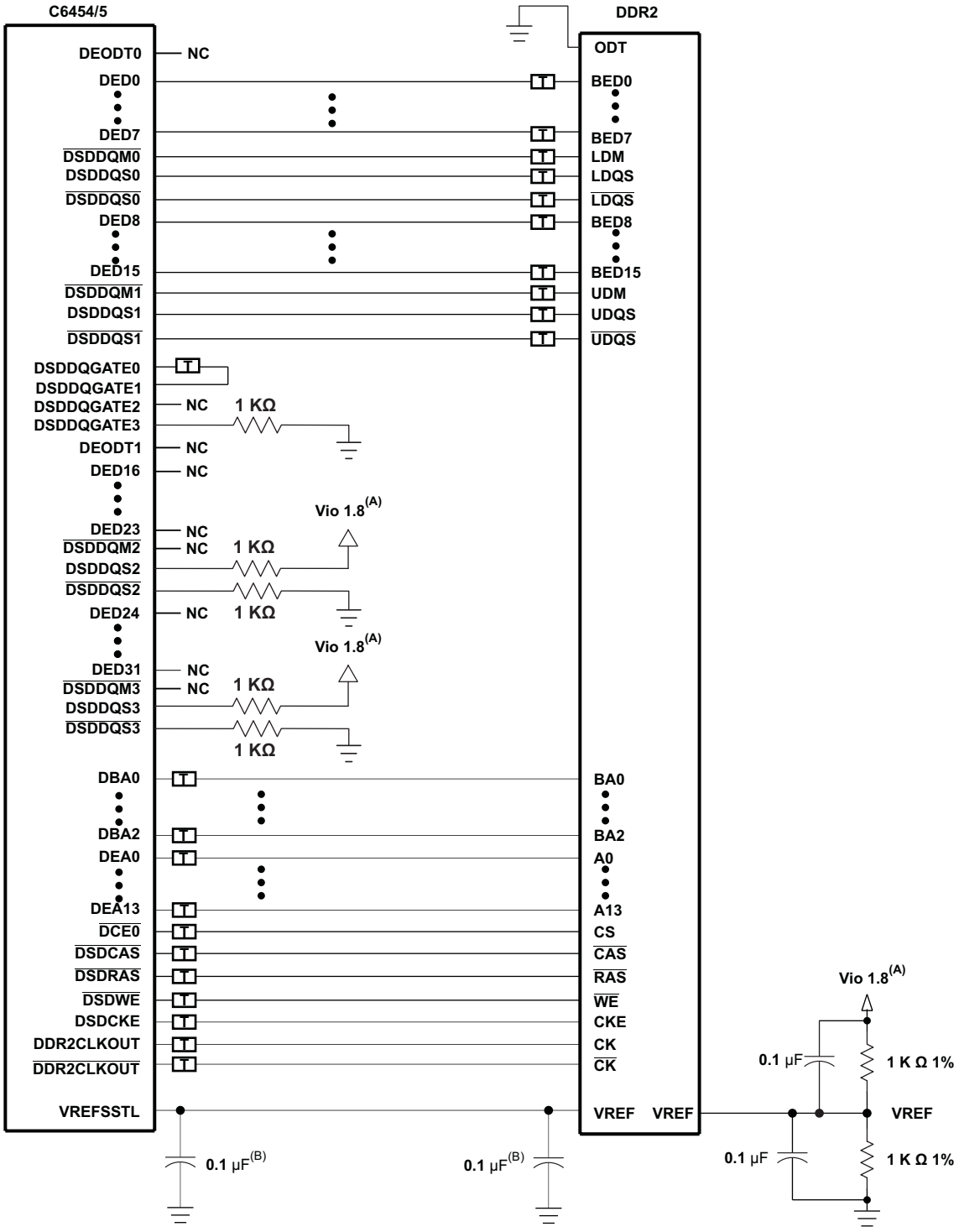


Terminator, if desired. See terminator comments.

* Vio1.8 is the power supply for the DDR2 memories and C6455 DDR2 interface.

** One of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin.

Figure 1. DM647/8 32-Bit DDR2 High Level Schematic



T Terminator, if desired. See terminator comments.

A Vio1.8 is the power supply for the DDR2 memory interface.

B One of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin.

Figure 2. DM647/8 16-Bit DDR2 High Level Schematic

Table 3. PCB Stack Up Specifications

No.	Parameter	Min	Typ	Max	Unit	Notes
1	PCB Routing/Plane Layers	6				
2	Signal Routing Layers	3				
3	Full ground layers under DDR2 routing Region	2				
4	Number of ground plane cuts allowed within DDR routing region			0		
5	Number of ground reference planes required for each DDR2 routing layer	1				
6	Number of layers between DDR2 routing layer and reference ground plane			0		
7	PCB Routing Feature Size		4		Mils	
8	PCB Trace Width w		4		Mils	
8	PCB BGA escape via pad size		18		Mils	
9	PCB BGA escape via hole size		8		Mils	
10	DSP Device BGA pad size					See Note (1)
11	DDR2 Device BGA pad size					See Note (2)
12	Single Ended Impedance, Zo	50		75	Ω	
13	Impedance Control	Z-5	Z	Z+5	Ω	See Note (3)

(1) Please refer to the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811) for DSP device BGA pad size.
(2) Please refer to the DDR2 device manufacturer documenation for the DDR2 device BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

1.1.4 Placement

Figure 2 shows the required placement for the C6454/5 device as well as the DDR2 devices. The dimensions for Figure 3 are defined in Table 4. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16 bit DDR memory systems, the high word DDR2 device is omitted from the placement.

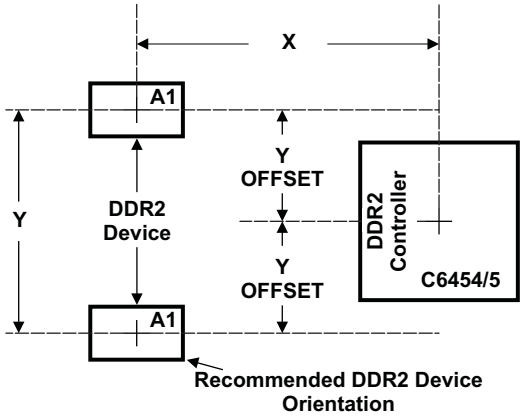


Figure 3. C6454/5 and DDR2 Device Placement

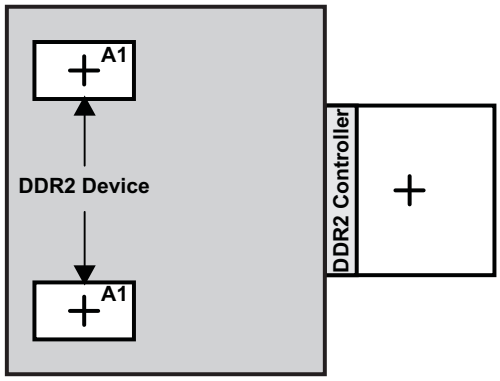
Table 4. Placement Specifications

No.	Parameter	Min	Max	Unit	Notes
1	X		1660	Mils	See Notes (1), (2)
2	Y		1280	Mils	See Notes (1), (2)
3	Y Offset		650	Mils	See Notes (1), (2), (3).
4	DDR2 Keepout Region				See Note (4)
5	Clearance from non-DDR2 signal to DDR2 Keepout Region	4		w	See Note (5)

(1) See Figure 1 for dimension defintions.
(2) Measurements from center of DSP device to center of DDR2 device.
(3) For 16 bit memory systems it is recommended that Y Offset be as small as possible.
(4) DDR2 Keepout region to encompass entire DDR2 routing area
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

1.1.5 DDR2 Keep Out Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keep out region is defined for this purpose and is shown in Figure 4. The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are shown in Table 4.



Region should encompass all DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keep out region. Non-DDR2 signals may be routed in the region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.

Figure 4. DDR2 Keepout Region

1.1.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 5 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DSP and DDR2 interfaces. Additional bulk bypass capacitance may be needed for other circuitry.

Table 5. Bulk Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	DV_{DD18} Bulk Bypass Capacitor Count	3		Devices	See Note (1)
2	DV_{DD18} Bulk Bypass Total Capacitance	30		µF	
3	DDR#1 Bulk Bypass Capacitor Count	1		Devices	See Note (1)
4	DDR#1 Bulk Bypass Total Capacitance	10		µF	
5	DDR#2 Bulk Bypass Capacitor Count	1		Devices	See Notes (1), (2)
6	DDR#2 Bulk Bypass Total Capacitance	10		µF	See Note (2)

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.
(2) Only used on 32-bit wide DDR2 memory systems

1.1.7 High-Speed Bypass Capacitors

High-Speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, DSP/DDR power, and DSP/DDR ground connections. Table 6 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

1.1.8 Net Classes

Table 7 lists the clock net classes for the DDR2 interface. Table 8 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

Table 6. High-Speed Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	HS Bypass Capacitor Package Size		0402	10 Mils	See Note (1)
2	Distance from HS bypass capacitor to device being bypassed		250	Mils	
3	Number of connection vias for each HS bypass capacitor	2		Vias	See Note (2)
4	Trace length from bypass capacitor contact to connection via	1	30	Mils	
5	Number of connection vias for each DDR2 device power or ground balls	1		Vias	
6	Trace length from DDR2 device power ball to connection via		35	Mils	
7	DV_{DD18} HS Bypass Capacitor Count	20		Devices	See Note (3)
8	DV_{DD18} HS Bypass Capacitor Total Capacitance	1.2		µF	
9	DDR#1 HS Bypass Capacitor Count	8		Devices	See Note (3)
10	DDR#1 HS Bypass Capacitor Total Capacitance	0.4		µF	
11	DDR#2 HS Bypass Capacitor Count	8		Devices	See Notes (3), (4)
12	DDR#2 HS Bypass Capacitor Total Capacitance	0.4		µF	See Note (4)

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Only used on 32-bit wide DDR2 memory systems

Table 7. Clock Net Class Definitions

Clock Net Class	DSP Pin Names
CK	DDR2CLKOUT/$\overline{\text{DDR2CLKOUT}}$
DQS0	DSDDQS0/$\overline{\text{DSDDQS0}}$
DQS1	DSDDQS1/$\overline{\text{DSDDQS1}}$
DQS2[1]	DSDDQS2/$\overline{\text{DSDDQS2}}$
DQS3[1]	DSDDQS3/$\overline{\text{DSDDQS3}}$

(1) Only used on 32-bit wide DDR2 memory systems.

Table 8. Signal Net Class Definitions

Clock Net Class	Associated Clock Net Class	DSP Pin Names
ADDR_CTRL	CK	DBA[2:0], DEA[13:0], $\overline{\text{DCE0}}$, $\overline{\text{DSDCAS}}$, $\overline{\text{DSDRAS}}$, $\overline{\text{DSDWE}}$, DSD_CKE
DQ0	DQS0	DED[7:0], DSDDQM0
DQ1	DQS1	DED[15:8], DSDDQM1
DQ2[1]	DQS2	DED[23:16], DSDDQM2
DQ3[1]	DQS3	DED[31:24], DSDDQM3
DQGATEL	CK, DQS0, DQS1	DSDDQGATE0, DSDDQGATE1
DQGATEH[1]	CK, DQS2, DQS3	DSDDQGATE2, DSDDQGATE3

(1) Only used on 32-bit wide DDR2 memory systems.

1.1.9 DDR2 Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 9 shows the specifications for the series terminators.

Table 9. DDR2 Signal Terminations

No.	Parameter	Min	Typ	Max	Unit	Notes
1	CK Net Class	0		10	Ω	See Note (1)
2	ADDR_CTRL Net Class	0	22	Zo	Ω	See Notes (1), (2), (3)
3	Data Byte Net Classes (DQS0-DQS3, DQ0-DQ3)	0	22	Zo	Ω	See Notes (1), (2), (3), (4)
4	DQGATE Net Classes (DQGATEL, DQGATEH)	0	10	Zo	Ω	See Notes (1), (2), (3)

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.
(4) When no termination is used on data lines (0 Ωs), the DDR2 devices must be programmed to operate in 60% strength mode.

1.1.10 VREF Routing

VREF is used as a reference by the input buffers of the DDR2 memories as well as the C6454/5's. VREF is intended to be 1/2 the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 1. Other methods of creating VREF are not recommended. Figure 5 shows the layout guidelines for VREF.

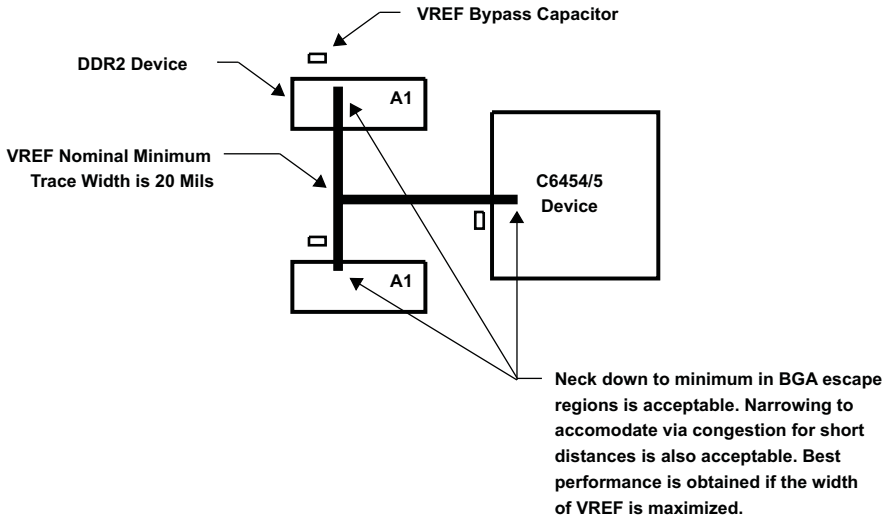


Figure 5. VREF Routing and Topology

1.1.11 DDR2 CK and ADDR_CTRL Routing

Figure 6 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

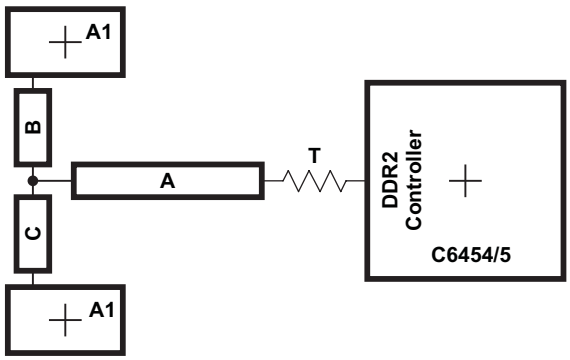


Figure 6. CK and ADDR_CTRL Routing and Topology

Table 10. CK and ADDR_CTRL Routing Specification (1)

No	Parameter	Min	Typ	Max	Unit	N otes
1	Center to center CK-$\overline{CK}$ spacing			2w		
2	CK A to B/A to C Skew Length Mismatch			25	Mils	See Note (1)
3	CK B to C Skew Length Mismatch			25	Mils	
4	Center to center CK to other DDR2 trace spacing	4w				See Note (2)
5	CK/ADDR_CTRL nominal trace length	CACLM-50	CACLM	CACLM+50	Mils	See Note (3)
6	ADDR_CTRL to CK Skew Length Mismatch			100	Mils	
7	ADDR_CTRL to ADDR_CTRL Skew Length Mismatch			100	Mils	
8	Center to center ADDR_CTRL to other DDR2 trace spacing	4w				See Note (2)
9	Center to center ADDR_CTRL to other ADDR_CTRL trace spacing	3w				See Note (2)
10	ADDR_CTRL A to B/A to C Skew Length Mismatch			100	Mils	See Note (1)
11	ADDR_CTRL B to C Skew Length Mismatch			100	Mils	

(1) Series terminator, if used, should be located closest to DSP.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 7 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

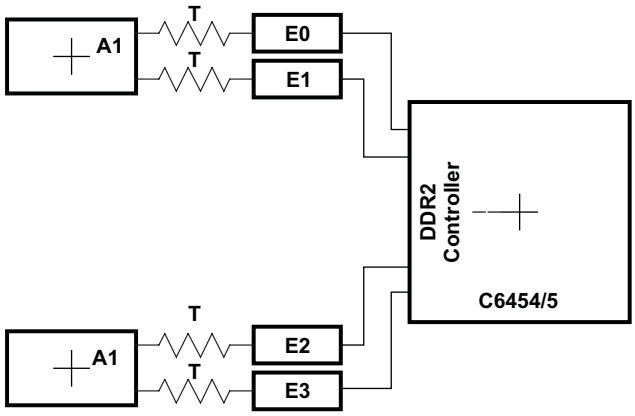


Figure 7. DQS and DQ Routing and Toplogy

Table 11. DQS and DQ Routing Specification (1)

No.	Parameter	Min	Typ	Max	Unit	Notes
1	Center to center DQS-$\overline{DQS}$ spacing			2w		
2	DQS E Skew Length Mismatch			25	Mils	
3	Center to center DQS to other DDR2 trace spacing	4w				See Note (2)
4	DQS/DQ nominal trace length	DQLM-50	DQLM	DQLM+50	Mils	See Notes (1), (3), (4), (5)
5	DQ to DQS Skew Length Mismatch			100	Mils	See Notes (3), (4), (5)
6	DQ to DQ Skew Length Mismatch			100	Mils	See Notes (3), (4), (5)
7	Center to center DQ to other DDR2 trace spacing	4w				See Notes (2), (6)
8	Center to Center DQ to other DQ trace spacing	3w				See Notes (7), (2)
9	DQ/DQS E Skew Length Mismatch			100	Mils	See Notes (3), (4), (5)

(1) Series terminator, if used, should be located closest to DDR.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) A 16 bit DDR memory system will have two sets of data net classes, one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQS's).
(4) A 32 bit DDR memory system will have four sets of data net classes, one each for data bytes 0 through 3, and each associated with a DQS (4 DQS's).
(5) There is no need and it is not recommended to skew match across data bytes, ie from DQS0 and data byte 0 to DQS1 and data byte 1.
(6) DQ's from other DQS domains are considered *other DDR2 trace*.
(7) DQLM is the longest Manhattan distance of each of the DQS and DQ net classes.

Figure 8 shows the routing for the DQGATE net classes. Table 12 contains the routing specification.

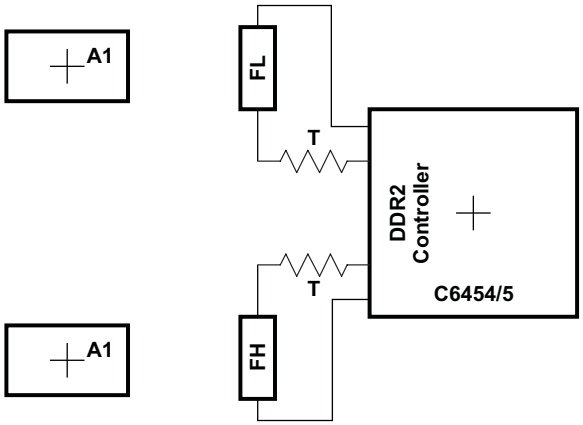


Figure 8. DQGATE Routing

Table 12. DQGATE Routing Specification

No.	Parameter	Min	Typ	Max	Unit	Notes
1	DQGATEL Length F		CKB0B1			See Note (1)
2	DQGATEH Length F		CKB2B3			See Notes (2), (3)
3	Center to center DQGATE to any other trace spacing	4w				
4	DQS/DQ nominal trace length	DQLM-50	DQLM	DQLM+50	Mils	
5	DQGATEL Skew			100	Mils	See Note (4)
6	DQGATEH Skew			100	Mils	See Notes (5), (3)

(1) CKB0B1 is the sum of the length of the CK net plus the average length of the DQS0 and DQS1 nets.
(2) CKB2B3 is the sum of the length of the CK net plus the average length of the DQS2 and DQS3 nets.
(3) Only used on 32-bit wide DDR2 memory systems.
(4) Skew from CKB0B1
(5) Skew from CKB2B3

2 References

- *TMS320C6454 Fixed-Point Digital Signal Processor Data Manual* (SPRS311)
- *TMS320C6455 Fixed-Point Digital Signal Processor Data Manual* (SPRS276)
- *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0)
- *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265