

TMS320VC5501 Hardware Designer’s Resource Guide

DSP Hardware Application Team

ABSTRACT

The DSP Hardware Designer’s Resource Guide is organized by development flow and functional areas to make your design effort as seamless as possible. Topics covered include getting started, board design, system testing, and checklists to aid in your initial design and debug efforts. Each section includes pointers to valuable information including technical documentation, models, symbols, and reference designs for use in each phase of design. Particular attention is given to peripheral interfacing and system level design concerns.

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1 Getting Started

1.1 Registering on my.TI

my.TI is a customizable area within the Texas Instruments web site. By registering on my.TI, you can receive the following benefits:

- Quick Reference to information you select as part of your profile.
- Email alerts that inform you of updates to products, technical documentation, and errata.
- The my.TI newsletter providing information on the latest innovations and product releases.

To register on my.TI for updates related to the this device:

1. Go to the device product folder.
2. Select the link called “ADD To my.TI” in the upper right hand corner, and follow the on-screen instructions.
3. Select Customize my.TI to specify what you would like to receive notification about.

Use the following link to access the product folder.

[TMS320VC5501 DSP product folder](#)

1.2 Training and Support

Texas Instruments offers a variety of training options tailored for your specific needs and requirements. Options include on-line training, webcasts, seminars, single and multi-day workshops, and conferences. For more information about training, visit Texas Instruments [Training Home](#). For assistance with technical questions regarding TI Semiconductor products and services, you can access the [Semiconductor Technical Support KnowledgeBase](#).

1.3 Technical Documentation

1.3.1 *Where to Start*

The key area for obtaining documentation for this device is the product folder. When getting started, it is of great importance to have the latest data sheet and silicon errata. Often, a “Getting Started with” or “How to Begin Development with” application report is available as well. Listed below are links to this key information:

- [TMS320VC5501 DSP product folder](#)
- [TMS320VC5501 Fixed-Point Digital Signal Processor \(SPRS206\)](#)
- [C55x CPU Programmer’s Reference Supplement \(SPRU652\)](#)
- [TMS320VC5502 and TMS320VC5501 Digital Signal Processors Silicon Errata \(SPRZ020\)](#)

1.3.2 *Using TI Literature Numbers*

All TI documentation is assigned a literature number. This number can be used to search for the document on the Web. Technical documentation revisions are indicated by the alpha character at the end of the literature number on the title page, and in the file name.

Use the literature number (without the trailing alpha character) to search the TI website for the document. For example, if a data manual has a literature number of SPRS205B, the "B" indicates the revision of the document. If the document has no trailing alpha character, it is the original version of the document. When searching for this document on the TI web site, you can simply enter "SPRS205" as the search keyword.

1.3.3 Technical Publication Descriptions

This section describes the content contained in technical publications which support this device. All of the technical publications described below can be found in the device product folder. Check your device product folder frequently for the most recent technical documentation.

Data Sheets and Data Manuals

The Data Sheet or Data Manual is the functional specification for the device. Topics covered in this document include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Silicon Errata

The Silicon Errata documents exceptions to the functional specification as defined in the Data Sheet or Data Manual.

Reference Guides

Reference Guides provide additional information describing the architecture and operation of hardware components of the DSP platform, generation, or device, beyond the scope of the Data Sheet or Data Manual.

Application Reports

Application Reports are written to describe implementation details specific to a device, peripheral, use of technology, or explanation of usage.

1.3.4 Peripheral Reference Guides

Each peripheral has a reference guide that provides beneficial information for completing a design. Each peripheral and its respective reference guide is listed here. There are two categories. The first category contains peripherals which connect directly to external devices. The second category lists the internal peripherals.

Peripherals that connect directly to external devices:

- [TMS320VC5501/5502/5503/5507/5509/5510 DSP \(McBSP\) Reference Guide \(SPRU592\)](#)
- [TMS320VC5501/5502 DSP Universal Asynchronous Receiver/Transmitter \(UART\) Reference Guide \(SPRU597\)](#)
- [TMS320VC5501/5502/5503/5507/5509 DSP Inter-Integrated Circuit \(I2C\) Module Reference Guide \(SPRU146\)](#)
- [TMS320VC5501/5502 DSP External Memory Interface \(EMIF\) Reference Guide \(SPRU621\)](#)
- [TMS320VC5501/5502 DSP Host Port Interface \(HPI\) Reference Guide \(SPRU620\)](#)
- [TMS320VC5501/5502 DSP Timers Reference Guide \(SPRU618\)](#)

Internal peripherals:

- [TMS320C55x DSP Peripherals Overview Reference Guide \(SPRU317\)](#)
- [TMS320VC5501/5502 DSP Instruction Cache Reference Guide \(SPRU630\)](#)
- [TMS320VC5501/5502 DSP Direct Memory Access \(DMA\) Controller Reference Guide \(SPRU613\)](#)

1.3.5 **Application Reports**

Organized by category and listed below are application reports that provide useful information for designing on this device.

Instruction Cache:

- [Achieving Efficient Memory System Performance w/ I-Cache on the TMS320VC5501/02 \(SPRA924\)](#)

2 **Board Design and Layout**

2.1 **Reference Design**

A reference design is not currently available for this device.

2.2 **Schematics**

TI provides CAD symbols in a variety of formats to assist in schematic generation. The symbols are located in the DSP product folder or directly accessible through the link below.

<http://focus.ti.com/docs/prod/folders/print/tms320vc5501.html#symbols>

2.3 Signal Integrity and Timing Considerations

High-speed interfaces require strict timings and accurate system design. To achieve the necessary timings for a given system, input/output buffer information specification (IBIS) models must be used. These models accurately represent the device drivers under various process conditions. Board characteristics, such as impedance, loading, length, number of nodes, etc., affect signal performance. The following IBIS models are available for this device:

- [C5501 PGF IBIS Model \(SPRM160\)](#)
- [C5501 GZZ IBIS Model \(SPRM161\)](#)

The following application report discusses how to use IBIS models for timing analysis:

[Using IBIS Models for Timing Analysis \(SPRA839\)](#)

2.4 Board Layout

The significance of electromagnetic compatibility (EMC) of electronic circuits and systems has recently been increasing. This increase has led to more stringent requirements for the electromagnetic properties of equipment. Two property aspects are of interest: the ability of a circuit to generate the lowest (or zero) interference, and the immunity of a circuit to the effects of the electromagnetic energy it is subjected to. The effects on electronic circuits and systems is well documented, but little attention has been paid to circuit behavior and the interference it generates. The following link discusses the important criteria that determine the EMC of a circuit.

[Printed-Circuit Board Layout for Improved Electromagnetic Compatibility \(SDYA011\)](#).

2.5 Power Supply and Sequencing Considerations

Texas Instruments offers several [Power Management Products](#) for this device. For a complete list of product offerings, visit the power.ti.com website.

2.6 Power/Thermal Management Considerations

Circuit designers must always consider the effects of heat transfer from a device die to the surrounding package. The flow of heat from the device to ambient must be sufficient to maintain the device temperature as specified in the device data manual. The thermal resistance characteristics for this device are documented in the data manual. Available application reports relating to thermal analysis, heat sink selection, and power consumption are listed below:

[TMS320VC5501/02 Power Consumption Summary \(SPRA993\)](#)

2.7 Boot Mode Configurations

The TMS320VC5501 provides an on-chip bootloader and supports the following boot modes:

- HPI boot
- EMIF boot (from 16-bit asynchronous memory)
- Direct execution from external 16-bit or 32-bit asynchronous memory
- Standard serial port boot from McBSP0 (with 16-bit word size)
- Serial SPI EEPROM boot from McBSP0
- I2C boot
- UART boot

The desired boot mode is selected by the state of the BOOTM pins at reset. These pins have a shared function with GPIO pins. For information on all of the boot modes, see the document:

[Using the TMS320VC5501/5502 Bootloader \(SPRA911\)](#)

2.8 Joint Test Action Group (JTAG) Emulation Interface

DSP devices have a JTAG interface that allows for emulation hardware and software to communicate with the DSP. The JTAG port also supports boundary scan testability. For information about emulation capabilities, emulation technical documentation and products, see the emulation tools product folders below:

If you are using the TI XDS510 emulator, go to:

[XDS510 product folder](#)

If you are using the TI XDS560 emulator, go to:

[XDS560 product folder](#)

If you are using a third-party emulator, contact the emulator manufacturer.

2.9 Board Manufacturing

When designing with a high-density BGA package, it is important to be aware of different techniques that aid in the quality of manufacturing. The following documentation discusses board manufacturing considerations:

- [High-Density Design With MicroStar™ BGAs \(SPRA471\)](#)
- [Electrostatic Discharge \(SSYA008\)](#)

3 System Test

3.1 Boundary Scan Description Language (BSDL) Model(s)

BSDL models can be used to perform board interconnect tests as well as other board level diagnostics and functions. Boundary scan tests require that each scan device on the board be described in the Boundary Scan Description Language (BSDL) model. Depending on the available silicon, more than one BSDL model may be available. The following BSDL models are available for this device:

- [C5501 PGF BSDL Model \(SPRM158\)](#)
- [C5501 GZZ BSDL Model \(SPRM159\)](#)

4 Checklists

4.1 Design Checklist

The Design Checklist was put together by Texas Instruments application and field support staff as a guide to considerations made during the design phase of development. Use this check list to keep track of considerations you make during the design phase of development.

	Issue	Description
<input type="checkbox"/>	Clean power supplies	Noisy power supplies can create several problems in your system. Power supplies should conform to the specification in the DSP data manual and voltage ripple and switching noise should be minimized. Voltage ripple of less than 20 mV is recommended.
<input type="checkbox"/>	Decoupling capacitors	Decoupling capacitors provide power stability during current load transients and also help shunt system switching noise to ground instead of entering the logic inside the DSP. Decoupling capacitors should be placed as near the DSP package as possible.
<input type="checkbox"/>	RESET	It is important to be able to reset the DSP if it gets into an unstable state. It may be useful to provide a reset switch on the board to facilitate this during debug. Power supervisors also can trigger a reset if the system power supplies fall below a predefined level. For more information on power supervisors, see power.ti.com . Note that while RESET is low, the emulator will not initialize.
<input type="checkbox"/>	Bootmode Selection Pins (BOOTM)	Check to make sure the BOOTM pins are configured correctly for the desired boot mode. For debug purposes, it may be useful to provide the ability to change the BOOTM pins, such as using jumpers instead of hardwired connections.
<input type="checkbox"/>	IO4 Visibility	IO4 is used by the bootloader for different purposes depending on the boot mode chosen. It is very useful during bootloader debug to have the ability to monitor IO4. Consider bringing IO4 to a via or test point where it can be observed using an oscilloscope or logic analyzer.
<input type="checkbox"/>	EMU0 and EMU1 pins high when unused	EMU0 and EMU1 are pins used by the emulator to communicate with the DSP. After debug, when the emulator is no longer in use and disconnected, it is essential that these pins are driven high. On the TMS320VC5502, internal pull-ups are provided on these two pins and can be enabled/disabled through software. See TMS320VC5501 Fixed-Point Digital Signal Processor (SPRS206) for more information. You should ensure that nothing else in your design pulls down these pins when the emulator is not connected.
<input type="checkbox"/>	Do not pull-up TRST	TRST is the reset signal for the JTAG Test Access Port internal logic. This pin has an internal pull-down circuit inside the DSP. TRST should not be pulled up externally since the opposing circuits will pull the pin to an intermediate voltage and cause unpredictable behavior of the device.
<input type="checkbox"/>	CLKOUT	Even if CLKOUT is not being used in the design, it may be useful to bring CLKOUT to a test point for debug purposes. It is useful to verify PLL settings and behavior.

<input type="checkbox"/>	Unused EMIF ARDY signal should remain high	If the ARDY pin is not controlled by an external device, the board should be designed such that the ARDY pin is always driven high. If ARDY is uncontrolled, this can cause unpredictable behavior of the EMIF or cause the emulator to fail to initialize.
<input type="checkbox"/>	Unused EMIF $\overline{\text{HOLD}}$ signal should remain high	If the $\overline{\text{HOLD}}$ pin is not controlled by an external device, the board should be designed such that the $\overline{\text{HOLD}}$ pin is always driven high. If $\overline{\text{HOLD}}$ is uncontrolled, this can cause unpredictable behavior of the EMIF or cause the emulator to fail to initialize.
<input type="checkbox"/>	HPI timings	Verify that all HPI timings are met as specified in the data manual. Incorrect timings can cause data errors and unpredictable operation of the HPI.
<input type="checkbox"/>	Route peripheral signals to test points / vias	It may be useful to route the signals for the peripherals used to test points or vias on the board so they can be observed during debug. This assists in comparing the signals entering/leaving the peripheral with the desired send/receive data.
<input type="checkbox"/>	General Signal Visibility	If space allows, the more signals that are accessible, the easier the system will be to debug. At a minimum, signals can be routed to vias that are accessible from the top or bottom of the board. For other parallel and serial interfaces, it can be useful to have the buses routed to connectors that can be used with a logic analyzer. Once the design debug is completed, the connectors can be omitted from the final build of the board.
<input type="checkbox"/>	GPIO availability	<p>General-purpose I/O pins are very useful during debug. They can be used as indicators within the code to verify the progression of the algorithm. Even if some GPIO pins are not being used in the final design, consider bringing some of them out to vias or connectors on the board for debug purposes. GPIOs connected to LEDs provide very convenient observation tools during debug.</p> <p>XF is a dedicated general-purpose output controlled by the CPU. The other GPIOs are controlled as peripherals and have longer latency. XF responds within approximately one cycle of the execution of the instruction that modified it.</p> <p>GPIOs respond within approximately six cycles of the execution of the instruction that modified them.</p>
<input type="checkbox"/>	Controlling unused interrupts	Unused interrupt pins should be driven high. If left floating, noise coupled onto these pins can cause spurious interrupts to occur. Although most interrupts are maskable so these false interrupts could be masked in software, NMI is not maskable and cannot be prevented. It is good design practice to pull up any unused interrupt pin.
<input type="checkbox"/>	General-purpose I/O pins after boot	Some GPIO pins may remain configured as outputs after the bootloader process. Be aware of which pins are affected and their affect on your design after the application begins running. For more information on the affected pins, see Using the TMS320VC5501/5502 Bootloader (SPRA911) .

4.2 Debug Checklist

4.2.1 Peripherals Debug Tips

Table 1. Power

	Issue	Description
<input type="checkbox"/>	Higher than expected idle power	The connection of the emulator to the JTAG header can increase a device power measurement. This can be due to current flow through the PD pin and due to the current generated on the DSP by the presence of TCK running. Power measurements on a final application should be made with the emulation cable disconnected.
<input type="checkbox"/>	Higher than expected idle power	If the McBSP remains enabled and operating, it can prevent the CLKGEN domain from idling because it still requires a clock. For minimum idle power, the McBSP should be placed in reset.
<input type="checkbox"/>	Unexpected wake-up from IDLE mode	There are several events that can wake the DSP from IDLE mode. Make sure that the events that are not used are prevented from occurring. See the data manual for a list of the events capable of waking the DSP from IDLE mode.

Table 2. Crystal Oscillator

	Issue	Description
<input type="checkbox"/>	Crystal startup problems	<p>Startup problems can occur if the crystal is physically placed far away from the DSP on the board (due to additional resistance and parasitic effects). Place the crystal as close as possible to the DSP in the design layout.</p> <p>Use the recommended values for the load capacitors on the crystal. Changing load capacitors can alter the loop gain of the oscillator and cause slow or failed startup.</p>

Table 3. Phase Loop Lock (PLL) and Clock Generation

Issue		Description
<input type="checkbox"/>	CPU crashes after enabling the PLL	Make sure that the configuration for the PLL, in combination with the input clock to the DSP, does not produce an operating clock frequency higher than the clock specification in the datasheet. Although the PLL may be able to produce a clock speed higher than the rated value, proper operation of the device is only ensured at speeds within the data manual specification.
<input type="checkbox"/>	Incorrect clock group frequency relationships	On the DSP, there are required frequency relationships between the CPU clock, SYSCLK1, SYSCLK2, and SYSCLK3. Violating the required frequency relationships between these clock groups can cause unpredictable behavior. The DSP provides a set of dividers for configuring the frequency of each clock group. Use care when configuring the clock dividers to ensure that required frequency relationships for each clock group are maintained. See the Clock Groups section of TMS320VC5501 Fixed-Point Digital Signal Processor (SPRS206) for more information.

Table 4. Multi-channel Buffer Serial Port (McBSP)

Issue		Description
<input type="checkbox"/>	Higher than expected idle power	If the McBSP remains enabled and operating, it can prevent the CLKGEN domain from idling because it still requires a clock. For minimum idle power, the McBSP should be placed in reset.

Table 5. External Memory Interface (EMIF)

Issue		Description
<input type="checkbox"/>	Random SDRAM Issues	SDRAM is a synchronous memory type and relies on timing relative to a memory clock. Various problems can occur if the signal integrity of the interface is poor. Some issues that can contribute to SDRAM signal problems are: <ul style="list-style-type: none"> • SDRAMs are too far from the DSP on the board layout. • Interface is overloaded causing poor signal edge transitions. In this case, buffers should be used on the interface. • Interface signals are suffering reflections due to poor impedance matching. In this case, termination should be used.
<input type="checkbox"/>	Asynchronous memory interface hangs or behaves unpredictably	Make sure ARDY is controlled high if it is not used. If left floating, it can pick up environmental electrical noise and cause unpredictable behavior of the EMIF.
<input type="checkbox"/>	Asynchronous memory interface hangs or behaves unpredictably	Make sure $\overline{\text{HOLD}}$ is controlled high if it is not used. If left floating, it can pick up environmental electrical noise and cause unpredictable behavior of the EMIF.

<input type="checkbox"/>	Unexpected timing between the CPU and the EMIF	When the CPU writes data to the EMIF, the EMIF latches the data and prepares to initiate the external write to the memory. When the data is latched, the EMIF acknowledges the receipt of the data to the CPU, so the CPU gets acknowledgement of the write before the write is actually completed externally.
<input type="checkbox"/>	Unexpected read / write order on the EMIF	The CPU pipeline schedules memory accesses in the most efficient way possible, which may not correspond to the order they occurred in the code. The pipeline will ensure that reads and writes to the same address occur in code order, but accesses to different addresses will be scheduled as efficiently as possible. For more information, see TMS320VC5501/5502 DSP External Memory Interface (EMIF) Reference Guide (SPRU621) .
<input type="checkbox"/>	EMIF timings	If EMIF problems occur, be sure to verify that the EMIF timings are consistent with the timing requirements of the external memory being used. Both the fixed timings in the data manual and the configurable timings affect the overall timing of the interface.

Table 6. Host Port Interface (HPI)

Issue		Description
<input type="checkbox"/>	HPI errors	The minimum low pulse width and high pulse width for the data strobe ($\overline{HDS1}$ and/or $\overline{HDS2}$) is not being met. Refer to the data manual for timing requirements for the HPI.
<input type="checkbox"/>	Apparent incorrect operation of the HPI data bus	The HPI data is routed to pins according to the HPI mode selected. If the HPI is configured in non-multiplexed mode (GPIO6 is low during reset), the EMIF is disabled and pins D[15:0] are configured as HPI.HD[15:0]. If GPIO6 is high at reset, the EMIF is enabled and uses D[15:0] for EMIF functions and the HPI is configured in multiplexed mode and uses separate pins HD[7:0] for HPI functions. Also, A[15:0] are configured as HPI.A[15:0]. When debugging, make sure the appropriate pins are monitored according to the chosen mode. See the TMS320VC5501 Fixed-Point Digital Signal Processor (SPRS206) for more information.

Table 7. Direct Memory Access (DMA)

Issue		Description
<input type="checkbox"/>	Delay after enabling DMA channel	After a DMA channel is enabled, the DMA controller copies the channel context registers over to the working set. The working set of registers is used during the actual data movement on the DMA channel. This action causes some latency between the time the DMA channel is enabled and when the first transfer occurs.
<input type="checkbox"/>	DMA channel source and destination appear to be out of sync	The DMA channel FIFO can pre-fetch data from the source to be delivered later when the destination is ready. This can cause the source and destination address counters to appear to be out of sync.

<input type="checkbox"/>	Unexpected bus error flags	The DMA channel controller will issue a bus error flag/interrupt if the value written to the element or frame index registers is not valid for the DMA configuration even if indexed addressing is not being used. Always write a valid value to the element and frame index registers even if indexed addressing is not being used.
<input type="checkbox"/>	DMA system hangs or suffers long delays	Be careful to ensure that the addresses generated by the DMA controller produce actual addresses where something is mapped. For instance, if an invalid address is generated to the DMA DARAM port (meaning there is no actual physical memory at that location), the DMA system may hang waiting for the non-existent memory to respond. You can utilize the timeout features of the DMA to prevent the system from hanging, but generation of invalid addresses should be avoided anyway to prevent delays.
<input type="checkbox"/>	DMA data appears to be missing or placed at the wrong location	The DMA controller considers all addresses as byte addresses not word addresses. Make sure that the source and destination addresses during the DMA configuration are byte-addresses.
<input type="checkbox"/>	DMA reads data from external memory before sync events is received	The DMA will pre-fetch data into its FIFO when the source is external memory or internal memory. It will write the data to the destination when the sync events is received. For more information on the pre-fetch behavior of the DMA, see TMS320VC5501/5502 DSP Direct Memory Access (DMA) Controller Reference Guide (SPRU613) .

5 Summary

Using the information provided in this document, along with documentation that is pointed out for each step of the design process, a DSP designer will be able to make more knowledgeable decisions concerning their design.

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