Application Report
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TMS320VC5510/5510A Hardware Designer's Resource Guide

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ABSTRACT

The DSP Hardware Designer's Resource Guide is organized by development flow and functional areas to make your design effort as seamless as possible. Topics covered include getting started, board design, system testing, and checklists to aid in your initial design and debug efforts. Each section includes pointers to valuable information including technical documentation, models, symbols, and reference designs for use in each phase of design. Particular attention is given to peripheral interfacing and system level design concerns.

All of the resources listed in this document apply to both the TMS320VC5510 and the TMS320VC5510A unless specifically stated otherwise.

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1 Getting Started

All of the resources listed in this document apply to both the TMS320VC5510 and the TMS320VC5510A unless specifically stated otherwise.

1.1 Registering on my.TI

my.TI is a customizable area within the Texas Instruments web site. By registering on my.TI, you can receive the following benefits:

- Quick Reference to information you select as part of your profile.
- Email alerts that inform you of updates to products, technical documentation, and errata.
- The my.TI newsletter providing information on the latest innovations and product releases.

To register on my.TI for updates related to the this device:

1. Go to the device product folder.
2. Select the link called "ADD To my.TI" in the upper right hand corner, and follow the on-screen instructions.
3. Select Customize my.TI to specify what you would like to receive notification about.

Use the following link to access the product folder.

TMS320VC5510/5510A DSP product folder

1.2 Training and Support

Texas Instruments offers a variety of training options tailored for your specific needs and requirements. Options include on-line training, webcasts, seminars, single and multi-day workshops, and conferences. For more information about training, visit Texas Instruments Training Home. For assistance with technical questions regarding TI Semiconductor products and services, you can access the Semiconductor Technical Support KnowledgeBase .

1.3 Technical Documentation

1.3.1 Where to Start

The key area for obtaining documentation for this device is the product folder. When getting started, it is of great importance to have the latest data sheet and silicon errata. Often, a "Getting Started with" or "How to Begin Development with" application report is available as well. Listed below are links to this key information:

- TMS320VC5510/5510A DSP product folder
- TMS320VC5510/5510A Fixed-Point Digital Signal Processor (SPRS076)
- C55x CPU Programmer's Reference Supplement (SPRU652)
- TMS320VC5510/5510A Digital Signal Processor Silicon Errata (SPRZ008)

1.3.2 Using TI Literature Numbers

All TI documentation is assigned a literature number. This number can be used to search for the document on the Web. Technical documentation revisions are indicated by the alpha character at the end of the literature number on the title page, and in the file name.

Use the literature number (without the trailing alpha character) to search the TI website for the document. For example, if a data manual has a literature number of SPRS205B, the "B" indicates the revision of the document. If the document has no trailing alpha character, it is the original version of the document. When searching for this document on the TI web site, you can simply enter "SPRS205" as the search keyword.

1.3.3 Technical Publication Descriptions

This section describes the content contained in technical publications which support this device. All of the technical publications described below can be found in the device product folder. Check your device product folder frequently for the most recent technical documentation.

Data Sheets and Data Manuals

The Data Sheet or Data Manual is the functional specification for the device. Topics covered in this document include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Silicon Errata

The Silicon Errata documents exceptions to the functional specification as defined in the Data Sheet or Data Manual.

Reference Guides

Reference Guides provide additional information describing the architecture and operation of hardware components of the DSP platform, generation, or device, beyond the scope of the Data Sheet or Data Manual.

Application Reports

Application Reports are written to describe implementation details specific to a device, peripheral, use of technology, or explanation of usage.

1.3.4 Peripheral Reference Guides

Each peripheral has a reference guide that provides beneficial information for completing a design. Each peripheral and its respective reference guide is listed here. There are two categories. The first category contains peripherals which connect directly to external devices. The second category lists the internal peripherals.

Peripherals that connect directly to external devices:

- TMS320VC5501/5502/5503/5507/5509/5510 DSP (McBSP) Reference Guide (SPRU592)
- TMS320VC5510 DSP External Memory Interface (EMIF) Reference Guide (SPRU590)
- TMS320VC5510 DSP Host Port Interface (HPI) Reference Guide (SPRU588)
- TMS320VC5503/5507/5509/5510 DSP Timers Reference Guide (SPRU595)

Internal peripherals:

- TMS320C55x DSP Peripherals Overview Reference Guide (SPRU317)
- TMS320VC5510 DSP Instruction Cache Reference Guide (SPRU576)
- TMS320VC5503/5507/5509/5510 Direct Memory Access(DMA) Controller Reference Guide (SPRU587)

1.3.5 Application Reports

Organized by category and listed below are application reports that provide useful information for designing on this device.

Host Port Interface (HPI):

- TMS320VC5510 HPI Throughput and Optimization (SPRAA24)

External Memory Interface (EMIF):

- Interfacing TMS320VC5510 to SBSRAM (SPRA722)

Other:

- Migrating from TMS320VC5510 to TMS320VC5502 (SPRA898)

2 Board Design and Layout

2.1 Reference Design

A reference design is not currently available for this device.

2.2 Schematics

Schematic symbols for this DSP are available in a variety of common formats. The schematic symbols are available for download in the "Pricing/Packaging" section of the product folder.

Some pins on the DSP may multiplex several internal functions. When pins are shared, one function will be enabled while another function is disabled. Please refer to the data manual for more information concerning multiplexed pins.

2.3 Signal Integrity and Timing Considerations

High-speed interfaces require strict timings and accurate system design. To achieve the necessary timings for a given system, input/output buffer information specification (IBIS) models must be used. These models accurately represent the device drivers under various process conditions. Board characteristics, such as impedance, loading, length, number of nodes, etc., affect signal performance.

The following IBIS model is available for this device:

- TMS320VC5510/5510A GGW IBIS Model (SPRM165)

The following application report discusses how to use IBIS models for timing analysis:

Using IBIS Models for Timing Analysis (SPRA839)

2.4 Board Layout

The significance of electromagnetic compatibility (EMC) of electronic circuits and systems has recently been increasing. This increase has led to more stringent requirements for the electromagnetic properties of equipment. Two property aspects are of interest: the ability of a circuit to generate the lowest (or zero) interference, and the immunity of a circuit to the effects of the electromagnetic energy it is subjected to. The effects on electronic circuits and systems is well documented, but little attention has been paid to circuit behavior and the interference it generates. The following link discusses the important criteria that determine the EMC of a circuit.

Printed-Circuit Board Layout for Improved Electromagnetic Compatibility (SDYA011)

2.5 Power Supply and Sequencing Considerations

Texas Instruments offers several Power Management Products for this device. For a complete list of product offerings, visit the power.ti.com website.

2.6 Power/Thermal Management Considerations

Circuit designers must always consider the effects of heat transfer from a device die to the surrounding package. The flow of heat from the device to ambient must be sufficient to maintain the device temperature as specified in the device data manual. The thermal resistance characteristics for this device are documented in the data manual. Available application reports relating to thermal analysis, heat sink selection, and power consumption are listed below:

TMS320VC5510 Power Consumption Summary (SPRA972)

2.7 Boot Mode Configurations

TMS320VC5510/5510A provide an on-chip bootloader and supports the following boot modes:

- EHPI boot (in multiplexed or non-multiplexed mode)
- EMIF boot (from 8-bit or 16-bit asynchronous memory)
- Standard serial port boot from McBSP0 (with 8-bit or 16-bit word size)
- Serial SPI EEPROM boot from McBSP0 (with 16-bit or 24-bit addresses)

The desired boot mode is selected by the state of the BOOTM pins at reset. These pins have a shared function with GPIO pins. For information on all of the boot modes, see the document:

Using the TMS320VC5510 Bootloader (SPRA763)

2.8 Joint Test Action Group (JTAG) Emulation Interface

DSP devices have a JTAG interface that allows for emulation hardware and software to communicate with the DSP. The JTAG port also supports boundary scan testability. Listed below are links to this key information.

- Emulation Fundamentals for TI DSP Solutions (SPRA439)
- 60-pin Emulation Header Technical Reference (SPRU655)

Although the TMS320VC5510 does not require the 60-pin emulation header, the link above has been included in the event that the board design involves other DSPs that do.

2.9 Board Manufacturing

When designing with a high-density BGA package, it is important to be aware of different techniques that aid in the quality of manufacturing. The following documentation discusses board manufacturing considerations:

- High-Density Design With MicroStart BGAs (SPRA471)
- Electrostatic Discharge (SSYA008)

3 System Test

3.1 Boundary Scan Description Language (BSDL) Model(s)

BSDL models can be used to perform board interconnect tests as well as other board level diagnostics and functions. Boundary scan tests require that each scan device on the board be described in the Boundary Scan Description Language (BSDL) model. Depending on the available silicon, more than one BSDL model may be available. The following BSDL model is available for this device:

- VC5510 GGW BSDL Model (SPRM085)

4 Checklists

4.1 Design Checklist

The Design Checklist was put together by Texas Instruments application and field support staff as a guide to considerations made during the design phase of development. Use this check list to keep track of considerations you make during the design phase of development.

	Issue	Description
☐	Clean power supplies	Noisy power supplies can create several problems in your system. Power supplies should conform to the specification in the DSP data manual and voltage ripple and switching noise should be minimized. Voltage ripple of less than 20 mV is recommended.
☐	Decoupling capacitors	Decoupling capacitors provide power stability during current load transients and also help shunt system switching noise to ground instead of entering the logic inside the DSP. Decoupling capacitors should be placed as near the DSP package as possible.
☐	RESET	It is important to be able to reset the DSP if it gets into an unstable state. It may be useful to provide a reset switch on the board to facilitate this during debug. Power supervisors also can trigger a reset if the system power supplies fall below a predefined level. For more information on power supervisors, see power.ti.com. Note that while RESET is low, the emulator will not initialize.
☐	Bootmode Selection Pins (BOOTM)	Check to make sure the BOOTM pins are configured correctly for the desired boot mode. For debug purposes, it may be useful to provide the ability to change the BOOTM pins, such as using jumpers instead of hardwired connections.
☐	IO4 Visibility	IO4 is used by the bootloader for different purposes depending on the boot mode chosen. It is very useful during bootloader debug to have the ability to monitor IO4. Consider bringing IO4 to a via or test point where it can be observed using an oscilloscope or logic analyzer.

☐	EMU0 and EMU1 pins high when unused	EMU0 and EMU1 are pins used by the emulator to communicate with the DSP. After debug, when the emulator is no longer in use and disconnected, it is essential that these pins are driven high. On the DSP, internal pull-ups are provided on these two pins. You should ensure that nothing else in your design pulls down these pins when the emulator is not connected.
☐	Do not pull-up TRST	TRST is the reset signal for the JTAG Test Access Port internal logic. This pin has an internal pull-down circuit inside the DSP. TRST should not be pulled up externally since the opposing circuits will pull the pin to an intermediate voltage and cause unpredictable behavior of the device.
☐	CLKOUT	Even if CLKOUT is not being used in the design, it may be useful to bring CLKOUT to a test point for debug purposes. It is useful to verify PLL settings and behavior.
☐	Unused EMIF ARDY signal should remain high	If the ARDY pin is not controlled by an external device, the board should be designed such that the ARDY is always driven high. If ARDY is uncontrolled, this can cause unpredictable behavior of the EMIF or cause the emulator to fail to initialize.
☐	Unused EMIF $\overline{\text{HOLD}}$ signal should remain high	If the $\overline{\text{HOLD}}$ pin is not controlled by an external device, the board should be designed such that the $\overline{\text{HOLD}}$ is always driven high. If $\overline{\text{HOLD}}$ is uncontrolled, this can cause unpredictable behavior of the EMIF or cause the emulator to fail to initialize.
☐	EMIF CE space(s) configuration	The external memory space is divided into 4 spaces, each selected by a DSP signal CE0 -CE3. Each space is configured for a particular memory type in software. Some memory types also have timing controls that are configurable through software. Verify that the software configuration for each space is correct.Use of some SDRAM configurations requires that multiple CE spaces be used. The following CE spaces may be linked together in SDRAM mode depending on the configuration: CE0 and CE1, or CE2 and CE3, or CE0, CE1, CE2 and CE3 If these configurations are used, all of the associated CE spaces must be configured as SDRAM. For more information, see the TMS320VC5510 DSP External Memory Interface (EMIF) Reference Guide (SPRU590).
☐	EHPI timings	Verify that all EHPI timings are met as specified in the data manual. Incorrect timings can cause data errors and unpredictable operation of the EHPI.
☐	Route peripheral signals to test points / vias	It may be useful to route the signals for the peripherals used to test points or vias on the board so they can be observed during debug. This assists in comparing the signals entering/leaving the peripheral with the desired send/receive data.
☐	General Signal Visibility	If space allows, the more signals that are accessible, the easier the system will be to debug. At a minimum, signals can be routed to vias that are accessible from the top or bottom of the board. For other parallel and serial interfaces, it can be useful to have the buses routed to connectors that can be used with a logic analyzer. Once the design debug is completed, the connectors can be omitted from the final build of the board.
☐	GPIO availability	General-purpose I/O pins are very useful during debug. They can be used as indicators within the code to verify the progression of the algorithm. Even if some GPIO pins are not being used in the final design, consider bringing some of them out to vias or connectors on the board for debug purposes. GPIOs connected to LEDs provide very convenient observation tools during debug. XF is a dedicated general-purpose output controlled by the CPU. The other GPIOs are controlled as peripherals and have longer latency. XF responds within approximately one cycle of the execution of the instruction that modified it. GPIOs respond within approximately six cycles of the execution of the instruction that modified them.
☐	Controlling unused interrupts	Unused interrupt pins should be driven high. If left floating, noise coupled onto these pins can cause spurious interrupts to occur. Although most interrupts are maskable so these false interrupts could be masked in software, NMI is not maskable and cannot be prevented. It is good design practice to pull up any unused interrupt pin.

4.2 Debug Checklist

4.2.1 Peripherals Debug Tips

Table 1. Power

	Issue	Description
☐	Higher than expected idle power	The connection of the emulator to the JTAG header can increase a device power measurement. This can be due to current flow through the PD pin and due to the current generated on the DSP by the presence of TCK running. Power measurements on a final application should be made with the emulation cable disconnected.
☐	Higher than expected idle power	If the McBSP remains enabled and operating, it can prevent the CLKGEN domain from idling because it still requires a clock. For minimum idle power, the McBSP should be placed in reset.
☐	Higher than expected idle power	Since an external oscillator is used as a clock source to the DSP, the input clock will not stop when all of the DSP domains are idled (standby). The clock input buffer on the DSP continues to toggle and consume some power even though the clocks to the rest of the DSP are disabled.
☐	Idle mode changes	After the Idle Configuration Register (ICR) is modified (written), approximately six CPU clock cycles are required for the internal write to be completed. So an Idle instruction intended to use the new configuration should follow the ICR write by no less than six cycles. The instructions in between can be NOPs or other useful instructions that do not modify ICR.

Table 2. Phase Loop Lock (PLL)

	Issue	Description
☐	Excessive Jitter on the DPLL	The digital PLL (DPLL) used to provide clock to the DSP is sensitive to the quality of the power supply. Excessive power supply ripple can contribute to excessive clock edge jitter on the DPLL. CVdd power supply ripple of less than 20 mV is recommended for optimal DPLL jitter performance.
☐	DPLL lock bit is active before the updated clock is passed to the rest of the DSP.	The LOCK bit in the DPLL indicates that the PLL has locked on the desired frequency. After this occurs, the clock logic on the DSP allows the new clock speed to propagate to the rest of the DSP. Because of this, the LOCK bit becomes active before the DSP is running at the new clock speed. The delay between the LOCK bit status and DSP operating at the new clock speed may be as long as 500 us.

Table 3. Multi-channel Buffer Serial Port (McBSP)

	Issue	Description
☐	Higher than expected idle power	If the McBSP remains enabled and operating, it can prevent the CLKGEN domain from idling because it still requires a clock. For minimum idle power, the McBSP should be placed in reset.

Table 4. External Memory Interface (EMIF)

	Issue	Description
☐	Random SDRAM Issues	SDRAM is a synchronous memory type and relies on timing relative to a memory clock. Various problems can occur if the signal integrity of the interface is poor. Some issues that can contribute to SDRAM signal problems are: • SDRAMs are too far from the DSP on the board layout. • Interface is overloaded causing poor signal edge transitions. In this case, buffers should be used on the interface. • Interface signals are suffering reflections due to poor impedance matching. In this case, termination should be used
☐	Asynchronous memory interface hangs or behaves unpredictably	Make sure ARDY is controlled high if it is not used. If left floating, it can pick up environmental electrical noise and cause unpredictable behavior of the EMIF.
☐	Unused EMIF $\overline{\text{HOLD}}$ signal should remain high	If the $\overline{\text{HOLD}}$ pin is not controlled by an external device, the board should be designed such that the $\overline{\text{HOLD}}$ is always driven high. If $\overline{\text{HOLD}}$ is uncontrolled, this can cause unpredictable behavior of the EMIF or cause the emulator to fail to initialize.
☐	Unexpected timing between the CPU and the EMIF	When the CPU writes data to the EMIF, the EMIF latches the data and prepares to initiate the external write to the memory. When the data is latched, the EMIF acknowledges the receipt of the data to the CPU, so the CPU gets acknowledgement of the write before the write is actually completed externally.
☐	Unexpected read / write order on the EMIF	The CPU pipeline schedules memory accesses in the most efficient way possible, which may not correspond to the order they occurred in the code. The pipeline will ensure that reads and writes to the same address occur in code order, but accesses to different addresses will be scheduled as efficiently as possible. For more information, see TMS320VC5510 DSP External Memory Interface (EMIF) Reference Guide (SPRU590).
☐	EMIF timings	If EMIF problems occur, be sure to verify that the EMIF timings are consistent with the timing requirements of the external memory being used. Both the fixed timings in the data manual and the configurable timings affect the overall timing of the interface.
☐	EMIF CE spaces(s) configuration	The external memory space is divided into four spaces, each selected by a DSP signal CE0 -CE3. Each space is configured for a particular memory type in software. Some memory types also have timing controls that are configurable through software. Verify that the software configuration for each space is correct. Use of some SDRAM configurations requires that multiple CE spaces be used. The following CE spaces may be linked together in SDRAM mode depending on the configuration: CE0 and CE1, or CE2 and CE3, or CE0, CE1, CE2 and CE3 If these configurations are used, all of the associated CE spaces must be configured as SDRAM. For more information, see TMS320VC5510 DSP External Memory Interface (EMIF) Reference Guide (SPRU590).

Table 5. Host Port Interface (HPI)

	Issue	Description
☐	HPI errors or HRDY stuck low	The minimum low pulse width and high pulse width for the data strobe ($\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$) is not being met. Refer to the data manual for timing requirements for the HPI.

Table 5. Host Port Interface (HPI) (continued)

☐	HPI errors	HPI transactions cannot be initiated until the previous transaction has been completed as indicated by HRDY. It is recommended to use HRDY since HPI latencies can depend on other CPU and DMA activity.

Table 6. Direct Memory Access (DMA)

	Issue	Description
☐	Delay after enabling DMA channel	After a DMA channel is enabled, the DMA controller copies the channel context registers over to the working set. The working set of registers is used during the actual data movement on the DMA channel. This action causes some latency between the time the DMA channel is enabled and when the first transfer occurs.
☐	DMA channel source and destination appear to be out of sync	The DMA channel FIFO can pre-fetch data from the source to be delivered later when the destination is ready. This can cause the source and destination address counters to appear to be out of sync.

5 Summary

Using the information provided in this document, along with documentation that is pointed out for each step of the design process, a DSP designer will be able to make more knowledgeable decisions concerning their design.

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