TMS320C6412 Hardware Designer's Resource Guide

DSP Hardware Application Team

ABSTRACT

The DSP Hardware Designer's Resource Guide is organized by development flow and functional areas to make your design effort as seamless as possible. Topics covered include getting started, board design, system testing, and checklists to aid in your initial design and debug efforts. Each section includes pointers to valuable information including technical documentation, models, symbols, and reference designs for use in each phase of design. Particular attention is given to peripheral interfacing and system level design concerns.

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1 Getting Started

1.1 Registering on my.TI

my.TI is a customizable area within the Texas Instruments web site. By registering on my.TI, you can receive the following benefits:

- Quick Reference to information you select as part of your profile.
- Email alerts that inform you of updates to products, technical documentation, and errata.
- The my.TI newsletter providing information on the latest innovations and product releases.

To register on my.TI for updates related to the this device:

1. Go to the device product folder.
2. Select the link called “ADD To my.TI” in the upper right hand corner, and follow the on-screen instructions.
3. Select Customize my.TI to specify what you would like to receive notification about.

Use the following link to access the product folder.

TMS320C6412 DSP product folder

1.2 Training and Support

Texas Instruments offers a variety of training options tailored for your specific needs and requirements. Options include on-line training, webcasts, seminars, single and multi-day workshops, and conferences. For more information about training, visit Texas Instruments Training Home. For assistance with technical questions regarding TI Semiconductor products and services, you can access the Semiconductor Technical Support KnowledgeBase .

1.3 Technical Documentation

1.3.1 Where to Start

The key area for obtaining documentation for this device is the product folder. When getting started, it is of great importance to have the latest data sheet and silicon errata. Often, a “Getting Started with” or “How to Begin Development with” application report is available as well. Listed below are links to this key information:

- TMS320C6412 DSP product folder
- TMS320C6412 Fixed−Point Digital Signal Processor Data Manual (SPRS219)
- TMS320C6412 Errata (SPRZ199)

1.3.2 Using TI Literature Numbers

All TI documentation is assigned a literature number. This number can be used to search for the document on the Web. Technical documentation revisions are indicated by the alpha character at the end of the literature number on the title page, and in the file name.

Use the literature number (without the trailing alpha character) to search the TI website for the document. For example, if a data manual has a literature number of SPRS205B, the ”B” indicates the revision of the document. If the document has no trailing alpha character, it is the original version of the document. When searching for this document on the TI web site, you can simply enter ”SPRS205” as the search keyword.

1.3.3 Technical Publication Descriptions

This section describes the content contained in technical publications which support this device. All of the technical publications described below can be found in the device product folder. Check your device product folder frequently for the most recent technical documentation.

Data Sheets and Data Manuals

The Data Sheet or Data Manual is the functional specification for the device. Topics covered in this document include but are not limited to the following:

- High−level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device−specific information about peripherals and registers
- Electrical specifications

Silicon Errata

The Silicon Errata documents exceptions to the functional specification as defined in the Data Sheet or Data Manual.

Reference Guides

Reference Guides provide additional information describing the architecture and operation of hardware components of the DSP platform, generation, or device, beyond the scope of the Data Sheet or Data Manual.

Application Reports

Application Reports are written to describe implementation details specific to a device, peripheral, use of technology, or explanation of usage.

1.3.4 Peripheral Reference Guides

Each peripheral has a reference guide that provides beneficial information for completing a design. Each peripheral and its respective reference guide is listed here. There are two categories. The first category contains peripherals which connect directly to external devices. The second category lists the internal peripherals.

Peripherals that connect directly to external devices:

- TMS320C6000 DSP External Memory Interface (EMIF) Reference Guide (SPRU266)
- TMS320C6000 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide (SPRU580)
- TMS320C6000 DSP General-Purpose Input/Output (GPIO) Reference Guide (SPRU584)
- TMS320C6000 DSP Peripheral Component Interconnect (PCI) Reference Guide (SPRU581)
- TMS320C6000 DSP Host-Port Interface (HPI) Reference Guide (SPRU578)
- TMS320C6000 DSP EMAC/MDIO Module Reference Guide (SPRU628)
- TMS320C6000 DSP Inter−Integrated Circuit (I2C) Module Reference Guide (SPRU175)

Internal peripherals:

- TMS320C6000 DSP Interrupt Selector Reference Guide (SPRU646)
- TMS320C6000 DSP Power-Down Logic and Modes Reference Guide (SPRU728)
- TMS320C6000 DSP Enhanced Direct Memory Access (EDMA) Controller Reference Guide (SPRU234)
- TMS320C64x DSP Two-Level Internal Memory Reference Guide (SPRU610)
- TMS320C6000 DSP 32-bit Timer Reference Guide (SPRU582)

1.3.5 Application Reports

Organized by category and listed below are application reports that provide useful information for designing on this device.

External Memory Interface (EMIF):

- *TMS320C6000 EMIF:Overview of Support of High Performance Memory Technology (SPRA631)*
- *TMS320C6000 EMIF to USB Interfacing Using Cypress EZ-USB SX2 (SPRAA13)*
- *TMS320C6000 EMIF-to-External SDRAM Interface (SPRA433)*
- *TMS320C6000 EMIF to TMS320C6000 Host Port Interface (SPRA536)*
- *TMS320C6000 EMIF to External Flash Memory (SPRA568)*
- *Interfacing the TMS320C6000 EMIF to a PCI Bus Using the AMCC S5933 PCI Controller (SPRA479)*
- *TMS320C6000 EMIF to External Asynchronous SRAM Interface (SPRA542)*
- *TMS320C6000 EMIF to External FIFO Interface (SPRA543)*
- *TMS320C6000 EMIF to External SBSRAM Interface (SPRA533)*

Multichannel Buffered Serial Port (McBSP):

- *TMS320C6000 McBSP Interface to an ST-BUS Device (SPRA511)*
- *Using the TMS320C6000 McBSP as a High Speed Communication Port (SPRA455)*
- *TMS320C6000 McBSP to Voice Band Audio Processor (VBAP) Interface (SPRA489)*
- *TMS320C6000 McBSP: AC'97 Codec Interface (TLV320AIC27) (SPRA528)*
- *TMS320C6000 McBSP Interface to SPI ROM (SPRA487)*
- *TMS320C6000 McBSP: IOM-2 Interface (SPRA569)*
- *TMS320C6000 McBSP: UART (SPRA633)*
- *TMS320C6000 McBSP as a TDM Highway (SPRA491)*
- *TMS320C6000 Multichannel Communications System Interface (SPRA637)*
- *TMS320C6000 McBSP: I^2S Interface (SPRA595)*

Host Port Interface (HPI):

- *TMS320C6000 Host Port to MC68360 Interface (SPRA545)*
- *TMS320C6000 Host Port to the i80960 Microprocessors Interface (SPRA541)*
- *TMS320C6000 Host Port to MPC860 Interface (SPRA546)*

Peripheral Component Interconnect (PCI):

- TMS320C64x DSP Peripheral Component Interconnect (PCI) Performance (SPRA965)

2 Board Design and Layout

2.1 High−Speed DSP Systems Design Reference Guide

Today's digital signal processors (DSPs) are typically run at a 1GHz internal clock rate while transmit and receive signals to and from external devices operate at rates higher than 200MHz. These fast switching signals generate a considerable amount of noise and radiation, which degrades system performance and creates electromagnetic interference (EMI) problems that make it difficult to pass tests required to obtain certification from the Federal Communication Commission (FCC). Good high−speed system design requires robust power sources with low switching noise under dynamic loading conditions, minimum crosstalk between high−speed signal traces, high− and low−frequency decoupling techniques, and good signal integrity with minimum transmission line effects. This document provides recommendations for meeting the many challenges of high−speed DSP system design.

For more information, refer to High−Speed DSP Systems Design Reference Guide (SPRU889).

2.2 Schematics

TI provides CAD symbols in a variety of formats to assist in schematic generation. The symbols are located in the DSP product folder or directly accessible through the link below:

- http://focus.ti.com/docs/prod/folders/print/tms320c6412.html#symbols

2.3 Signal Integrity and Timing Considerations

High-speed interfaces require strict timings and accurate system design. To achieve the necessary timings for a given system, input/output buffer information specification (IBIS) models must be used. These models accurately represent the device drivers under various process conditions. Board characteristics, such as impedance, loading, length, number of nodes, etc., affect signal performance. The following IBIS model is available for this device:

- C6412 GDK/GNZ IBIS Model (IBIS Model)

The following application report discusses how to use IBIS models for timing analysis:

Using IBIS Models for Timing Analysis (SPRA839)

2.4 Board Layout

The significance of electromagnetic compatibility (EMC) of electronic circuits and systems has recently been increasing. This increase has led to more stringent requirements for the electromagnetic properties of equipment. Two property aspects are of interest: the ability of a circuit to generate the lowest (or zero) interference, and the immunity of a circuit to the effects of the electromagnetic energy it is subjected to. The effects on electronic circuits and systems is well documented, but little attention has been paid to circuit behavior and the interference it generates. The following link discusses the important criteria that determine the EMC of a circuit.

Printed-Circuit Board Layout for Improved Electromagnetic Compatibility (SDYA011).

2.5 Power Supply and Sequencing Considerations

Texas Instruments offers several Power Management Products for this device. For a complete list of product offerings, visit the power.ti.com website.

2.6 Power/Thermal Management Considerations

Circuit designers must always consider the effects of heat transfer from a device die to the surrounding package. The flow of heat from the device to ambient must be sufficient to maintain the device temperature as specified in the device data sheet. The thermal resistance characteristics for this device are documented in the data sheet. The following application reports discuss thermal analysis, heat sink selection, and power consumption.

- *TMS320C6x Thermal Design Considerations (SPRA432)*
- *TMS320C6412 Power Consumption Summary (SPRA967)*

2.7 Boot Mode Configurations

The TMS320C6412 has three types of boot modes:

- Host boot
- EMIF boot (using default ROM timings)
- No boot

At /RESET, the DSP uses EMIFA address pins 21 and 22 for selecting one of the boot modes. Boot mode bit 0 maps to EMIFA address pin 21 and boot mode bit 1 maps to EMIFA address pin 22. To select the boot modes use the following table.

Boot Mode AEA[22:21]	Boot Process
00	No boot (default mode)
01	HPI/PCI boot (based on PCI_EN pin)
10	Reserved
11	EMIFA boot

For more information, please refer to the data sheet and the following application reports.

- *TMS320C6000 Tools: Vector Table and Boot ROM Creation (SPRA544)*
- *TMS320C6000 Boot Mode and Emulation Reset (SPRA978)*

2.8 Joint Test Action Group (JTAG) Emulation Interface

DSP devices have a JTAG interface that allows for emulation hardware and software to communicate with the DSP. The JTAG port also supports boundary scan testability. For information about emulation capabilities, emulation technical documentation and products, see the emulation tools product folders below:

If you are using the TI XDS510 emulator, go to:

XDS510 product folder

If you are using the TI XDS560 emulator, go to:

XDS560 product folder

If you are using a third−party emulator, contact the emulator manufacturer.

2.9 Board Manufacturing

When designing with a high−density BGA package, it is important to be aware of different techniques that aid in the quality of manufacturing. The following documentation discusses board manufacturing considerations:

Flip Chip Ball Grid Array Package Reference Guide (SPRU811).

3 System Test

3.1 Boundary Scan Description Language (BSDL) Model(s)

BSDL models can be used to perform board interconnect tests as well as other board level diagnostics and functions. Boundary scan tests require that each scan device on the board be described in the Boundary Scan Description Language (BSDL) model. Depending on the available silicon, more than one BSDL model may be available. The following BSDL models are available for this device:

- C6412 GNZ BSDL Model
- C6412 GDK BSDL Model

4 Checklists

4.1 Design Checklist

The Design Checklist was put together by Texas Instruments application and field support staff as a guide to considerations made during the design phase of development. Use this check list to keep track of considerations you make during the design phase of development.

☐	Check the data sheet and errata for the most up to date information.
☐	Are decoupling capacitors placed on the board near the DSP? Voltages from traces on a printed circuit board can couple to each other in places where it is not desired, (like power supply planes). To decouple the traces, we add capacitors to absorb some of the voltage and help reduce this effect. For more information on how to correctly place decoupling caps, see the data sheet section for power-supply decoupling.
☐	Are there provisions for power sequence? To operate properly, the DSP needs to be powered up in the correct sequence. Check the sequencing for power, according to data sheet specifications.
☐	Voltage levels changes? The board should be able to accommodate some voltage level changes. It can be useful to accommodate some changes by simply changing a resistor.
☐	Are the CLKMODEx pins configured correctly? In addition to checking the CLKMODE[1:0] pins to see if they are set up to generate the correct frequency, the CLKOUT4/6 pins should be checked with an oscilloscope. To do this, you must clock EMIFA. If the CLKOUT4/6 signal is correct, this verifies lock of the PLL, in addition to the correct frequency of operation for your DSP. If the CLKOUT4/6 signal is not correct, check that the PLL and the CLKMODE pins are configured correctly. Does the PLL have the correct circuitry around it, following the data sheet recommendations?
☐	Are there provisions for changing the clock during debug time? It can be very helpful to set up a jumper on your board to change the clock frequency. This can allow you to detect whether or not problems are related to the high clock rate.

☐	Reset circuitry? For debugging it is important to be able to reset the DSP when/if it gets into an unstable state. To perform this, one of the easiest things to do is to have a reset button on the board itself. For information on proper reset circuitry, see the Reset Circuit for the TMS320C6000 DSP (SPRA431) . Having a reset supervisor on board enables you to do things like monitor the supply rails for sags in power. The TPS3110 class of devices is the most commonly used reset supervisors from TI.
☐	Are boot mode pins configured correctly? The three boot modes for the C6000 devices are: no boot, boot over the HPI, or boot from a ROM device located at Chip Enable Space 1. Check the definition for these modes in the Boot loading Guide section of this document and choose the correct configuration you need. It is very useful to include the ability to choose an alternate boot configuration. Use unpopulated resistor pads to allow the choice of different boot modes.
☐	Are the AARDY pins used? If using asynchronous RAM, make sure AARDY (EMIFA) is being used appropriately. If NOT using asynchronous RAM, the pins are pulled up internally.
☐	Is the HOLD/HOLDA method being used? If using asynchronous RAM, make sure $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ are used properly. If NOT using asynchronous RAM, make sure the NOHOLD bit in GBLCTL register is set to 0.
☐	Are the HDS/HAS signals correctly configured to access the DSP? If using the HPI, then you have a choice of configurations. Examples of timing diagrams for when $\overline{\text{HAS}}$ is used or unused (tied high) are in TMS320C6000 DSP Peripherals Overview Reference Guide (SPRU190). Also, there is a choice on how to assert $\overline{\text{HSTROBE}}$ using both, one, or none of the $\overline{\text{HDS1/2}}$ in combination with $\overline{\text{HCS}}$. The gate logic for these pins should be checked in the aforementioned HPI reference guide as well.
☐	Is the emulation configured properly? Check to make sure EMU[1:0] pins are connected according to your needs. The JTAG port can function in one of two ways, emulation mode or boundary scan mode. The table below documents the selection based on EMU[1:0] pins. **EMU[1:0]** — **Operation** 00 — Boundary Scan/Normal Mode 01 — Reserved 10 — Reserved 11 — Emulation/Normal Mode **NOTE:** Check the data sheet for more information about these pins. To use with Code Composer Studio, Emulation/Normal mode should be selected. $\overline{\text{TRST}}$ has an internal pull-down, though it may be useful to include an external pull-down. In the future, TI will be switching to more advanced emulation using a 60-pin header instead of the traditional 14-pin. See the aforementioned *60-Pin Emulation Header Technical Reference* for details. For now, leave the extra emulation pins EMU[11:2] unconnected because they have internal pull-ups. For full details on designing with JTAG, *IEEE Std 1149.1 (JTAG) Testability Primer (SSYA002)* The IEEE Std 1149.1 (JTAG) Testability Primer provides additional information that is useful. These resources will allow you to check your JTAG circuitry for correctness.

☐	Are the McBSP signals pinned to via for scope trace? For debugging information it can be very useful to have the McBSP signals pinned out to a via. This allows you to check the signals (clock, frame sync, data, etc.,) on a scope for correct operation.
☐	Do the DSP vias go all the way through the board? For debugging information it can be very useful to have the McBSP signals pinned out to a via. This allows you to check the signals (clock, frame sync, data, etc.) on a scope for correct operation. It is extremely helpful to have the DSP pins available through all layers. This will increase the layout difficulty. However, this will also allow visibility into all possible pins on the DSP, which can be a useful for debug.
☐	How much general visibility is there on the board? If space allows it, the more signals and pins that are accessible, the easier it is to debug. One common consideration is adding hooks for a logic analyzer on the EMIF bus. This can help with any timing issues that might come up during development.
☐	Are there any GPIOs pinned out to via or LED for probing? GPIOs can be very useful for debugging. If a GPIO pin is available for use, it is worthwhile to pin it out to a via or an LED to observe the operation.

4.2 Debug Checklist

☐	Are the power supplies clean? Noisy supplies can create several problems in your system. Be sure that your power supplies are working as expected.
☐	Do EMIF timings match the data sheets? The data sheets for both the DSP and the external memory device should have timing diagrams. Check the timings from the point of view of both the DSP and external memory, and make sure the signals match their respective data sheets. An IBIS model can also be used to examine timings.
☐	Are the EMIF Clocks set up properly? To interface correctly with external memory like SDRAM, check the specifications for your memory's speed, then set the clock to the EMIF. Three options exist for the EMIF clock: CPU/4, CPU/6, or external ECLKIN. Check clocks with a scope for proper frequency.
☐	Are the CE spaces configured correctly? Using the EMIF control registers for each CE space make sure that each space is configured for the appropriate form of external memory. *Important note:* If booting from ROM, the ROM device needs to be on CE1, since the on-chip boot loader automatically looks there to start a ROM boot.
☐	Is the scan chain length set correctly? If the scan chain length is not detected properly on your board, Code Composer Studio will not correctly recognize power to the DSP. If it is a multiprocessor board, a scan chain test should return the correct number of devices.

☐	If it is a multiprocessor, is the TDI/TDO connection tied properly? In multiprocessor environments, the TDI (JTAG test-port data in) and TDO (JTAG test-port data out) pins need to be tied correctly. The TDI pin on the JTAG header should tie to the TDI pin on the first DSP, and the TDO pin on the first DSP should tie to the TDI pin on the second DSP. This sequence should continue for subsequent DSPs, until the TDO pin of the last DSP connects to the JTAG header's TDO pin. For more information on designing for JTAG emulation, see Chapter 16 of TMS320C6000 Designing for JTAG Emulation Reference Guide (SPRU641).
☐	If you can launch Code Composer Studio are you able to access the CPU registers? A good test to see if the emulation software can communicate with the DSP is to launch Code Composer Studio and then select the CPU registers from the toolbar and modify an A-side or B-side register.
☐	Simple memory accesses can be performed with no code. Before you have code available you can test memory accesses using Code Composer Studio. A simple method of doing this involves selecting the EMIF registers view from the toolbar in Code Composer Studio and setting these registers to their appropriate value based on the type of memory you will access. You can then open a memory window from the toolbar and read or write the memory of interest.

5 Summary

Using the information provided in this document, along with documentation that is pointed out for each step of the design process, a DSP designer will be able to make more knowledgeable decisions concerning their design.

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