

TMS320VC5503/C5506/C5507/C5509A Power Consumption Summary

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ABSTRACT

This document assists in the estimation of power consumption for the TMS320VC5503/C5506/C5507/C5509A digital signal processors (DSPs). Power consumption on these devices is highly application-dependent, so a spreadsheet is provided to model power consumption. The spreadsheet allows you to enter parameters that closely resemble the application and generate a realistic estimate of DSP power consumption based on your input. It also allows designers the ability to test the efficiency of different configurations before any hardware is assembled or any code is written.

The spreadsheet discussed in this application report can be downloaded from the following URL: <http://www.ti.com/lit/zip/SPRAA04>. Although this spreadsheet was developed for the C5509A device, it can be used to model power consumption on the C5503, C5506, and C5507. Features not supported on these devices should not be enabled in the spreadsheet.

1 Activity-Based Models

Power consumption of the TMS320VC5503/C5506/C5507/C5509A is application-dependent. This means the power consumption for a particular application depends on the level of CPU and peripheral activity models. You must have a clear understanding of the CPU, the peripherals, and the I/O activity levels of the application to get a realistic result. The output of the power estimation spreadsheet can aid in power supply design or battery life prediction.

The model used in this spreadsheet is based on two modes of power consumption: static and active power. With this approach, each of the DSP components (CPU, peripherals, and I/O pins) can be isolated to determine its contribution to the overall power consumption.

1.1 Static Power

Static power is the consumption when the on-chip oscillator is shut down (clock generation domain is idle). If an external clock source is used instead of the on-chip oscillator, the static power is consumed when the external clock source is stopped; therefore, no activity on the DSP is being clocked. The static power consumption depends purely on core and I/O, and the device operating temperature.

1.2 Active Power

Active power is the consumption of the active parts of the DSP. These include the CPU, the peripherals, and I/O pins associated with these peripherals. The active power consumption is based on the supply voltages, operating frequency, and the given configuration of each peripheral. To get a better understanding of the distribution of the active power consumption, each module can be evaluated independently.

The parameters used to describe each module activity are:

- *Frequency* is the operating frequency of a module or it is the operating frequency of the interface to that module.
- *Idle Status* indicates whether the module is in idle or in active state.
- *%Utilization* is the percentage of activity in a module relative to its maximum.
- *%Write* is the percentage of writes relative to the total number of transfers. Remaining transfers are treated as reads.
- *Bits* is the number of data bits in use on an interface that supports variable-width busses.
- *% Switch* is the probability that a data bit will switch from one cycle to the next.
- *Trace Length* is the average of the total board trace length being driven by each pin of the particular peripheral.
- *Load Capacitance* is the total capacitive load seen by each pin of the particular peripheral.

However, each module may not include all of these parameters.

1.3 Modules

Each of the following modules and sub-modules are user-configurable in the power estimation spreadsheet within realistic operating parameters.

- CLKGEN (DPLL-lock mode only)
- Central Processing Unit (CPU) and CLKOUT
- External Memory Interface (EMIF) (SDRAM and ASRAM mode)
- Direct Memory Access (DMA) (6 channels)
- Host-Post Interface (HPI) (Non-multiplexed mode only)
- Multichannel Buffered Serial Port (McBSP0), McBSP1, and McBSP2
- MultiMedia Card (MMC1) and MMC2
- Secure Data (SD1) and SD2
- Inter-Integrated Circuit (I2C)
- Timer0 and Timer1
- Watchdog Timer (WDT)
- Analog-to-Digital Converter (ADC)
- Real-Time Clock (RTC)
- General-Purpose Input/Output (GPIO/XF)

2 Using the Power Estimation Spreadsheet

To use the spreadsheet, enter the usage parameters in the white cells. To ensure that the data validation feature limits the input to realizable configurations, enter values from left to right, top to bottom. The spreadsheet takes the entered information and displays the power consumption details for that configuration.

To make the operation simple, the spreadsheet does not support more than one idle configuration at any given time. For applications where the idle status is constantly changing, each possible configuration should be estimated independently. For battery life predictions, the estimations from all configurations can be time-averaged to determine the overall device-current requirement. Power supply design should take into account the configuration that consumes the maximum power since a power supply must support peak requirements.

Although the spreadsheet was developed for the VC5509A device, it can be used to model power consumption on the VC5503, VC5506, and VC5507. Features not supported on these devices should not be enabled in the spreadsheet.

2.1 Choosing Appropriate Values

The accuracy of the power estimation spreadsheet result depends on how closely the parameters entered match with those of the actual system. Each module must be considered separately for a given process and you must account for all activity a given operation may include. For instance, EMIF activity is not included in the CPU activity when the code is being executed from external memory. The EMIF activity must be included separately in the EMIF section of the spreadsheet.

2.1.1 Frequency

In some cases the frequency parameter for a particular module denotes the output frequency of that module. For others, it denotes the internal operating frequency of the module.

2.1.1.1 CLKGEN (DPLL)

The CLKGEN or DPLL frequency is simply the output frequency of the clock generator in the DPLL-lock mode. The bypass mode of the clock generator is not supported. The DPLL synthesized is distributed to the CPU and the peripheral. Some of the peripheral's internal logic runs at the same rate as the CPU. Other peripherals support a user-configurable pre-scaler to run the module at an integer fraction of the CPU clock. For example, the DMA internal logic runs at the same rate as the CPU, but the I2C or the MMC/SD modules can be programmed to run its internal logic (state machine) at a much slower speed. The clock frequency of the DPLL and module clocks should not be set in a manner that violates the frequency restrictions imposed by the device data sheet and module reference guide.

2.1.1.2 CPU and CLKOUT

The clock frequency of the CPU is automatically set to the frequency DPLL output. The default CLKOUT frequency is the same as the CPU clock unless the CLKOUT frequency is divided down by programming the system register (SYSR).

2.1.1.3 EMIF

In case of synchronous memories (e.g., SDRAM), the frequency field represents the EMIF CLKMEM frequency. For asynchronous memories (e.g., ASRAM), this frequency field should be set equal to the CPU clock frequency. External clocking of the EMIF is not supported.

2.1.1.4 HPI

The internal operating frequency of the HPI is automatically set to the CPU clock and not user-configurable.

2.1.1.5 DMA

The internal operating frequency of the DMA is automatically set to the CPU clock and not user-configurable.

2.1.1.6 McBSP

The frequency field indicates the frequency of transmit or receive clocks (CLKX or CLKR).

2.1.1.7 MMC

Frequency field, in this case, indicates the frequency at which the MMC controller operates or the function clock frequency.

2.1.1.8 SD

Frequency field, in this case, indicates the frequency at which the SD controller operates or the function clock frequency.

2.1.1.9 I2C

Frequency field, in this case, indicates the I2C module clock frequency. This field only accepts values between 7 MHz and 12 MHz.

2.1.1.10 Timer

Frequency, in this case, indicates the output frequency or the periodic frequency. The timer output frequency depends on the timer pre-scaler and the period register values. Note that Timer 1 does not have an output pin; therefore, it does not affect the I/O power consumption.

2.1.1.11 USB

The universal serial bus (USB) internal clock is set to 48 MHz and is not made user-configurable on the spreadsheet.

2.1.1.12 WDT

In the spreadsheet, none of the usage parameters are configurable on the WDT module. The current consumed by the WDT alone while active and running is extremely small, therefore, its contribution to the total current consumed by the device is assumed to be negligible.

2.1.1.13 ADC

ADC clock frequency field is not user-configurable on the spreadsheet.

The current version of the spreadsheet estimates ADC current consumption with ADC programmed for the maximum sampling rate of 21.5 KHz. To minimize the power consumption of the ADC state machine, the ADC clock should be programmed lowest possible frequency. Therefore, the ADC power consumption values are provided at a fixed setting of ADC clock frequency at 4 MHz (lowest possible) and ADC conversion clock frequency programmed to be 2 MHz.

For simplicity, the current measured at the A/D module digital voltage pin (ADV_{DD}) is lumped into the column for the device I/O current column (DV_{DD}) in the spreadsheet.

2.1.1.14 RTC

Default RTC frequency is 32.768 KHz and not user-configurable. Additionally, in the spreadsheet none of the usage parameters are configurable on the RTC module. The current consumed by the RTC alone, while active and running, is extremely small and is primarily affected by whether or not the DSP is in standby mode. Therefore, its contribution to the total current consumed by the device is accounted for statically. Furthermore, to simplify the RTC core and I/O current consumption it is lumped together as $RTCV_{DD}$ in the spreadsheet.

2.1.1.15 GPIO/XF

The frequency input for GPIO and XF indicate the frequency at which the GPIO pins states are updated.

2.1.2 Idle Status

Idle status for a given module is used to specify whether or not that module is configured by software to be in its idle state. The spreadsheet only supports one idle configuration at any time.

The spreadsheet should not be programmed in a manner that enables mutually exclusive peripherals at the same time. For example, both the EMIF and EHPI should not be enabled at the same time.

Similarly, on the serial ports, the spreadsheet only allows one of the modules from McBSP1, MMC1 or SD1 and McBSP2, MMC2 or SD2 to be active at any time. Trying to enable more than one module multiplexed on Serial Port 1 and 2 zeros out the current/power consumption fields on the spreadsheet.

2.1.3 % Utilization

Utilization is explicitly defined for each module to provide a more accurate estimate of power consumption. If a module is not listed, then it is assumed to be in use whenever it is not idle or in some cases, like RTC and WDT, the contribution of the modules, while active and being maximally utilized, is small enough to be neglected as compared to the total current consumed.

2.1.3.1 CPU

Since the CPU can be involved in a wide range of activities, it is difficult to provide an exact CPU utilization number. Whenever the CPU is active (non-idle), it is executing some type of instructions. For this reason, 0% activity is assumed as a repeated NOP instruction - the smallest amount of power the CPU can consume while active. Conversely, 100% activity is assumed as the most power-intensive instruction - the dual multiply and accumulate. All other instructions fall somewhere in between. No single algorithm will achieve 100% utilization, but some highly-optimized functions can come close. On the other hand, when the CPU performs control-oriented tasks, it consumes far less current.

Let us, for example, assume that a certain application executes control code half of the time and a highly optimized algorithm for the other half. If the control code is estimated to be at 30% utilization and the dense DSP code is estimated to be at 90% utilization, the overall utilization would be 60% ($30\% \times 50\% + 90\% \times 50\%$). If the application spent more time executing the optimized algorithm, utilization would obviously go up, and vice versa. Examining individual segments of an application and estimating the time spent and the CPU utilization in each segment can provide a more accurate percentage of the CPU utilization.

2.1.3.2 EMIF

EMIF utilization is related to the maximum bandwidth of the EMIF. One hundred percent utilization corresponds to the maximum transfer rate for a given frequency when doing these types of transfers. This number will be scaled down by both slower and less frequent transfers.

In case of SDRAM, for writes, 100% utilization or maximum throughput is 1 16-bit word/cycle (with write posting enabled) and for reads 100 % utilization or maximum throughput is 2 16-bit words / 10 cycles. (EMIF is configured to communicate with the SDRAM using the divide-by-1 clock mode, i.e., CLKMEM equals the CPU clock frequency.) In case of asynchronous memory, the maximum throughput rate possible for read/writes is 1 16-bit word/ 2 CPU cycles and is defined as 100% utilization.

The utilization percentage is defined as the throughput of the application under question, divided by the maximum throughput rates as defined above. For example, CPU reading data from SDRAM at the rate of a 16-bit word every 20 cycles yields 20% EMIF utilization.

2.1.3.3 HPI

HPI utilization is related to the maximum bandwidth based on the HPI accesses time of 20 CPU cycles per 16-bit word read or write. The DSP running at 200 MHz, is equivalent to 10 Mwords per second.

2.1.3.4 DMA

DMA utilization for a given channel is based on the maximum attainable data transfer rate between the SARAM and DARAM port, which is one 32-bit transfer per CPU cycle. 20% DMA channel utilization would yield one 32-bit transfer per 5 CPU cycles.

2.1.3.5 McBSP

McBSP utilization is defined as the percentage of time that the McBSP is transferring data. The rest of the time the McBSP is assumed to be not transferring any data.

2.1.3.6 MMC

MMC utilization is based on the maximum attainable data transfer rates. The maximum data rate the MMC can support is 2.4 Mbytes/sec, which is defined as 100 % utilization for the MMC module. The utilization percentage is defined as the data rate of the application under question, divided by the maximum data transfer rate.

2.1.3.7 SD

SD utilization is based on the maximum attainable data transfer rates. The maximum data rate the SD can support is 12.5 Mbytes/sec, which is defined as 100 % utilization for the SD module. The utilization percentage is defined as the data rate of the application under question, divided by the maximum data transfer rate.

2.1.3.8 USB

USB utilization is based on the maximum attainable data transfer rate between the DSP memory and the USB host device. This was calculated to be realistically around 8 Mbytes/sec (the rest being overhead). Therefore a 25% utilization would yield a data rate of 2 Mbytes/sec.

2.1.3.9 I2C

I2C maximum utilization is defined as maximum data transfer of 400 Kbps. For example, if the I2C is module configured for data transfer rate of 10 Kbps, it will yield 2.5% utilization.

2.1.3.10 Timer

Timer utilization is defined as the percentage of time that the timer is counting.

2.1.3.11 ADC

ADC utilization is defined as the percentage of time that the ADC is performing the analog-to-digital conversion.

2.1.3.12 GPIO/XF

Utilization for general-purpose outputs is the percentage of time that they are switching at their specified frequency.

2.1.4 % Writes

For modules that move data onto a bus, % writes is defined as the percentage of utilization in which the peripheral is putting data on the bus. The rest of the bus utilization period is assumed to as read operation. For modules with equal input/output activities, the write percentage should be 50%.

2.1.5 Bits

Bits is the number of data bits on a variable width bus. For serial ports, such as McBSP, this number indicates the size of the serial data units. For HPI, this field is fixed at 16 bits.

2.1.6 % Switch

Random data has a 50% chance that any bit will change from one cycle to the next. Some applications may be able to predict this change using some a priori information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. All other applications should use the default number of 50%.

Typically, switching in the EMIF data lines is the dominant factor in the EMIF I/O power consumption. The effect of the address and control lines is minimal.

2.1.7 Trace Length

The trace length parameter indicates the average length of controlled-impedance board trace of each output for a given interface (assumed 50W trace). This only affects I/O power and further, only makes significant contribution when the module is writing.

In case of USB, the trace length is replaced with the USB cable length.

2.1.8 Load Capacitance

Load capacitance is the average of the sum of the input capacitances of all external devices connected to a given module's output. This parameter should be obtained from the data sheets of the devices that are connected to the DSP and the board trace capacitance.

2.1.9 Other

Some modules have additional parameters for a more granular estimation of the power consumption. They are:

2.1.9.1 EMIF

Select between synchronous (sync) and asynchronous (async) memory.

2.1.9.2 McBSPs

This field allows choosing whether the McBSP is being clocked from the internal CPU clock (internal) or from an external clock source (external).

2.1.9.3 Timer0

This field is used to select if the timer pin is configured as input (TOUT disabled) or as an output (TOUT enabled).

2.1.9.4 GPIO/XF

The input to this field is the number of GPIO pins configured as outputs.

2.1.10 Units

The results are estimated in the spreadsheet and displayed in milliamps (mA) or milliwatts (mW). Click the units in the Total row of the calculated results and use the pull-down menu to select the desired units.

2.2 Graphs

The graphs included in the spreadsheet show the relative contribution of total core and I/O power for each module. They provide a visual display of power usage and allow easy identification of the major power consumers.

3 Using the Results

The results presented in the spreadsheet are based on measured data with revision 1.1 silicon. The measured units were selected based on the high end of power consumption limits for production units. Most production units will typically consume power that is below the value given in the spreadsheet, if correctly used. Transient currents can cause power to spike above the estimated value for short periods, but long term power consumption should be below the spreadsheet value. This allows for better estimates of power supply requirements and more accurate battery life predictions.

4 Examples

The examples below demonstrate how to choose the values for the power estimation spreadsheet for two sample applications running on C5509A. The values can be filled into the spreadsheet by clicking the Sample Application 1 and Sample Application 2.

4.1 Sample Application 1

In this example, the DSP is running a highly-optimized MP3 decoding algorithm. The encoded data is transferred from a multimedia card (MMC) to the DSP internal memory using a DMA channel at the rate of 128 Kbps. The decoded audio data is transferred to the McBSP using another DMA channel, and the decoded audio stream is sent out via an AIC23 audio codec and is played back at 44.1 KHz sampling rate. The audio codec is interfaced to the DSP using a McBSP port for data and I2C for control.

The AIC23 is operating in the master-mode and its interface configured to inter-IC sound (I2S), i.e., it is providing the SCLK of 1.41 MHz ($44.1 \text{ KHz} * 32$) to the CLKX pin and the LRCOUT of 44.1 KHz for the frame synchronization.

- Temp: 25°C
- CV_{DD} : 1.6 V
- CLKGEN (DPLL): 72 MHz
- CPU: 75% utilization
 - CLKOUT off
- DMA
 - Channel 0: 0.06 % utilization, 32-bit element , 100% switching (for internal memory to McBSP0 transfers)
 - 1 32-bit word every 32 cycles at 1.41 MHz ($32 * 44.1 \text{ KHz}$) divided by 1 32-bit word every cycle at 72 MHz (DMA frequency) yields about 0.06% utilization.
 - Channel 1: 0.005% utilization, 16-bit element, and 100% switching (for MMC to internal memory transfers)
 - MMC data transfer rate 128 kbps divided by maximum DMA transfer rate of 2304 Mbps ($72 \text{ MHz} * 32\text{-bit}$), yields about 0.005% utilization.
- McBSP0: 1.41 MHz , 100 % utilization, 32-bit element, 100 % switching, External clock source (AIC23)
- MMC1: 5.3 % utilization , 36 MHz (MMC controller or function clock frequency), 0 % writes (all reads), 100 % switching
 - MMC transferring data transfer rate 128 kbps divided by 2.4 Mbps (maximum data throughput rate for MMC on C5509A) yields about 5.3% utilization.
- I2C: Active, 0% utilization. Since I2C is used for control interface for the AIC23, the throughput rate for control data is very small, therefore its utilization is considered negligible.
- All other peripherals are Idled and have 0% utilization.
- Assumed load capacitances and trace lengths are shown in the spreadsheet.

Entering these values in the spreadsheet gives us current consumption of about 54.8 mA for the core and about 2.377 mA for I/O (includes DV_{DD} , $USBV_{DD}$ and $RTCV_{DD}$).

Note: Since the above application is running at a CPU speed of 72 MHz, a 25% current savings can be achieved by operating it at 1.2 V instead of 1.6 V. The core current consumption for the above application running at 1.2 V CV_{DD} yields 41.2 mA core current consumption. The I/O current remains unchanged.

4.2 Sample Application 2

In this example, the DSP is running a highly optimized algorithm while several DMA channels move data to and from several peripherals. The CPU is executing code completely from within the on-chip RAM leaving the EMIF free for data transfers.

One DMA channel is being used to move data out to external SDRAM at maximum throughput rate and

divide-by-2 clock mode (CLKMEM is half the CPU clock frequency). The EMIF is configured for 16-bit synchronous mode. Two McBSPs are being used to shift 32-bit data in and out of the internal memory at 20 MHz, one of them being driven by external clock. Two DMA channels servicing the McBSPs. Timer 0 is generating a 5 MHz clock. A DMA channel transfers data within internal memory using Timer 1 event at 25 MHz. The USB module is being used by an external USB host is reading data from the DSP memory (IN transfers) at a rate of 2 Mbytes/sec.

- Temp: 25°C
- CLKGEN (DPLL): 200 MHz
- CV_{DD}: 1.6 V
- CPU: 75% utilization
 - CLKOUT Disabled
- EMIF: 100 MHz, 50% utilization, 100% writes, 16-bits, 75% switching
 - Utilization
 - Maximum EMIF throughput for SDRAM : 1 16-bit word every CPU cycle if EMIF configured for divide-by-1 operation
 - EMIF throughput for SDRAM configured for divide-by-1 operation, 1 16-bit word every 2 CPU cycles
 - Dividing the throughput by maximum attainable throughput yields 50% utilization
- DMA
 - Channel 0: 25 % utilization, 16-bit element, 75% switching (for internal to external memory transfer)
 - One 16-bit element every cycle at 100 MHz (EMIF frequency) divided by 1 32-bit element every cycle at 200 MHz (DMA frequency) yields 25% utilization of the DMA channel writing to external memory.
 - Channel 1 : 0.31 % utilization, 32-bit element , 50% switching (for McBSP0 to internal memory transfers)
 - One 32-bit element every 32 cycles at 20 MHz (McBSP frequency) divided by 1 32-bit element every cycle at 200 MHz (DMA frequency) yields about 0.31% utilization.
 - Channel 2 : 0.31 % utilization, 32-bit element , 50% switching (for internal memory to McBSP1 transfers)
 - One 32-bit element every 32 cycles at 20 MHz (McBSP frequency) divided by 1 32-bit element every cycle at 200 MHz (DMA frequency) yields about 0.31% utilization.
 - Channel 3: 10% utilization, 32-bit element, 50% switching (for internal memory to internal memory transfers using Timer 1 event)
 - One 32-bit element every Timer 1 event (20 MHz) divided by one 32-element every cycle at 200 MHz (DMA frequency) yields about 10% utilization.
- McBSP0: 20 MHz, 100% utilization, 32-bit element, 50% switching, internal CPU clock driven.
- McBSP1: 20 MHz, 100% utilization, 32-bit element, 50% switching, external clock driven.
- Timer 0: 5 MHz, 100% utilization, TOUT enabled
- Timer 1: 20 MHz, 100 % utilization
- USB: 25% utilization, 100% switching, 6-foot cable
 - Data transfer rate of 2 Mbytes/sec divided by maximum data transfer rate of around 8 Mbytes/sec, yields a utilization percentage of about 25%.
- All other peripherals are idled, and have 0% utilization.
- Assumed load capacitances and trace lengths are shown in the spreadsheet.

Entering these values into the spreadsheet gives current consumption of about 201 mA for the core, about 25 mA for the I/O , along with 4.15 mA for USB I/O (measured at USBVDD pin) and 50 uA for RTC (core and I/O combined).

5 References

- *TMS320VC5509A Fixed-Point Digital Signal Processor Data Manual* ([SPRS205](#))
- *TMS320C55x DSP Peripherals Overview Reference Guide* ([SPRU317](#))
- *TMS320VC5510 Power Consumption Summary* ([SPRA972](#))
- *TMS320VC5501/02 Power Consumption Summary* ([SPRA993](#))

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