Application Report
SPRA997B–September 2008

Using the USB APLL on the TMS320VC5506/C5507/C5509A

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ABSTRACT

This document describes how to switch to and program the unisersal serial bus (USB) analog phase-locked loop (APLL) on the C5506/C5507/C5509A devices. Example assembly programs for programming and switching to and from the APLL are also provided in the attached zip file. It is assumed that the reader is familiar with the use and operation of the C5506/C5507/C5509A USB digital phase-locked loop (DPLL) and C55x™ Digital Signal Processor (DSP) IDLE procedures.

Project collateral and source code discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/SPRA997.

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1 Introduction

The TMS320VC5506/C5507/C5509A USB peripherals can be clocked from either the USB APLL or the USB DPLL. Since the APLL is inherently more noise tolerant and has less long-term jitter than the DPLL, it is recommended that you switch to it for any USB operations.

2 The C5506/C5507/C5509A Clocking Architecture

The C5506/C5507/C5509A includes a DSP clock generator and a USB clock generator. Both clock generators are sourced from an input clock signal connected at the CLKIN pin. The USB clock generation circuit consists of a DPLL and an APLL; either can be enabled or disabled. The DSP clock generator circuit only contains a DPLL. Figure 1 shows a high-level view of the C5506/C5507/C5509A clocking architecture. The power-up default USB clock is the bypass clock. The power-up default USB PLL is the DPLL.

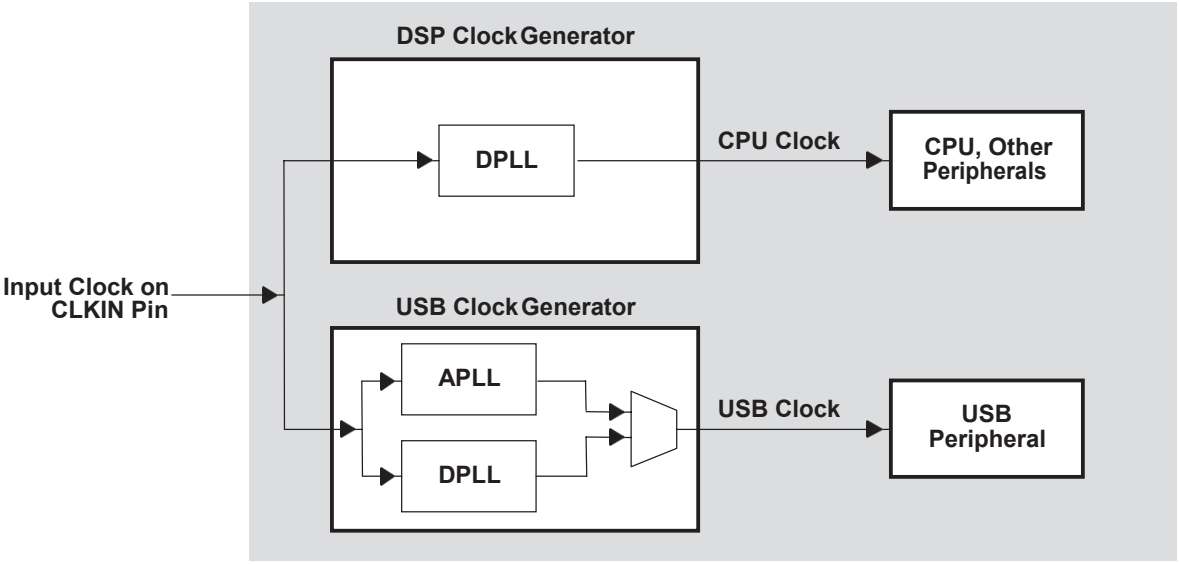
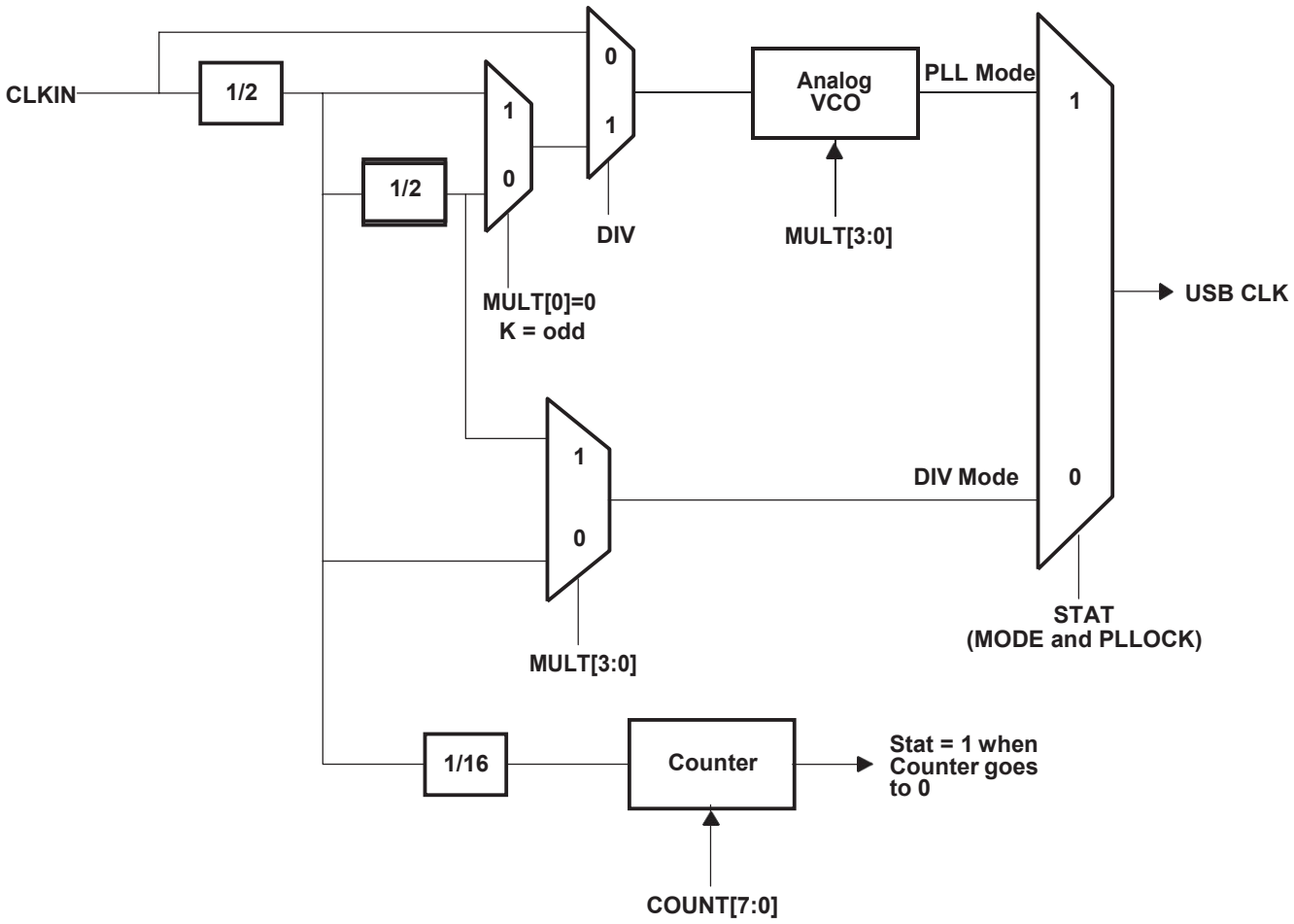


Figure 1. High-Level View of C5506/C5507/C5509A Clocking Architecture

3 APLL Overview

The purpose of the APLL is to generate the USB APLL output clock signal from the external input clock signal (CLKIN). Figure 2 shows a system diagram of the USB APLL. The APLL clock generator can be configured in one of two modes.

- DIV Mode - CLKIN/2 or CLKIN/4. The external input clock signal, CLKIN, is divided by 2 or 4.
- PLL Mode - CLKIN multiplied by one the 31 possible ratios from 0.25 to 15.



A SeeTable 2 for setting MULT[3:0] values. For setting APLL multiply values, see Table 1.

Figure 2. APLL System Diagram

3.1 APLL Operation in DIV Mode

The APLL is set to DIV Mode when the PLL is disabled (MODE=0 and PLLOCK=0). In DIV mode, if the K factor is set to a value other than 16 (MULT[3:0]=0xF), then the frequency of the USB APLL clock output is equal to the input clock frequency divided by 2. If the K factor is set to 16 (MULT[3:0]=0xF), then the frequency of the USB APLL clock output is equal to the input clock frequency divided by 4.

3.2 APLL Operation in PLL Mode

The APLL is set to PLL mode when the PLL is enabled (MODE=1 and PLLOCK=1). In PLL mode, the USB APLL clock output frequency is given by:

$F_{USBAPPLLCLK} = F_{CLKIN} \times (M/D)$

where the multiplication factor is M and the dividing factor is D.

4 USB APLL Register (USBAPLL)

All the different clock modes are programmable by software by programming the USBAPLL register. The USB APLL register (USGAPLL) is located at I/O address 0x1F00 and contains the control bits as shown in Figure 3 and described in Table 1.

Figure 3. USB APLL Register (USBAPLL)

15 12	11	10 3	2	1	0
MULT	DIV	COUNT[7:0]	ON	MODE	STAT
R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1. USB APLL Register (USBAPLL) Field Descriptions

Bit	Field	Value	Description
15-12	MULT[3:0]		PLL multiply factor - Defines the PLL frequency multiply factor K as shown below: MULT[3:0] K 0000 1 0001 2 0010 3 0011 4 0100 5 0101 6 0110 7 0111 8 1000 9 1001 10 1010 11 1011 12 1100 13 1101 14 1110 15 1111 16 Note: MULT[3:0] is set to a K-1
11	DIV		PLL mode divide factor - In conjunction with multiply factor K (see Table 2), defines the PLL frequency divide factor D.
10-3	COUNT[7:0]		PLL lock count - A counter that starts decrementing from its preset values as soon as MODE is set to HIGH.
2	ON		PLL on - Enables the APLL internal VCO. Both ON or MODE force operation of the PLL VCO. ON MODE Analog VCO 0 0 OFF 1 0 ON 0 1 ON 1 1 ON
1	MODE		PLL mode/Not DIV mode - Sets the clock generator mode to PLL when HIGH and to divider (Div) when LOW.
0	STAT		PLL lock status - Indicates the mode of the APLL clock generator.
		0	DIV mode, the system clock is the input clock divided by 2 or 4
		1	PLL mode, the system clock is the input clock multiplied by the PLL multiplication ratio.

DIV, combined with MODE and K, defines the PLL multiplication ratio M/D as indicated below. The USB APLL clock frequency is then given by:

$F_{USBAPPCLK} = F_{CLKIN} \times (M/D)$

The multiplication factor M and the dividing factor D are defined in Table 2.

Table 2. M and D Values Versus MODE, DIV and MULT[3:0]

MODE	DIV	K	M	D
0	x	1 to 15	1	2
0	x	16	1	4
1	1	1 to 15	K	1
1	1	16	1	1
1	4	odd	K	2
1	4	even	K-1	4

Since the APLL uses an analog VCO, the APLL requires a lockup time before it is stable. Normally, during lock up time, the APLL-clock mode cannot be used and it must be in DIV mode. In DIV mode MODE is set to 0.

A programmable timer COUNT is included in the APLL peripheral to use as a time keeper for PLL locking. This timer is a counter USBAPLL[10:3] which decrements from a preset value to zero. At zero, it sets the STAT bit USBAPLL[0] to 1. The time can be preset from 0 up to 255 and its input clock is CLKIN divided by 16. So, the corresponding lockup time can be set from 0x16 to 256x16 CLKIN cycles. The COUNT is located at USBAPLL[10:3] and is programmed using the following equation:

$$PLCOUNT = \left(\frac{LockTime}{16 \times T_{CLKIN}}\right)$$

where *TCLKIN* is the input reference clock period and *LockTime* = 30 μs.

5 USB PLL Selection Register (USBPLLSEL)

The DSP includes a USB PLL selection register (USBPLLSEL) that allows for switching between the APLL and DPLL, and allows for monitoring of the PLL status. A functional diagram of the USBPLLSEL register is shown in Figure 4.

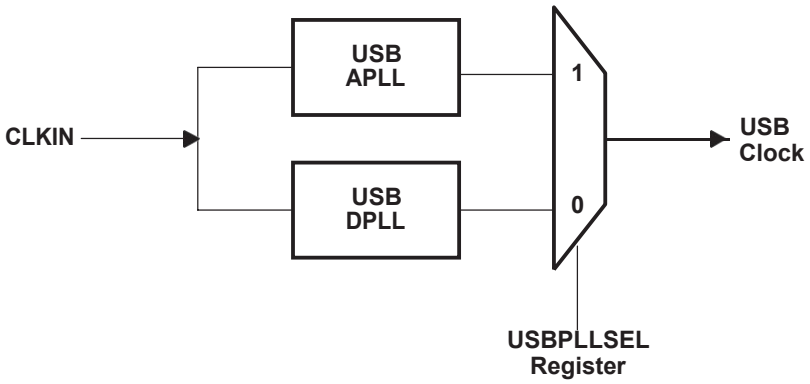


Figure 4. System Clock Selection Diagram

The USBPLLSEL register is located at I/O space address 0x1E80 and has the fields shown in Figure 5 and described in Table 3.

Figure 5. USB PLL Selection Register (USBPLLSEL)

15	3	2	1	0
Reserved		APLLSTAT	DPLLSTAT	PLLSEL
R		R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. USB PLL Selection Register (USBPLLSEL) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved
2	APLLSTAT		APLL status
		0	If set to 0, the APLL is providing the clock to the USB peripheral
		1	If set to 1, the APLL is not providing the clock to the USB peripheral.
1	DPLLSTAT		DPLL status
		0	If set to 0, the DPLL is providing the clock to the USB peripheral.
		1	If set to 1, the DPLL is not providing the clock to the USB peripheral.
0	PLLSEL		PLL selection control
		0	If set to 0, the DPLL is providing the clock to the USB peripheral.
		1	If set to 1, the APLL is providing the clock to the USB peripheral.

6 Switching Between the (USB DPLL/Bypass) and USB APLL

6.1 Switching to the APLL From the DPLL

Switching to the APLL from either the DPLL or the bypass clock is done by first enabling and setting up the APLL, while the system is being driven by the DPLL or bypass clock, then switching to the APLL. The flowchart shown in Figure 6 outlines this process, assuming that the system is operating with either the DPLL or bypass clock.

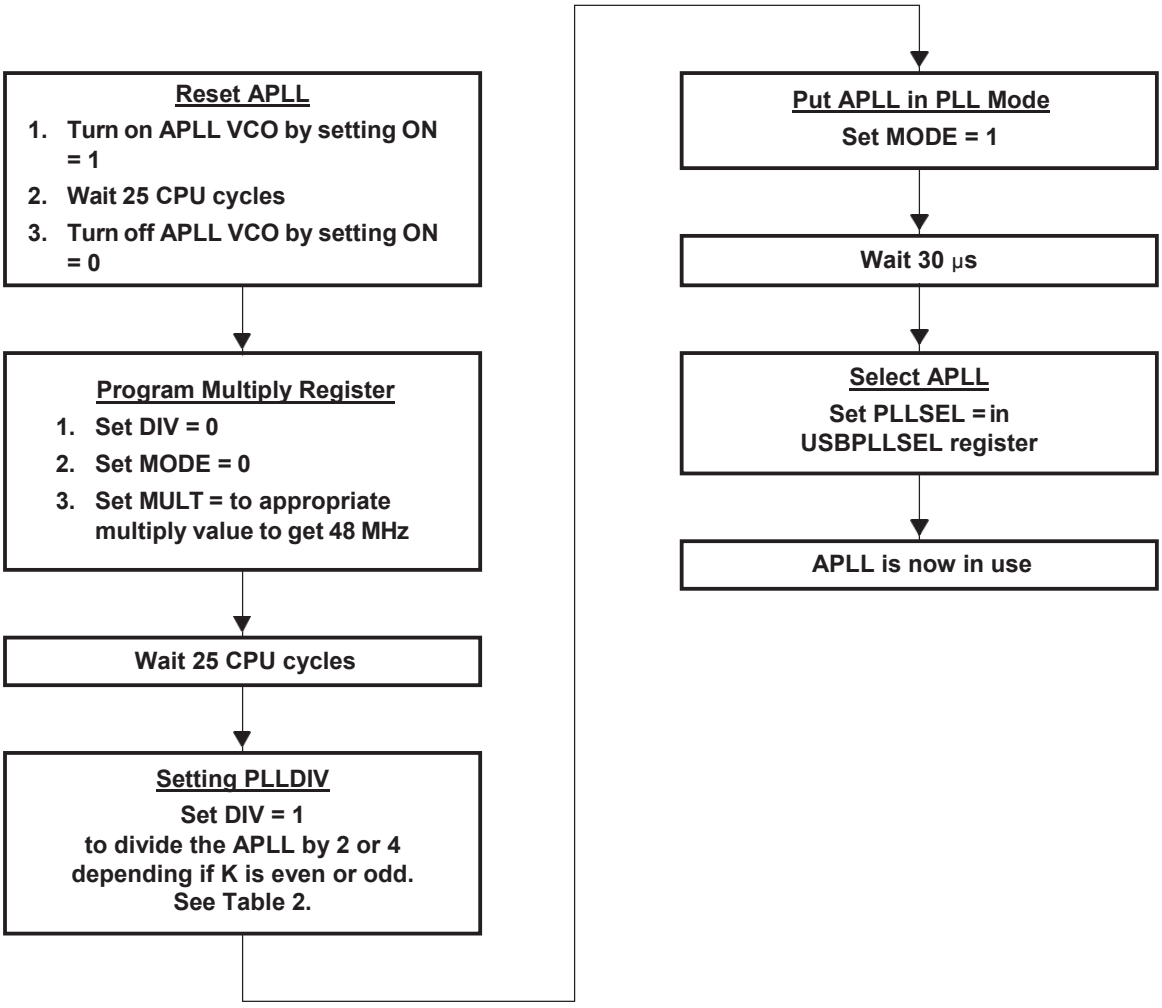


Figure 6. Switching to the APLL From the DPLL

6.2 Switching to the DPLL From the APLL

The procedure shown in Figure 7 outlines switching from APLL mode back to DPLL mode, assuming that the system is operating with APLL.

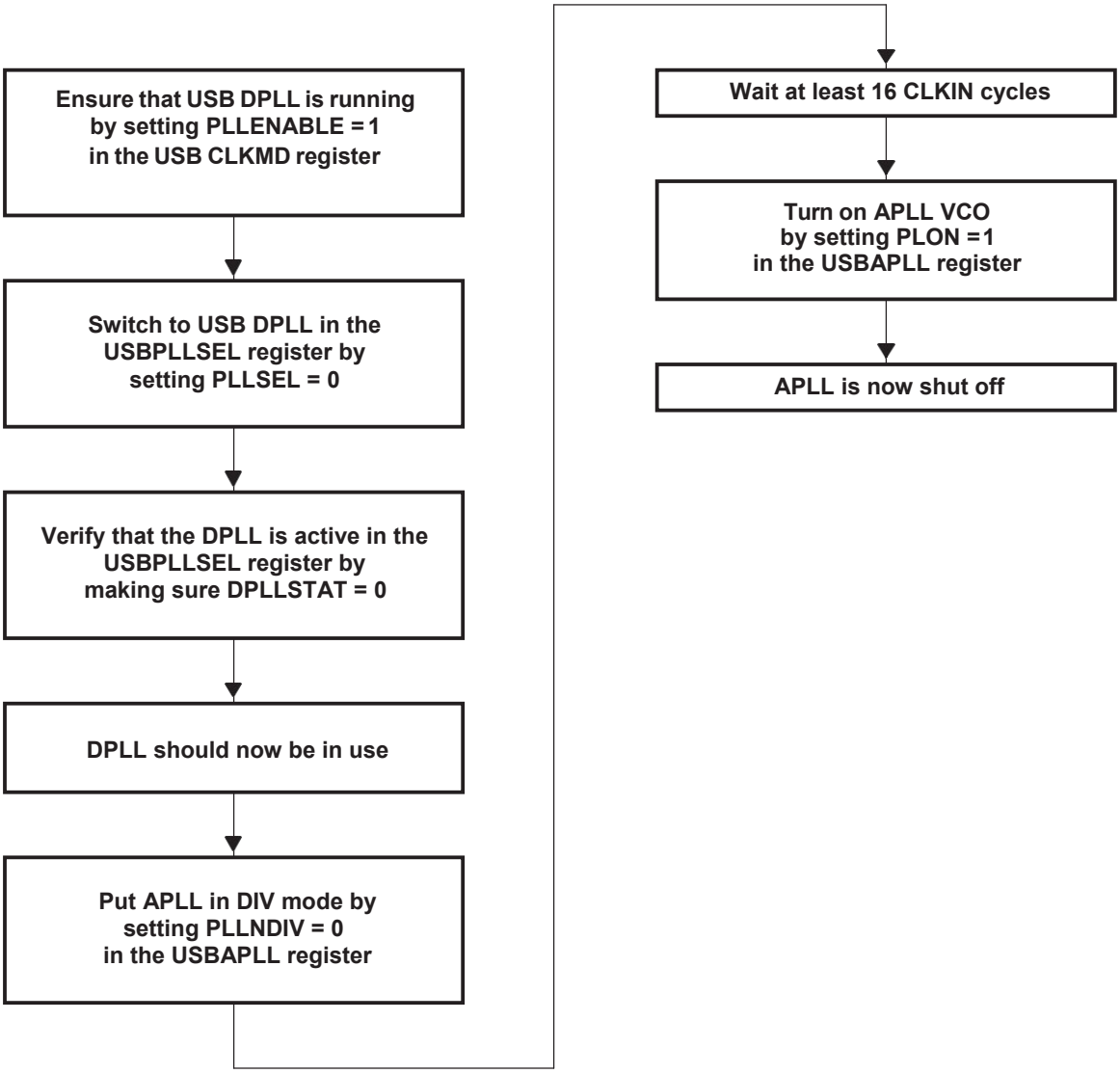


Figure 7. Switching to the DPLL From the APLL

7 IDLING the USB PLL

To IDLE the USB APLL, first switch to the USB DPLL and then shut off the APLL; then IDLE the clock generation domain. The following procedure outlines this process.

Assuming that the APLL is in operation, follow these steps:

1. Switch to the DPLL as described in Section 6.2.
2. Double check that the APLL VCO is off, by checking the ON bit.
3. IDLE the clock generation domain using the ICR and IDLE instruction.

8 Waking Up the USB From IDLE

Since the DPLL is used to get into IDLE, waking up from IDLE uses the DPLL wake-up criteria. For details, see *Disabling the Internal Oscillator on the TMS320VC5503/C5506/C5507/C5509/C5509A DSP* (SPRA078). After waking up from IDLE, follow Section 6.1 to reinitialize the APLL. The following procedure outlines this process:

- Wake-up event awakens the CPU
- CPU is in DPLL or bypass mode
- Switch to the APLL as described in Section 6.1

9 Example USB PLL Programs

Included in this application report are two example assembly programs which demonstrate some of the topics covered in this application note. It is highly recommended that you study and run these examples to get a clearer understanding of the USB APLL.

- DPLL_To_APLL - switches from the power on default of DPLL/Bypass to the APLL.
- APLL_To_DPLL - switches the APLL back to the DPLL and then shuts off the APLL.

10 References

- *Disabling the Internal Oscillator on the TMS320VC5503/C5506/C5507/C5509/C5509A DSP* (SPRA078)

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