Application Report
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C5000 Hardware Applications

TMS320VC5501, TMS320VC5502 Power Consumption Summary

Embedded Processors Catalog Applications

ABSTRACT

This document assists in the estimation of power consumption for the TMS320VC5501 and TMS320VC5502 digital signal processors (DSPs). Because power consumption can vary widely on these devices, a spreadsheet was developed to provide a better estimate. This spreadsheet allows the user to tailor the prediction to their particular application and also allows designers the ability to test the efficiency of different configurations before any hardware is assembled or code is written.

The Power Estimation Spreadsheet can be downloaded from http://www.ti.com/lit/zip/SPRA993.

Contents

1 Activity-Based Models

Power consumption of the TMS320VC5501 and TMS320VC5502 DSPs is extremely application dependent due to their many peripherals and varieties of power saving modes. Due to these features, the application to be measured must be well understood before a power estimate can be given. The activity of each peripheral must be known to configure the power estimation spreadsheet for accurate results, which can be used in power supply design or battery life prediction.

The model used in this spreadsheet is based on two modes of power consumption: static and activity power. With this model, each active component can be isolated and accurately modeled to determine its contribution to the static power.

1.1 Static Power

Static power is the consumption when the APLL is not enabled and nothing on the device is being clocked (including CLKIN). Therefore, power is based on only voltage and temperature. This number can be affected by core voltage (CV_{DD}), I/O voltage (DV_{DD}), APLL voltage (PV_{DD}), and the device operating temperature.

1.2 Activity Power

Activity power is the consumption of the active parts of the DSP. These parts include the CPU, EMIF, APLL, peripherals, and so on. Power consumption is based on voltage, frequency, and the given configuration of each module. To provide more accurate power estimation, each block can be characterized independently and its relative contribution to overall consumption is provided, which aids in system design for greater efficiency.

Each module has parameters used to describe its activity. These parameters include frequency, idle status, utilization, read/write balance, bus size, switching probability, trace length, and load capacitance. Each module may not include all of these parameters however.

- Frequency is the operating frequency of a module, or the operating frequency of the interface to that module.
- Idle status indicates whether the module is idle or active.
- %Utilization is the percentage of activity in a module relative to its maximum.
- %Writes is the percentage of writes relative to the total number of transfers.
- Bits is the number of data bits in use on a interface that supports variable-width busses.
- %Switch is the probability that a data bit switches from one cycle to the next.
- Trace length is the total board trace length being driven by each pin of the interface.
- Load capacitance is the sum of the input capacitances at the end of each trace.

1.3 Modules

Each of the following modules and sub-modules are user-configurable in the power estimation spreadsheet within realistic operating parameters. The C5501 does not include all the peripherals listed here, but the spreadsheet is written in a such manner that non-applicable peripherals can be easily disabled or idled.

- APLL (lock mode only)
- CPU
  - Instruction cache
  - CLKOUT
- EMIF
  - ECLKOUT1
  - ECLKOUT2
- DMA (six channels)
- HPI (multiplexed mode only)
- McBSP0
- McBSP1
- McBSP2
- UART
- I^{2}C
- Timer 0
- Timer 1
- Timer 3 (BIOS timer)
- Watchdog timer
- GPIO/XF

2 Using the Power Estimation Spreadsheet

Using the spreadsheet involves simply entering the usage parameters into the white cells. To ensure that the data validation feature limits the input to realizable configurations, enter values from left to right, top to bottom. Then, the spreadsheet takes the provided information and displays the details of power consumption for that configuration.

To simplify the operation of the spreadsheet, it does not support more than one idle configuration at any given time. For applications where the idle status is constantly changing, each possible configuration must be estimated independently, then the maximum taken for power supply design or all cases time-averaged for battery life prediction.

The Power Estimation Spreadsheet can be downloaded here.

2.1 Choosing Appropriate Values

Choosing the correct values for the power estimation spreadsheet is critical for accuracy in the results. Each module must be considered in isolation and the user must account for all activity a given operation may include. For example, EMIF activity is not included in the CPU activity when the code is being executed from external memory. The EMIF activity must be included separately in the EMIF section of the spreadsheet.

2.1.1 Frequency

In some cases the frequency parameter for a particular module denotes the output frequency of that module. For other modules it denotes the internal operating frequency.

2.1.1.1 APLL

The frequency of the APLL is simply the output frequency of the clock generator in lock mode. The bypass mode of the clock generator is not supported.

The clock frequency of the internal clocks SYSCLK1, SYSCLK2, and SYSCLK3 can be specified as a divided down value of the APLL clock output through the pull down menus included in the power spreadsheet. The internal clock for the CPU and peripherals is automatically set to the frequency of the clock domains to which they belong. For example, the CPU clock is set to the frequency of CLKOUT3, the frequency of the DMA module is set to the frequency of SYSCLK1, the internal frequency of the McBSPs is set to SYSCLK2, and so on. The clock frequency of the APLL and internal clocks must not be set in a manner that violates the frequency restrictions imposed on the device data manual. The device data manual must be referenced for more information on the clock structure and clock domains of the C5501 and C5502.

Note that the APLL consumes power from both the PV_{DD} supply and the DV_{DD} supply. Most systems have one 3.3 V source feeding the PV_{DD} and DV_{DD} supplies, in which case, the PVDD and the DVDD power shown on the spreadsheet must be added together to obtain the total power consumed from the 3.3 V source.

2.1.1.2 CPU

The clock frequency of the CPU, including the instruction cache, is automatically set to the frequency of CLKOUT3. Furthermore, the CLKOUT frequency can be specified to be a divided-down value of the CPU clock through its pull down menu.

2.1.1.3 EMIF

The EMIF module clock frequency is automatically set to the SYSCLK3 clock frequency. Note that the SYSCLK3 clock frequency must not be set in a manner that exceeds the maximum operating frequency of the EMIF as listed on the device data manual. The ECLKOUT1 and ECLKOUT2 clock frequencies can be set to a divided-down value of the EMIF clock frequency through their respective pull down menus. External clocking of the EMIF is not supported.

2.1.1.4 HPI

Since the HPI is an asynchronous interface, the frequency parameter is used to specify the data transfer rate between the host and the DSP. The transfer rate, expressed in Mwords per second, where a word is 16-bits, must be entered in the frequency box for the HPI. The internal operating frequency of the HPI is automatically set to the frequency of SYSCLK1.

2.1.1.5 DMA

The internal operating frequency of the DMA is automatically set to the frequency of SYSCLK1.

2.1.1.6 McBSP

Frequency in this case indicates the output frequency of the McBSPs. The internal operating frequency of the McBSPs is automatically set to the frequency of SYSCLK2.

2.1.1.7 Timer

Frequency in this case indicates the output frequency of the timers. The internal operating frequency of the timers is automatically set to SYSCLK1. Note that Timer 3 does not have an output pin therefore it does not affect the I/O power consumption.

2.1.1.8 UART

The operating baud rate of the UART, expressed in Mbaud, can be specified through the frequency input. The internal operating frequency of the UART is automatically set to the frequency of SYSCLK2.

2.1.1.9 I²C

The operating frequency of the I^2C, expressed in MHz, can be specified through the frequency input. The internal operating frequency of the I^2C is automatically set to the frequency of SYSCLK2.

2.1.1.10 GPIO/XF

The frequency input for GPIO indicates the frequency at which the GPIO pins are switching.

2.1.2 Idle Status

Idle status for a given module is used to specify whether or not that module is configured by software to be in its idle state. The spreadsheet only supports one idle configuration at any time.

The idle status is also used to specify whether or not a peripheral with multiplexed pins was enabled at reset. The spreadsheet should not be programmed in a manner that enables mutually exclusive peripherals at one time. For example, on the C5502 both the UART and McBSP2 cannot both be enabled at the same time. The idle status can also be used to disabled peripherals that are not available on the C5501.

2.1.3 % Utilization

Utilization is explicitly defined for each module to provide a more accurate estimate of power consumption. If a module is not listed, then it is assumed to be in use whenever it is not idle.

2.1.3.1 CPU

Since there are varying degrees of activity for the CPU, it is more difficult to provide a utilization number. Whenever the CPU is active (non-idle) it is repeatedly executing instructions. For this reason, 0% activity is defined as a repeated NOP instruction – the smallest amount of power the CPU can consume while active. Conversely, 100% activity is defined as the most power intensive instruction – the dual multiply and accumulate. All other instructions fall somewhere in between. No single algorithm achieves 100% utilization, but some highly optimized functions can come close. In addition, the CPU must also be used for control oriented tasks that consume far less current.

For example, assume that a certain application executes control code half of the time and a highly optimized algorithm for the other half. If the control code is estimated to be at 30% utilization and the dense DSP code is estimated to be at 90% utilization, the overall utilization would be 60% (30% × 50% + 90% × 50%). If the application spent more time executing the optimized algorithm, utilization would obviously go up, and vice versa. By examining individual portions of an application and estimating the utilization and time spent in each, a more accurate CPU utilization percentage can be obtained.

2.1.3.2 EMIF

EMIF utilization is related to the maximum bandwidth of the EMIF for internal to external DMA transfers using SBSRAM memory. One hundred percent utilization corresponds to the maximum transfer rate for a given frequency when doing these types of transfers. Since the EMIF throughput varies based on the type of memory being used, this number can be scaled up or down depending on which type of memory is being used.

As stated on the *Achieving Efficient Memory System Performance With the I-Cache on the TMS320VC5502* application report (SPRA924), the maximum throughput for internal to external memory DMA transfers using SBSRAM memory is four 32-bit words per 20 EMIF clock cycles (80 Mbytes per sec at 100 MHz). The utilization percentage is defined as the EMIF throughput for the application under question divided by the throughput for these SBSRAM accesses.

Switching in the EMIF data lines is the dominant factor in the EMIF I/O power consumption. The effect of the address and control lines is minimal. Therefore, when selecting a utilization number for a memory type that is not SBSRAM it is valid to focus on the transfer rate of the EMIF without regard for the memory type.

2.1.3.3 HPI

HPI utilization is defined as the percentage of time the HPI is transferring data at the rate specified using the frequency input for this module. The HPI is assumed to not be transferring any data for the remainder of the time.

2.1.3.4 DMA

DMA utilization for a given channel is related to the maximum bandwidth of the port for each data resource, which is four 32-bit transfers per 12 DMA clock cycles (using bursting and with no other DMA traffic). This calculation results in a utilization number that is simply the average bandwidth of the DMA channel divided by the maximum bandwidth.

2.1.3.5 McBSP

McBSP utilization is defined as the percentage of time that the McBSP is transferring data. The McBSP is assumed to not be transferring any data for the remainder of the time.

2.1.3.6 UART

UART utilization is defined as the percentage of time that the UART is transferring data. The UART is assumed to not be transferring any data for the remainder of the time.

The UART core activity number automatically includes the core power consumption required to use two DMA channels (one to send data to the UART and the other to read data from the UART). Therefore the DMA module must be activated and two channels must be reserved with 0% utilization in the spreadsheet to get an accurate estimate of core power when using the UART.

2.1.3.7 I²C

I^2C utilization is defined as the percentage of time that the I^2C is transferring data, where the remainder of the time the I^2C is assumed to not be transferring any data.

The I^2C core activity number automatically includes the core power consumption required to use two DMA channels (one to send data to the I^2C and the other to read data from the I^2C). Therefore the DMA module must be activated and two channels must be reserved with 0% utilization in the spreadsheet to get an accurate estimate of core power when using the I^2C.

2.1.3.8 Timer

Timer utilization is defined as the percentage of time that the timer is counting.

2.1.3.9 GPIO/XF

Utilization for GPIOs is the percentage of time that they are switching at their specified frequency.

2.1.4 % Writes

For modules that move data onto a bus, % writes is defined as the percentage of utilization in which the peripheral is putting data on the bus. Data is assumed to be taken off the bus for the remainder of the utilization period. For modules with equal I/O bandwidth, the write percentage is 50%.

2.1.5 Bits

Bits is the number of data bits on a variable width bus. The spreadsheet only permits valid bus sizes.

2.1.6 % Switch

Random data has a 50% chance any bit changes from one cycle to the next. Some applications may be able to predict this change using some a priori information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. All other applications must use the default number of 50%.

2.1.7 Trace Length

The trace length parameter indicates the average length of controlled-impedance board trace of each output for a given interface (assumed 50 Ω trace). This only affects I/O power and further, only makes significant contribution when the module is writing.

2.1.8 Load Capacitance

Load capacitance is the average of the sum of the input capacitances of all external devices connected to given outputs of a module. This parameter can be obtained from the data sheets of the devices that are connected to the DSP.

2.1.9 Other

Some modules have other parameters that are self explanatory. These parameters include whether the timer pins are configured as outputs, and the number of GPIO pins configured as outputs.

2.1.10 Units

The results are estimated in the spreadsheet and displayed in milliamps (mA) or milliwatts (mW). Click on the units in the Total row of the calculated results and use the pull-down menu to select the desired units.

2.2 Graphs

The graphs included in the spreadsheet show the relative contribution of total core and I/O activity power for each module. They provide a visual display of power usage and allow easy identification of the major power consumers. Note that the power consumed by the APLL on the DV_{DD} and the PV_{DD} supplies is lumped together and shown in the graph for I/O power as APLL.

3 Using the Results

The results presented in the spreadsheet are based on measured data for revision 1.0 silicon. The measured units were selected to be towards the high end of power consumption for production units. Most production units have power consumption that is below the value given in the spreadsheet, if accurately modeled. Transient currents may cause power to spike above the estimated value for short periods, but long term power consumption must be below the spreadsheet value. This allows for better estimates of power supply requirements and more accurate battery life predictions.

4 Example

The following example demonstrates how to choose the values for the power estimation spreadsheet for a sample application running on the C5502. The values shown can be filled into the spreadsheet by clicking on the Sample App Configuration button included in the spreadsheet.

4.1 Sample Application

In this example, the DSP is running a highly optimized algorithm while several DMA channels move data to and from several peripherals. The CPU is executing code completely from within the instruction cache leaving the EMIF free for data transfers. One DMA channel is being used to move data out to external asynchronous memory at the maximum throughput rate. The EMIF is configured for 32-bit asynchronous mode. Two McBSPs are being used to shift 32-bit data in and out of internal memory at 25 MHz with two DMA channels servicing the McBSPs. The UART is being used to transmit and receive data at 9600 baud using two DMA channels. One timer is generating a 5 MHz clock while another generates a 10 MHz clock. The watchdog timer generates a DMA event at 30 MHz. A DMA channel transfers data within internal memory using the watchdog timer event. An external host is reading data from the DSP at a rate of 5 Mwords per second using the HPI. All internal clocks are set to divide-by-two mode except for the EMIF clock which runs in divide-by-four mode.

- Temp: 25°C
- APLL: 300 MHz
- CPU: 85% utilization
  - Instruction cache enabled
  - CLKOUT off
- EMIF: 75 MHz, 118% utilization, 100% writes, 32 bits, 100% switching
  - Utilization
    - Maximum EMIF throughput for asynchronous memory: four 32-bit words per 17 EMIF clock cycles.
    - Maximum EMIF throughput for SBSRAM memory: four 32-bit words per 20 EMIF clock cycles.
    - Asynchronous memory throughput divided by SBSRAM memory throughput yields 118%.
  - ECLKOUT1 and ECLKOUT2: off (not needed for asynchronous memory)
- HPI: 5 Mwords per second, 100% utilization, 100% writes, 100% switching
- DMA
  - Channel 0: 35% utilization, 32-bit elements, 100% switching (for internal memory to external memory transfers)
    - Four 32-bit words every 17 cycles at 75 MHz (EMIF frequency) divided by four 32-bit words every 12 cycles at 150 MHz (DMA frequency) yields about 35% utilization for the DMA channel writing to external memory.
  - Channel 1: 1.56% utilization, 32-bit elements, 100% switching (for internal memory to McBSP0 transfers)
    - One 32-bit word every 32 cycles at 25 MHz (McBSP frequency) divided by four 32-bit words every 12 cycles at 150 MHz (DMA frequency) yields about 1.56% utilization.
  - Channel 2: 1.56% utilization, 32-bit elements, 100% switching (for McBSP1 to internal memory transfers)
    - One 32-bit word every 32 cycles at 25 MHz (McBSP frequency) divided by four 32-bit words every 12 cycles at 150 MHz (DMA frequency) yields about 1.56% utilization.
  - Channel 3 and 4: 0% utilization (reserved for UART transfers)
  - Channel 5: 60% utilization (for internal memory to internal memory transfers using watchdog timer event)
    - One 32-bit word every watchdog timer event (30 MHz) divided by four 32-bit words every 12 cycles at 150 MHz or, alternatively, one 32-bit word at 50 MHz yields about 60% utilization.
- McBSP0: 25 MHz, 100% utilization, 100% switching
- Timer0: 5 MHz, 100% utilization, 100% switching
- Timer1: 10 MHz, 100% utilization, 100% switching
- WD Timer: 30 MHz, 100% utilization, 100% switching
- UART: 9600 baud, 100% utilization
- All other peripherals use 0 MHz and 0% utilization

- Assumed load capacitances and trace lengths are shown in the spreadsheet

Entering these values into the spreadsheet gives us a maximum power consumption of about 239 mA for the core and about 50 mA for I/O (includes both pin I/O and PLL I/O).

Note that in this example percent switching was set to maximum so that the maximum power number could be estimated.

5 References

1. *TMS320VC5510 Power Consumption Summary* (SPRA972)
2. *TMS320VC5502 Fixed-Point Digital Signal Processor* (SPRS166)
3. *TMS320VC5501 Fixed-Point Digital Signal Processor* (SPRS206)
4. *Achieving Efficient Memory System Performance With the I-Cache on the TMS320VC5502* (SPRA924)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2004) to A Revision	Page
• Changed link in *Using the Power Estimation Spreadsheet*	2

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