TMS320DM642 EVM Daughtercard Specification Revision 1.0

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ABSTRACT

The daughtercard specification is based on the interface provided with the TMS320DM642 (DM642) Evaluation Module (EVM). This specification provides the information necessary to allow daughtercards to be designed to function with the DM642 EVM. It also provides guidelines for designing new DSP motherboards aiming to provide a compatible interface. This includes systems based on different DSPs as well as systems from different vendors. Signals are brought to the daughtercard through three 90-pin headers, with two headers primarily for the DM642's three video port peripheral signals and the other primarily for the DM642's external memory interface (EMIF).

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1 Introduction

This application report documents details on how to design a daughtercard to work with the existing TMS320DM642 EVM development board, as well as how to design DSP boards with compatible interfaces.

The DM642 EVM provides daughtercard connectors with signals to the DM642's EMIF, three video ports, I2C interface, timers, multiple interrupts, and general-purpose I/Os allowing developers to design interfaces without designing an actual DSP board. This interface provides a cost-effective way to prototype a system.

1.1 Glossary

The following terms and abbreviations are used throughout the document.

DSP – Digital Signal Processor

EMIF – External Memory Interface

EVM – Evaluation Module

JTAG – Joint Test Action Group (common name for TMS320 emulation port)

McASP – Multichannel Audio Serial Port

McBSP – Multichannel Buffered Serial Port

OSD FPGA – On Screen Display Field Programmable Gate Array

PCB – Printed Circuit Board

VIC – VXCO Interpolated Control Port

XDS – eXtended Development System (e.g., XDS560 for the PC)

2 Daughtercard Interface

The daughtercard interface on the DM642 EVM motherboard consists of three .050" x .050" micro strip 90-pin female connectors (Samtec SFM-145-L2-S-D-LC). Two headers provide an interface to the DM642's three video ports plus other peripherals. The other header provides an interface to the DM642's EMIF.

2.1 DM642 Video Port Interface

The DM642's video ports along with some other peripherals will be routed to 2 daughtercard connectors. These are shown below. Refer to the *TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor* data sheet (SPRS200) for information on the peripherals.

Connector 1 (DC_P1 shown in Figure 1):

- DM642's Video Port 2
- Switch enable/disable control for display functionality on video port 2 (DISPLAY_$\overline{EN}$)
- DM642's I^2C interface
- DM642's Timer 0 and Timer 1
- DM642's NMI and EXT_INT[5:4]/GPIO[5:4]
- DM642's GPIO[3]
- 8 User GPIOs from OSD FPGA on EVM
- Digital Power (+5V, +3.3V, and Ground)

Connector 2 (DC_P2 shown in Figure 1):

- DM642's Video Port 0 (which is muxed with McBSP0 and McASP0 Control)
- DM642's Video Port 1 (which is muxed with McBSP1 and McASP0 Data)
- Switch enable/disable control for capture functionality on video port 0 (CAPTURE1_$\overline{EN}$ and CAPTURE2_$\overline{EN}$)
- Switch enable/disable control for audio functionality on video port 1 (AUDIO_$\overline{EN}$)
- STCLK from VIC on EVM
- System Reset

Table 1 provides the pinout for connector 1 and Table 2 provides the pinout for connector 2.

Table 1. TMS320DM642 EVM Daughtercard Connector (DC_P1) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	GPIO[3]/PCIEEAI	I/O/Z	GPIO/configuration pin	2	EXT_INT4/GPIO[4]	I/O/Z	External interrupt/GPIO
3	GND		System ground	4	EXT_INT5/GPIO[5]	I/O/Z	External interrupt/GPIO
5	NMI	I	DM642 nonmaskable interrupt	6	GND		System ground
7	GND		System ground	8	TINP1	I	Timer 1
9	TINP0	I	Timer 0	10	TOUT1	I/O/Z	Timer 1
11	TOUT0	I/O/Z	Timer 0	12	GND		System ground
13	GND		System ground	14	DISPLAY_$\overline{EN}$	O	Display switch enable/disable control
15	VP2CLK1	I	Video port 2 clock 1	16	GND		System ground

Table 1. TMS320DM642 EVM Daughtercard Connector (DC_P1) Pinout (Continued)

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
17	GND		System ground	18	GND		System ground
19	VP2D18	I/O/Z	Video port 2 data bit 18	20	VP2D19	I/O/Z	Video port 2 data bit 19
21	VP2D16	I/O/Z	Video port 2 data bit 16	22	VP2D17	I/O/Z	Video port 2 data bit 17
23	VP2D14	I/O/Z	Video port 2 data bit 14	24	VP2D15	I/O/Z	Video port 2 data bit 15
25	GND		System ground	26	GND		System ground
27	VP2D12	I/O/Z	Video port 2 data bit 12	28	VP2D13	I/O/Z	Video port 2 data bit 13
29	VP2D10	I/O/Z	Video port 2 data bit 10	30	VP2D11	I/O/Z	Video port 2 data bit 11
31	GND		System ground	32	GND		System ground
33	VP2D8	I/O/Z	Video port 2 data bit 8	34	VP2D9	I/O/Z	Video port 2 data bit 9
35	VP2D6	I/O/Z	Video port 2 data bit 6	36	VP2D7	I/O/Z	Video port 2 data bit 7
37	VP2D4	I/O/Z	Video port 2 data bit 4	38	VP2D5	I/O/Z	Video port 2 data bit 5
39	GND		System ground	40	GND		System ground
41	VP2D2	I/O/Z	Video port 2 data bit 2	42	VP2D3	I/O/Z	Video port 2 data bit 3
43	VP2D0	I/O/Z	Video port 2 data bit 0	44	VP2D1	I/O/Z	Video port 2 data bit 1
45	GND		System ground	46	GND		System ground
47	VP2CLK0	I	Video port 2 clock 0	48	GND		System ground
49	GND		System ground	50	GND		System ground
51	VP2CTL0	I/O/Z	Video port 2 control bit 0	52	VP2CTL1	I/O/Z	Video port 2 control bit 1
53	VP2CTL2	I/O/Z	Video port 2 control bit 2	54	GND		System ground
55	GND		System ground	56	GND		System ground
57	SCL	I/O/Z	I^2C clock	58	USER_GPIO7	I/O	User GPIO 7 from OSD FPGA
59	SDA	I/O/Z	I^2C data	60	USER_GPIO6	I/O	User GPIO 6 from OSD FPGA
61	GND		System ground	62	GND		System ground
63	USER_GPIO4	I/O	User GPIO 4 from OSD FPGA	64	USER_GPIO5	I/O	User GPIO 5 from OSD FPGA
65	USER_GPIO2	I/O	User GPIO 2 from OSD FPGA	66	USER_GPIO3	I/O	User GPIO 3 from OSD FPGA

Table 1. TMS320DM642 EVM Daughtercard Connector (DC_P1) Pinout (Continued)

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
67	USER_GPIO0	I/O	User GPIO 0 from OSD FPGA	68	USER_GPIO1	I/O	User GPIO 1 from OSD FPGA
69	GND		System ground	70	GND		System ground
71	GND		System ground	72	GND		System ground
73	+3.3V		+3.3V voltage supply pin	74	+3.3V		+3.3V voltage supply pin
75	+3.3V		+3.3V voltage supply pin	76	+3.3V		+3.3V voltage supply pin
77	+3.3V		+3.3V voltage supply pin	78	+3.3V		+3.3V voltage supply pin
79	GND		System ground	80	GND		System ground
81	GND		System ground	82	GND		System ground
83	GND		System ground	84	GND		System ground
85	+5V		+5V voltage supply pin	86	+5V		+5V voltage supply pin
87	+5V		+5V voltage supply pin	88	+5V		+5V voltage supply pin
89	+5V		+5V voltage supply pin	90	+5V		+5V voltage supply pin

Table 2. TMS320DM642 EVM Daugthercard Connector (DC_P2) Pinout

Pin	Signal	Type	Description	Pin	Signal	I/O	Description
1	$\overline{\text{RESET}}$	I	System reset	2	CAPTURE1_$\overline{\text{EN}}$	O	Capture 1 switch enable/disable control
3	AUDIO_$\overline{\text{EN}}$	O	Audio switch enable/disable control	4	CAPTURE2_$\overline{\text{EN}}$	O	Capture 2 switch enable/disable control
5	GND		System ground	6	GND		System ground
7	VP0D0	I/O/Z	Video port 0 data bit 0	8	VP0D1	I/O/Z	Video port 0 data bit 1
9	VP0D2	I/O/Z	Video port 0 data bit 2	10	VP0D3	I/O/Z	Video port 0 data bit 3
11	GND		System ground	12	GND		System ground
13	VP0D4	I/O/Z	Video port 0 data bit 4	14	VP0D5	I/O/Z	Video port 0 data bit 5
15	VP0D6	I/O/Z	Video port 0 data bit 6	16	VP0D7	I/O/Z	Video port 0 data bit 7
17	VP0D8	I/O/Z	Video port 0 data bit 8	18	VP0D9	I/O/Z	Video port 0 data bit 9
19	GND		System ground	20	GND		System ground
21	VP0D10	I/O/Z	Video port 0 data bit 10	22	VP0D11	I/O/Z	Video port 0 data bit 11

Table 2. TMS320DM642 EVM Daugthercard Connector (DC_P2) Pinout (Continued)

Pin	Signal	Type	Description	Pin	Signal	I/O	Description
23	VP0D12	I/O/Z	Video port 0 data bit 12	24	VP0D13	I/O/Z	Video port 0 data bit 13
25	GND		System ground	26	GND		System ground
27	VP0D14	I/O/Z	Video port 0 data bit 14	28	VP0D15	I/O/Z	Video port 0 data bit 15
29	VP0D16	I/O/Z	Video port 0 data bit 16	30	VP0D17	I/O/Z	Video port 0 data bit 17
31	VP0D18	I/O/Z	Video port 0 data bit 18	32	VP0D19	I/O/Z	Video port 0 data bit 19
33	GND		System ground	34	GND		System ground
35	VP0CTL2	I/O/Z	Video port 0 control bit 2	36	GND		System ground
37	GND		System ground	38	VP0CTL0	I/O/Z	Video port 0 control bit 0
39	VP0CTL1	I/O/Z	Video port 0 control bit 1	40	GND		System ground
41	GND		System ground	42	GND		System ground
43	GND		System ground	44	VP0CLK1	I	Video port 0 clock 1
45	VP0CLK0	I	Video port 0 clock 0	46	GND		System ground
47	GND		System ground	48	GND		System ground
49	GND		System ground	50	VP1CLK1	I	Video port 1 clock 1
51	VP1CLK0	I	Video port 1 clock 0	52	GND		System ground
53	GND		System ground	54	VP1CTL0	I/O/Z	Video port 1 control bit 0
55	VP1CTL2	I/O/Z	Video port 1 control bit 2	56	GND		System ground
57	GND		System ground	58	VP1CTL1	I/O/Z	Video port 1 control bit 1
59	GND		System ground	60	GND		System ground
61	VP1D18	I/O/Z	Video port 1 data bit 18	62	VP1D19	I/O/Z	Video port 1 data bit 19
63	VP1D16	I/O/Z	Video port 1 data bit 16	64	VP1D17	I/O/Z	Video port 1 data bit 17
65	VP1D14	I/O/Z	Video port 1 data bit 14	66	VP1D15	I/O/Z	Video port 1 data bit 15
67	GND		System ground	68	GND		System ground
69	VP1D12	I/O/Z	Video port 1 data bit 12	70	VP1D13	I/O/Z	Video port 1 data bit 13
71	VP1D10	I/O/Z	Video port 1 data bit 10	72	VP1D11	I/O/Z	Video port 1 data bit 11
73	GND		System ground	74	GND		System ground

Table 2. TMS320DM642 EVM Daugthercard Connector (DC_P2) Pinout (Continued)

Pin	Signal	Type	Description	Pin	Signal	I/O	Description
75	VP1D8	I/O/Z	Video port 1 data bit 8	76	VP1D9	I/O/Z	Video port 1 data bit 9
77	VP1D6	I/O/Z	Video port 1 data bit 6	78	VP1D7	I/O/Z	Video port 1 data bit 7
79	VP1D4	I/O/Z	Video port 1 data bit 4	80	VP1D5	I/O/Z	Video port 1 data bit 5
81	GND		System ground	82	GND		System ground
83	VP1D2	I/O/Z	Video port 1 data bit 2	84	VP1D3	I/O/Z	Video port 1 data bit 3
85	VP1D0	I/O/Z	Video port 1 data bit 0	86	VP1D1	I/O/Z	Video port 1 data bit 1
87	GND		System ground	88	GND		System ground
89	DCARD_STCLK	O	VCXO buffered output clock	90	GND		System ground

2.1.1 Video Port Signals

The DM642 has three 20-bit video ports (Video Port 0, 1, and 2). Two of these video ports (Video Port 0 and 1) are muxed with other peripherals. Table 3 shows the peripherals that are muxed with the video ports. Refer to the *TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor* data sheet (SPRS200) for more information.

Table 3. Video Port Muxing

Video Port	Muxed With
Video Port 0 (lower)	McBSP0
Video Port 0 (upper)	McASP Control
Video Port 1 (lower)	McBSP1
Video Port 1 (upper)	McASP Data
Video Port 2	Not Muxed

The DM642 EVM has 2 Philips SAA7115 Video Decoders connected to the lower halves of Video Port 0 and Video Port 1 and a Philips SAA7105 Video Encoder connected to Video Port 2. The EVM also has a TI TLV320AIC23 stereo audio codec and a SPDIF output tied to the McASP. Refer to the TMS320DM642 Evaluation Module Technical Reference (Spectrum Digital Literature Number: 506845-0001) for further information on the EVM.

Switches are provided on the DM642 EVM to allow the video decoders and encoders and audio interface to be disconnected from the video ports. Therefore, if a daughtercard wants to use the video or audio functionality on the DM642 EVM it can or it can disconnect it from the video port and use the video port as it needs to. The switches are placed as close as possible to the daughtercard connectors to minimize trace lengths and stubs when the switches are disabled. There are two control signals for the video decoders (CAPTURE1_$\overline{EN}$ and CAPTURE2_$\overline{EN}$ on Connector 2), one for the video encoder (DISPLAY_$\overline{EN}$ on Connector 1), and one for the audio interface (AUDIO_$\overline{EN}$ on Connector 2). This will allow a daughtercard to use or disconnect any functionality independently. The control signals are active low so a 10K Ω pull-down resistor will be provided on the baseboard. The daughtercard can use a pull-up resistor to disconnect the switches.

2.1.2 Timers

The DM642's on-chip timers are made available to the daughtercard. Each of the two timers available consists of an input signal and an output signal. The input can be used as either a general-purpose input or as an event to be counted internally. The output signal can be a periodic pulse, or a clock output. The output signal for each timer (TOUT0 and TOUT1) are used for configuration pins on the DM642 and therefore should not be driven or have pullups or pulldowns on the daughtercard.

2.1.3 Interrupts

The daughtercard interface provides three interrupts for the daughtercard to signal events. This includes two maskable interrupts (EXT_INT[5:4]/GPIO[5:4]) plus the non-maskable (system) interrupt (NMI). The maskable interrupts can also be configured as GPIOs.

2.1.4 VCXO Interpolated Control (VIC)

A buffered VIC clock is provided from the DM642 EVM. Refer to the TMS320DM642 Evaluation Module Technical Reference (Spectrum Digital Literature Number: 506845-0001) and *TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor* data sheet (SPRS200) for further information on the VIC.

2.1.5 System Reset

A system reset (active low) is provided from the DM642 EVM.

2.1.6 General-Purpose I/O

The daughtercard interface has one dedicated general-purpose I/O from the DM642 (GPIO[3]). GPIO[3] is used for configuration of the DM642 and therefore should not be driven during device reset or have pullups or pulldowns on the daughtercard. There is also the DM642 peripheral signals described elsewhere in this document that can be used in GPIO mode.

There are 8 general-purpose I/Os from the OSD FPGA (USER_GPIO[7:0]) that is located on the EVM. These GPIOs have pullups on the EVM. Refer to the TMS320DM642 Evaluation Module Technical Reference (Spectrum Digital Literature Number: 506845-0001) or DM642 OSD FPGA User's Guide for further information on the OSD FPGA GPIOs.

2.2 Memory Interface

The third daughtercard connector has the following DM642 EMIF signals routed to it. All these signals are buffered and not tied directly to the DM642.

Connector 3 (DC_P3 shown in Figure 1):

- ED[31:0] (Only supports 32-bits, not full 64-bit bus)
- EA[22:3]
- $\overline{CE2}$ and $\overline{CE3}$
- $\overline{BE0}$, $\overline{BE1}$, $\overline{BE2}$, and $\overline{BE3}$
- ECLKOUT2
- $\overline{ARE}$/$\overline{SDCAS}$/$\overline{SADS}$/$\overline{SRE}$
- $\overline{AOE}$/$\overline{SDRAS}$/$\overline{SOE}$
- $\overline{AWE}$/$\overline{SDWE}$/$\overline{SWE}$
- ARDY

Two of the DM642's memory spaces (CE2 and CE3) are provided for the daughtercard. Memory space CE3 is defined as a 32-bit programmable synchronous memory interface. Refer to TMS320DM642 EVM Technical Reference for the DM642's EMIF configuration register settings.

For this configuration, there are 4MB of addressable memory space available for use. However, the DM642 EVM utilizes 2MB of this space leaving 2MB available for the daughtercard. This 4MB of memory space comprises the daughtercard addresses of DC_A[22:3] = 0x000000 – 0x7FFFF8 (word address range = 0x000000 – 0x3FFFFC). DC_A[22:3] = 0x000000 – 0x3FFFF8 (word address range = 0x000000 – 0x1FFFFC) is used by the EVM and DC_A[22:3] = 0x400000 – 0x7FFFF8 (word address range = 0x200000 – 0x3FFFFC) is available for the daughtercard.

The DM642's memory space CE2 is not used by the EVM and can be configured anyway the daughtercard needs.

Table 4 provides the pinout for connector 3.

Table 4. TMS320DM642 EVM Daughtercard Connector (DC_P3) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	GND		System ground	2	GND		System ground
3	ED31	I/O/Z	EMIF data pin 31	4	ED30	I/O/Z	EMIF data pin 30
5	ED29	I/O/Z	EMIF data pin 29	6	ED28	I/O/Z	EMIF data pin 28
7	ED27	I/O/Z	EMIF data pin 27	8	ED26	I/O/Z	EMIF data pin 26
9	ED25	I/O/Z	EMIF data pin 25	10	ED24	I/O/Z	EMIF data pin 24
11	GND		System ground	12	GND		System ground
13	ED23	I/O/Z	EMIF data pin 23	14	ED22	I/O/Z	EMIF data pin 22
15	ED21	I/O/Z	EMIF data pin 21	16	ED20	I/O/Z	EMIF data pin 20
17	ED19	I/O/Z	EMIF data pin 19	18	ED18	I/O/Z	EMIF data pin 18

Table 4. TMS320DM642 EVM Daughtercard Connector (DC_P3) Pinout (Continued)

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
19	ED17	I/O/Z	EMIF data pin 17	20	ED16	I/O/Z	EMIF data pin 16
21	GND		System ground	22	GND		System ground
23	ED15	I/O/Z	EMIF data pin 15	24	ED14	I/O/Z	EMIF data pin 14
25	ED13	I/O/Z	EMIF data pin 13	26	ED12	I/O/Z	EMIF data pin 12
27	ED11	I/O/Z	EMIF data pin 11	28	ED10	I/O/Z	EMIF data pin 10
29	ED9	I/O/Z	EMIF data pin 9	30	ED8	I/O/Z	EMIF data pin 8
31	GND		System ground	32	GND		System ground
33	ED7	I/O/Z	EMIF data pin 7	34	ED6	I/O/Z	EMIF data pin 6
35	ED5	I/O/Z	EMIF data pin 5	36	ED4	I/O/Z	EMIF data pin 4
37	ED3	I/O/Z	EMIF data pin 3	38	ED2	I/O/Z	EMIF data pin 2
39	ED1	I/O/Z	EMIF data pin 1	40	ED0	I/O/Z	EMIF data pin 0
41	GND		System ground	42	GND		System ground
43	N/C		No connect	44	ECLKOUT2	O/Z	EMIF output clock 2
45	GND		System ground	46	GND		System ground
47	$\overline{\text{BE3}}$	O/Z	EMIF byte enable 3	48	$\overline{\text{BE2}}$	O/Z	EMIF byte enable 2
49	$\overline{\text{BE1}}$	O/Z	EMIF byte enable 1	50	$\overline{\text{BE0}}$	O/Z	EMIF byte enable 0
51	GND		System ground	52	GND		System ground
53	$\overline{\text{CE3}}$	O/Z	EMIF chip enable 3	54	$\overline{\text{CE2}}$	O/Z	EMIF chip enable 2
55	GND		System ground	56	GND		System ground
57	$\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/ $\overline{\text{SADS}}$/$\overline{\text{SRE}}$	O/Z	EMIF async read enable	58	$\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$ /$\overline{\text{SOE}}$	O/Z	EMIF async output enable
59	$\overline{\text{AWE}}$/$\overline{\text{SDWE}}$ /$\overline{\text{SWE}}$	O/Z	EMIF async write enable	60	ARDY	I	EMIF async ready
61	GND		System ground	62	GND		System ground
63	EA22	O/Z	EMIF address pin 22	64	EA21	O/Z	EMIF address pin 21
65	EA20	O/Z	EMIF address pin 20	66	EA19	O/Z	EMIF address pin 19
67	EA18	O/Z	EMIF address pin 18	68	EA17	O/Z	EMIF address pin 17

Table 4. TMS320DM642 EVM Daughtercard Connector (DC_P3) Pinout (Continued)

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
69	EA16	O/Z	EMIF address pin 16	70	EA15	O/Z	EMIF address pin 15
71	GND		System ground	72	GND		System ground
73	EA14	O/Z	EMIF address pin 14	74	EA13	O/Z	EMIF address pin 13
75	EA12	O/Z	EMIF address pin 12	76	EA11	O/Z	EMIF address pin 11
77	EA10	O/Z	EMIF address pin 10	78	EA9	O/Z	EMIF address pin 9
79	GND		System ground	80	GND		System ground
81	EA8	O/Z	EMIF address pin 8	82	EA7	O/Z	EMIF address pin 7
83	EA6	O/Z	EMIF address pin 6	84	EA5	O/Z	EMIF address pin 5
85	EA4	O/Z	EMIF address pin 4	86	EA3	O/Z	EMIF address pin 3
87	GND		System ground	88	GND		System ground
89	N/C		No connect	90	N/C		No connect

2.3 Physical EVM Layout

The layout of the DM642 EVM motherboard is shown in Figure 1. See Figure 4 for a photograph of the motherboard. Note that the layout shows the top of the DSP board and *not* the daughtercard. The diagram shows the physical dimensions of the area that is available for a daughtercard and the placement of the daughtercard connectors. The daughtercard interface on the DM642 EVM consists of three 90-pin connectors from Samtec. The part number for the connectors is SFM-145-L2-S-D-LC. Details on the required mating connectors on the daughtercard are provided in the daughtercard section.

The diagram shows four keepout zones on the motherboard. Keepout zones 1, 2, and 3 have various connectors that are too high to clear a daughtercard (maximum mated height of 11.81mm, see section 2.4). Therefore, the daughtercard cannot extend over these areas.

Keepout zone 4 is the JTAG connector. The daughtercard cannot extend over this area it the user wants to use the 14-pin JTAG connector for emulation. The width of this zone is not shown since it really depends on the emulator header. The XDS510 and XDS560 have different JTAG headers. See Section 2.5 for another option.

All measurements show [mm] on top and [inches] on bottom. The 8 mounting holes have a diameter of 0.125 inches. The pad diameter around the mounting hole is 0.25 inches and is used for a keepout area if spacers are used to attach the daughtercard to the motherboard. The 4 mounting holes on top, the 2 mounting holes on the bottom, and the 2 mounting holes under DC_P1 and DC_P2 are aligned in the horizontal direction. DC_P1 and DC_P2 are aligned in the horizontal direction also.

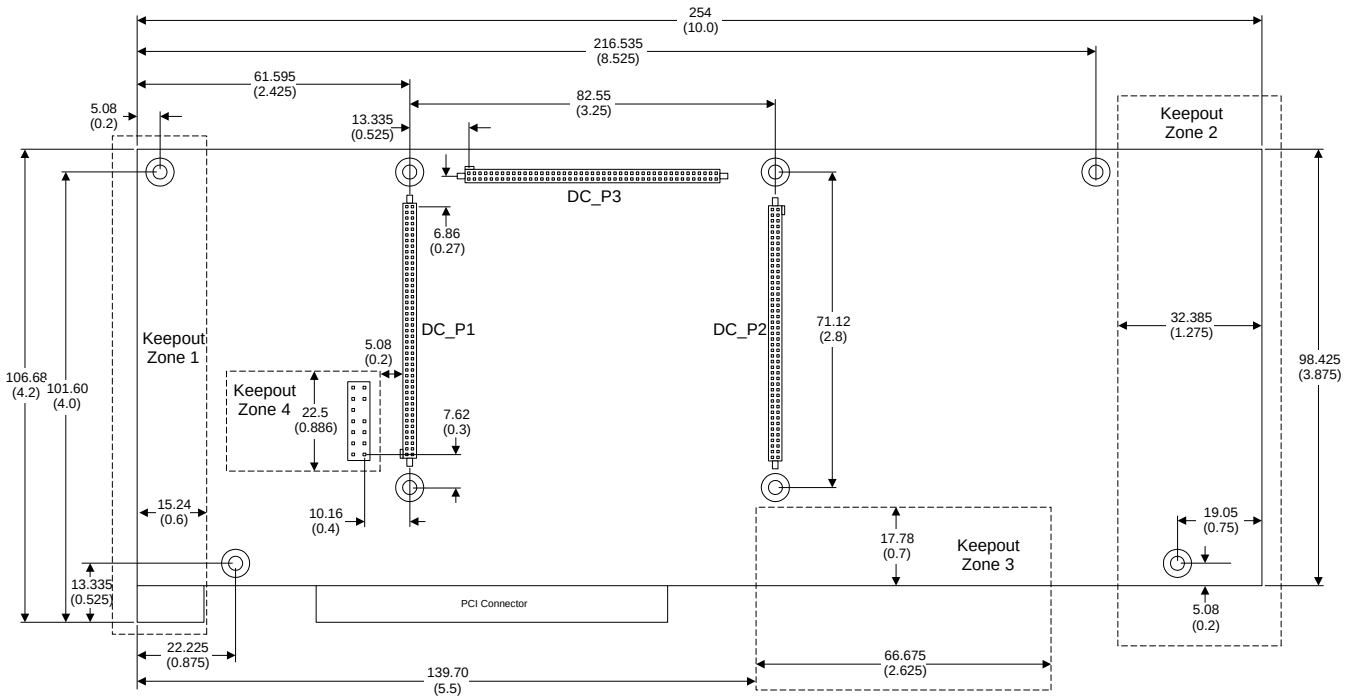

Figure 1. Daughtercard Interface Layout on DSP Motherboard

2.4 Daughtercard Connectors and Component Height

The interface on the daughtercard consists of three of any 90-pin TFM series connectors from Samtec. It is highly recommended that the tallest connectors be used, as they allow the most height for components on the daughtercard. The recommended part numbers are shown in Table 5.

Table 5. Daughtercard Interface Connector Part Numbers

Location	Part Number	Mating Height
DSP Motherboard	SFM-145-L2-S-D-LC	–
Daughtercard	TFM-145-32-S-D-LC (surface mount)	11.81mm (0.465in)

Figure 2 depicts a mounted daughtercard designed to attach to the DM642 EVM. It is assumed that a minimum of 1.27mm (0.050in) clearance is maintained between components. The component heights for the pair are provided in Table 6.

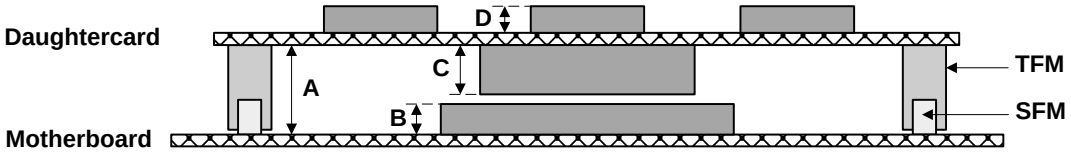

Figure 2. EVM Motherboard and Daughtercard Illustration

Table 6. PCI Motherboard and Daughtercard Component Height

Label	Description	Dimension
A	Mated Height	11.81 mm (0.465 in)
B	Maximum motherboard Component Height	4.0 mm (0.1575 in)
C	Maximum Daughtercard Component Height	6.54 mm (0.2575 in)
D	Maximum “bottom-side” daughtercard component height	None

The DM642 EVM’s tallest component is 26.0mm (1.02in) which doesn’t meet the PCI’s maximum component height of 14.48mm (0.57in) to fit within a single PCI slot. So it will require the slot next to it to be empty. Therefore, the ‘D’ dimension is not as critical.

2.5 JTAG Option

Figure 1 shows the keepout zone (zone 4) for the JTAG connector. Another option is shown in Figure 3. The daughtercard could extend over the JTAG connector on the DM642 EVM motherboard if a connector is used to pass the 14-pin JTAG header through the daughtercard. All measurements are in [mm] in Figure 3.

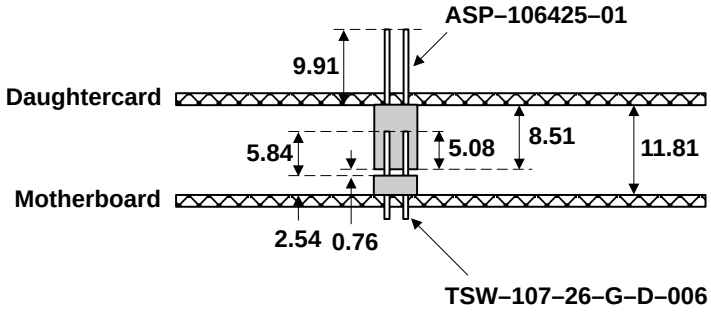

Figure 3. EVM Motherboard and Daughtercard JTAG Illustration

The connectors shown in Figure 3 are Samtec connectors. The connector shown on the daughtercard is a Samtec SSQ-107-03-G-D with pin 6 removed because the JTAG connector is keyed. ASP-106425-01 is a part number created by Samtec’s Application Specific Product group for this type of connector since it is not an option on their standard part numbers.

2.6 Signal Characteristics

The signal characteristics of the DM642 EVM comply with the guidelines outlined in the following section. These guidelines should be used when designing a daughtercard. The most important considerations for the daughtercard design are the following:

2.6.1 Signal Drive

Buffer the daughtercard input signals for loads exceeding 10pF. The motherboard may not supply more drive capability than this.

2.6.2 Input and Output Voltage Tolerance

Input signals from the daughtercard to the DM642 EVM must be 3.3V since the DM642 EVM daughtercard signals are not 5V-tolerant. All output signals from the DM642 EVM to the daughtercard are 3.3V signals.

2.6.3 Timing Delay

The signals for the DM642's EMIF are all buffered with a TI SN74LVTH16245A. All other DM642 signals to the daughtercard interface come directly from the DM642 and are not buffered. Refer to the TMS320DM642 Evaluation Module Technical Reference (Spectrum Digital Literature Number: 506845-0001) for the EVM system architecture.

2.6.4 Power

Obey power supply limits. If a daughtercard requires a voltage that is not present at the interface, or if the card requires an excess amount of power, then power should be supplied separately from the motherboard. This may be done either as part of the daughtercard, or on a supplemental card. The power available to the daughtercard is shown in .

NOTE: Note that if a supplemental power source is provided in this manner, the supplemental power planes should NOT be connected to the power planes of the motherboard.

2.7 Power Supply

The daughtercard interface provides two voltages: 3.3V and 5V. These supplies are intended to provide basic power to the components on the daughtercard. The minimum current that the motherboard is able to supply is provided in Table 7.

Table 7. Minimum Power Supply Requirements

Power Supply	Minimum Current Supplied
3.3V	1A
5V	1A

2.8 EVM Motherboard

Figure 4 shows the DM642 EVM motherboard. This is for reference only.

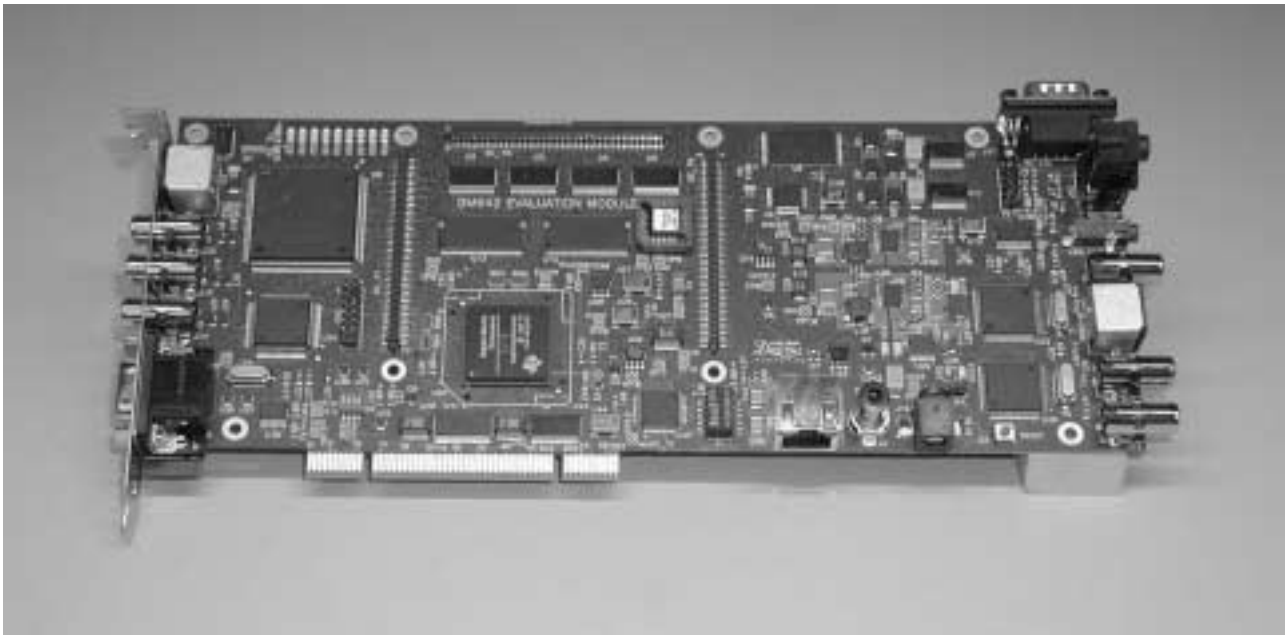

Figure 4. EVM Motherboard

3 References

1. TMS320DM642 Evaluation Module Technical Reference (Spectrum Digital Literature Number: 506845-0001)
2. *TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor* (SPRS200)
3. *TMS320C6000 Peripherals Reference Guide* (SPRU190)
4. *DM642 EVM OSD FPGA Users Guide* (SPRU295)

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