TMS320C6000: Board Design for JTAG

David Bell
Scott Chen

Digital Signal Processing Solutions

ABSTRACT

Designing a TMS320C6000™ DSP board to utilize all of the functionality of the JTAG scan path is a simple process, but a few considerations must be taken into account. The default state of the emulation signals determines whether the JTAG port is used for emulation or for boundary scan. It is therefore necessary to provide flexibility in the design to accommodate those modes that are desired. Through proper design, the JTAG interface can be used to facilitate emulation and/or boundary scan.

Contents

List of Figures

List of Tables

1 Introduction

The IEEE 1149.1 specification covers the requirements for the test access port (TAP) bus slave devices. A superset of this specification is applied to bus master (emulator) devices. The TMS320C6000 generation of DSPs uses the JTAG scan path for boundary scan and/or emulation. There are several layout considerations that must be taken into account when designing a board for emulation and/or boundary scan.

2 JTAG Signal Descriptions for C6000 Devices

The JTAG port of the C6000™ devices† consists of 7 to 17 signals, as listed in Table 1 and Table 2.

Table 1. JTAG Signal Descriptions for TMS320C620x/C670x

Signal	Description	I/O/Z	IPU/IPD
TMS	Test mode select	I	IPU
TDI	Test data input	I	IPU
TDO	Test data output	O/Z	
TCK	Test clock	I	
$\overline{\text{TRST}}$	Test reset	I	IPD
EMU0	Emulation pin 0	I/O/Z	
EMU1	Emulation pin 1	I/O/Z	

Table 2. JTAG Signal Descriptions for TMS320C621x/C671x and TMS320C64x

Signal	Description	I/O/Z	IPU/IPD
TMS	Test mode select	I	IPU
TDI	Test data input	I	IPU
TDO	Test data output	O/Z	IPU
TCK	Test clock	I	IPU
$\overline{\text{TRST}}$	Test reset	I	IPD
EMU0	Emulation pin 0	I/O/Z	IPU
EMU1	Emulation pin 1	I/O/Z	IPU
EMU2	Emulation pin 2. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMU3	Emulation pin 3. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMU4	Emulation pin 4. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMU5	Emulation pin 5. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMU6	Emulation pin 6. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMU7	Emulation pin 7. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMU8	Emulation pin 8. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMU9	Emulation pin 9. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMUCLK0	Emulation clock 0. Reserved for future use. Leave unconnected.	I/O/Z	IPU
EMUCLK1	Emulation clock 1. Reserved for future use. Leave unconnected.	I/O/Z	IPU

† For a complete list of Texas Instruments DSP devices, go to the TI web site at http://www.ti.com

C6000 is a trademark of Texas Instruments.

3 Emulation and Boundary Scan

The emulation signals, EMU*n,* exist for emulation capability of the DSP. Two of these emulation signals, EMU0 and EMU1, also select between emulation operation (normal DSP operation) and boundary scan operation. The selection is made through pullup and pulldown resistors. It is therefore critical that the DSP board layout corresponds to the desired JTAG function(s). Figure 1 and Table 3 show how this is done.

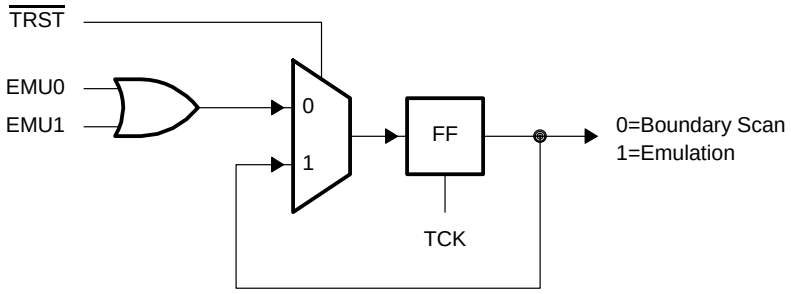


Figure 1. Internal Circuitry for JTAG Operation Mode Select

Table 3. Operation Mode Selection Configuration Table

EMU0	EMU1	Operation Mode
0	0	Boundary Scan Mode
0	1	Reserved
1	0	Reserved
1	1	Emulation Mode (Normal DSP operation)

$\overline{\text{TRST}}$ holds the boundary scan logic in reset (normal DSP operation) when pulled low (its default state, since $\overline{\text{TRST}}$ on all C6000 devices has an internal pulldown resistor). On C620x/C670x, EMU0 and EMU1 do not feature internal pullup resistors; therefore, external resistors must be provided. On C621x/C671x and TMS320C64x™, the internal pullup ensures that at power up, the C6000 DSP functions in its normal (non-test) operation mode if $\overline{\text{TRST}}$ is not connected. Otherwise, $\overline{\text{TRST}}$ should be driven by the boundary scan controller. Boundary scan test cannot be performed while the $\overline{\text{TRST}}$ pin is pulled low. Once TCK is clocking, the JTAG port of C6000 DSP latches EMU0 and EMU1 on the rising edge of $\overline{\text{TRST}}$, to select between emulation operation and boundary scan modes.

On C621x/C671x and C64x™, the EMU0 and EMU1 pins are internally pulled up with a dedicated 30 kΩ resistor; therefore, for emulation and normal operation, no external pullup/pulldown resistors are necessary. For boundary scan operation, pull down the EMU0 and EMU1 with a dedicated 1 kΩ resistor on C621x/C671x and C64x. On the C620x/C670x, pull up EMU0 and EMU1 with a dedicated 20 kΩ resistor for emulation and normal operation, and pull down EMU0 and EMU1 with a dedicated 20 kΩ for boundary scan.

There are two test access ports (TAPs), one for boundary scan and one for emulation. When EMU0 and EMU1 are pulled high, both TAPs are included in the scan path, and only emulation is possible. When EMU0 and EMU1 are pulled low, then only the boundary scan TAP is in the path, and only boundary scan is possible.

TMS320C64x and C64x are trademarks of Texas Instruments.

The instruction length (number of bits in the TAP Instruction Register) of the boundary scan TAP register is different from that of the emulation TAP register. This is important when using the BYPASS instruction. If a C6000 device is in boundary scan mode, the bypass value (BYPASS*xx*, where *xx* is the two-digit bypass value) equals to the instruction length of the boundary scan TAP register. However, if a C6000 device is in emulation mode, the bypass value is the sum of instruction lengths of boundary scan and emulation TAP registers. Instruction lengths for boundary scan TAP register can be found in the BSDL files. Look in the line that contains “Instruction_Length” in BSDL files.

When designing a multiprocessor board, BYPASS instruction can be used to bypass CPUs so that only one CPU is visible. Another useful method is to space and layout each device on the board so a simple wire loop back can be done.

The layout rules for a board that supports emulation are provided in detail in the *TMS320C6000 Peripherals Reference Guide* (SPRU190). Often it is desirable to enable the use of both emulation and boundary scan on the DSP board. This is true if boundary scan test software is used to verify the connectivity and functionality of JTAG devices on the board, or if in-system programmable (ISP) devices are used, as shown in Figure 2.

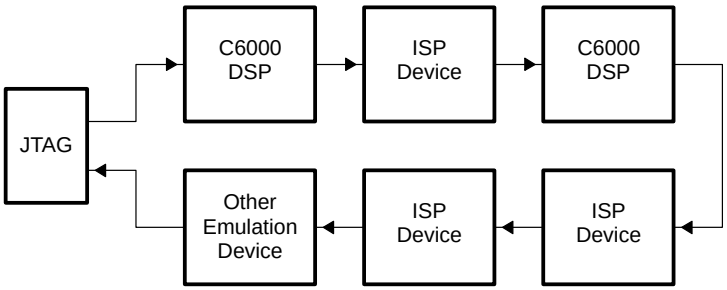
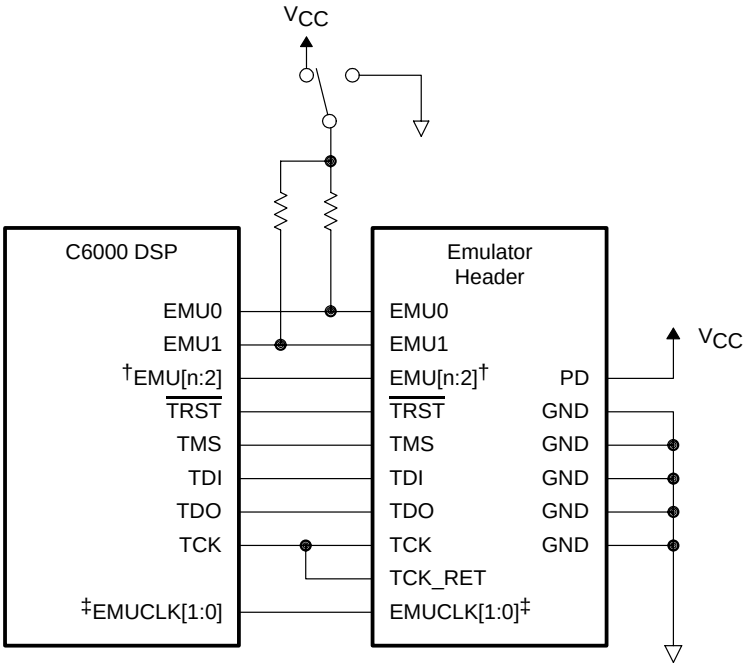


Figure 2. JTAG Chain for Both Emulation and Boundary Scan

For this situation, it is necessary to provide a selection between the pullup and pulldown resistors on EMU0 and EMU1. On the C621x/C671x and C64x, since both EMU0 and EMU1 have internal pullup resistors, a simple solution is to provide external pulldown resistors on the board with a switch to select if pulling low is desired. This is shown in Figure 3.



† 'n' in EMU[n:0] depends on device. For example, C64x has EMU[9:0].
‡ EMUCLK[1:0] is only found on C64x.

Figure 3. JTAG Layout for Both Emulation and Boundary Scan for C621x/C671x and C64x

On C620x/C670x, this can be accomplished either via a switch, or by having both pullup and pulldown resistor pads on the board with one set populated. This is shown in Figure 4.

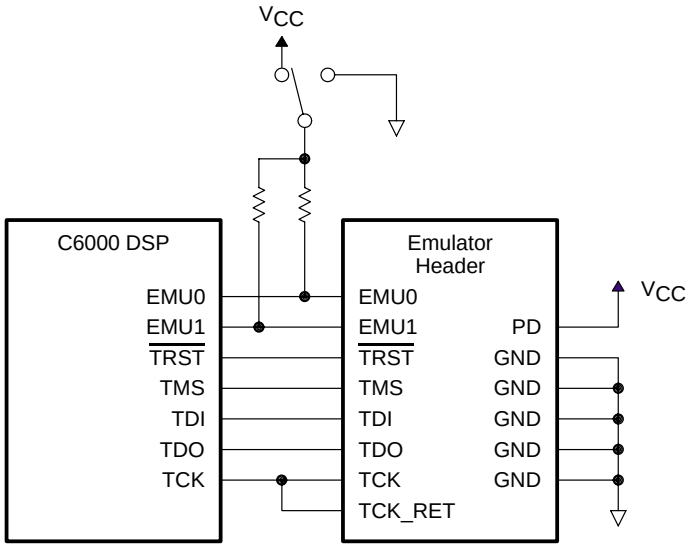


Figure 4. JTAG Layout for Both Emulation and Boundary Scan for C620x/C670x

If the purpose of both boundary scan and emulation to be incorporated into a system is to program logic devices in circuit, then it is advantageous to separate the in–system programmable (ISP) device JTAG chain from the emulation chain, as shown in Figure 5.

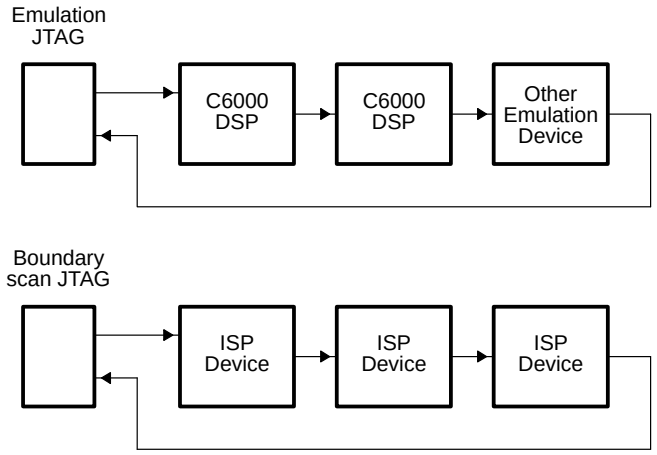
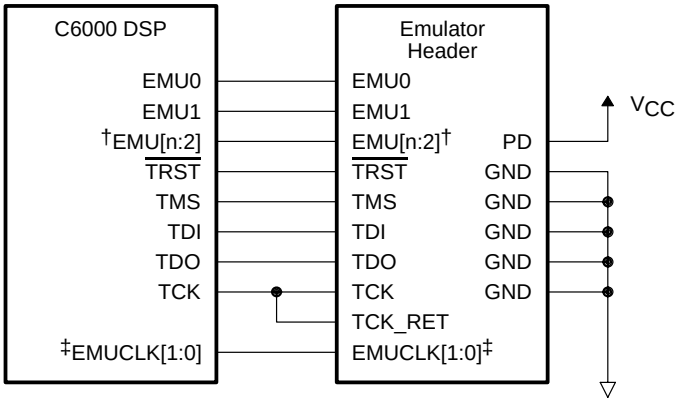


Figure 5. Separate JTAG Chains for Emulation and Boundary Scan

This prevents a selection between boundary scan and emulation from being required. The basic circuit used for emulation only is shown in Figure 6 and Figure 7, with some signals requiring buffering and pullup resistors for trace lengths greater than six inches. On C621x/C671x and C64x, the emulation signals EMU0 and EMU1 are pulled high to enable emulation, so no external resistors are required.



† 'n' in EMU(n:0) depends on device. For example, C64x has EMU[9:0].
‡ EMUCLK[1:0] is only found on C64x.

Figure 6. JTAG Layout for Emulation for C621x/C671x and C64x

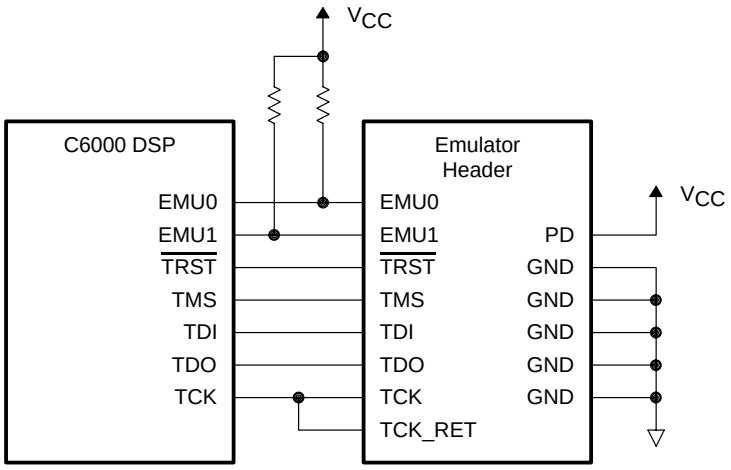
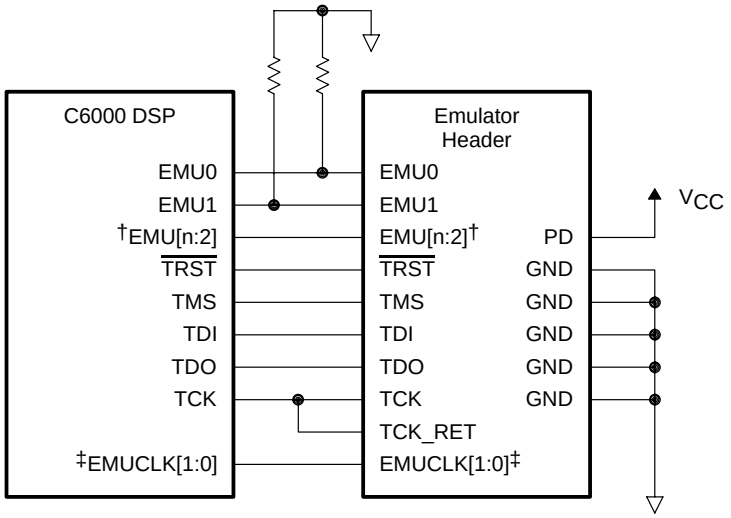


Figure 7. JTAG Layout for Emulation for C620x/C670x

On C620x/C670x, the emulation signals EMU0 and EMU1 are pulled high with external resistors to enable emulation.

If no emulation is required for the C6000 devices in a system, then it is possible to design the board for boundary scan only. As stated previously, to facilitate boundary scan; EMU0 and EMU1 must be pulled down with dedicated external resistors. This is shown in Figure 8.



† 'n' in EMU(n:0) depends on device. For example, C64x has EMU[9:0].
‡ EMUCLK[1:0] is only found on C64x.

Figure 8. JTAG Layout for Boundary Scan

The emulation-only circuit is the most commonly used layout for C6000 DSP boards due to the limited use of boundary scan test software and ISP components, as compared to the number of boards with strictly emulation capability. Those who wish to take advantage of the advantage boundary scan test software and ISP devices provided need to use the appropriate layout shown above for their system.

4 Reference

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265