TMS320C6000 Host Port to MC68360 Interface

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ABSTRACT

This application report describes an interface between the Motorola MC68360 quad integrated communication controller (QUICC) and the host port interface (HPI) of a TMS320C6000™ (C6000™) digital signal processor (DSP) device. This includes a schematic showing connections between the two devices and verification that timing requirements are met for each device (tables and timing diagrams).

NOTE: This application report has not been verified in a board design.

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1 MC68360 Processor Interface

The MC68360 QUICC is 32-bit controller that is an extension of other members of the Motorola M68300 family. The MC68360 QUICC is a one-chip integrated microprocessor and peripheral combination that can be used in controller applications (particularly in communications activities). Figure 1 and Figure 2 show diagrams of the host (MC68360) interface to TMS320C62x™/C67x™/C64x™ HPIs.

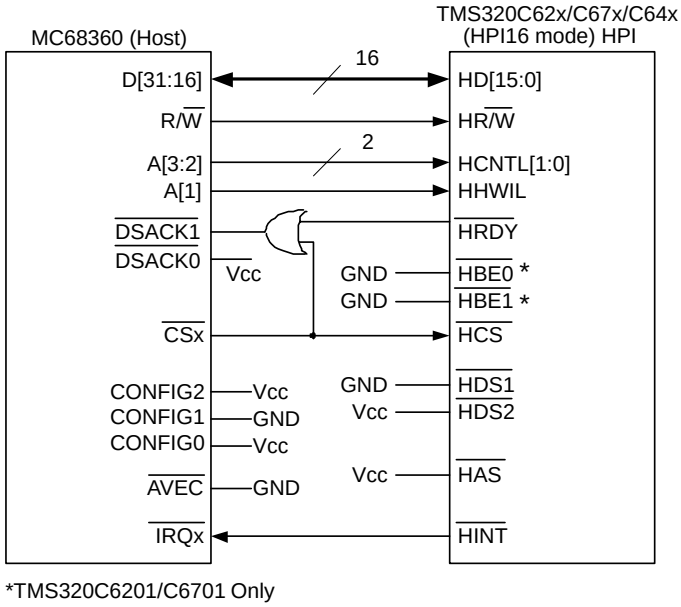

Figure 1. MC68360 to TMS320C62x/C67x/C64x (HPI16) HPI Interface Block Diagram

TMS320C62x, TMS320C67x, TMS320C64x, C62x, C67x and C64x are trademarks of Texas Instruments.

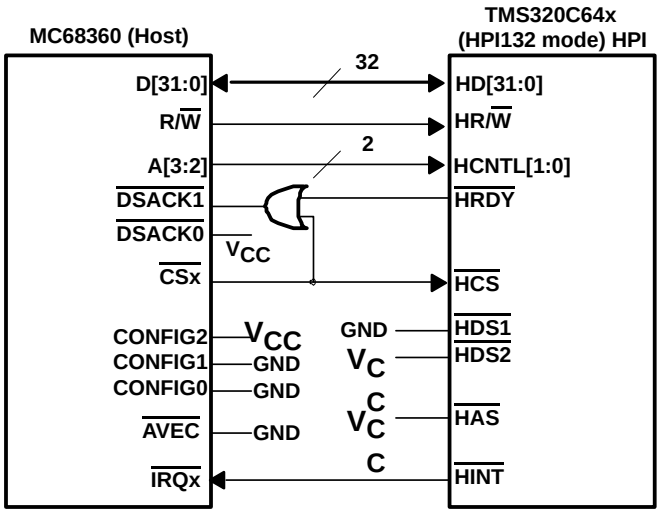

Figure 2. MC68360 to TMS320C64x (HPI32) HPI Interface Block Diagram

Table 1. MC68360 to HPI Pin Connections

HPI Pin	MC68360 Pin	Comments
HCNTL[1:0]	A[3:2]	Address bits of MC68360 are used as control signals.
HHWIL	A[1]	A[1] identifies the first or second halfword of transfer. Unused for HPI32 mode transfers.
HR/$\overline{W}$	R/$\overline{W}$	Indicates a read or write access
HD[15:0] HD[31:0]	D[31:16] D[31:0]	MC68360 uses D[31:16] for 16-bit port interface and D[31:0] for 32-bit port interface.
$\overline{HDS1}$	GND	$\overline{HDS1}$ and $\overline{HDS2}$ are internally exclusively-NORed. $\overline{HDS1}$ and $\overline{HDS2}$ are tied logic low and high, respectively, to enable data strobe at all time.
$\overline{HDS2}$	V_{CC}	See above.
$\overline{HAS}$	V_{CC}	Because host device MC68360 has separate address and data bus, $\overline{HAS}$ does not need to be used. $\overline{HAS}$ is tied inactive high.
$\overline{HCS}$	$\overline{CSx}$	Any one of the chip-selects of MC68360 can be connected to $\overline{HCS}$ as the chip-select signal. This also serves as the data-strobe signal in this case (because $\overline{DS}$ of MC68360 is not used as data strobe).
$\overline{HBE0}$	GND	MC68360 does not have byte write enable signals that have the same timing as other control signals. Therefore, $\overline{HBE1}$ and $\overline{HBE0}$ of HPI are tied low to enable host access to both lower and upper bytes of the half-word during a write. TMS320C6211 does not have $\overline{HBE[1:0]}$ signals.
$\overline{HBE1}$	GND	See above.
-	CONFIG[2:0]	Because CONFIG[2:1] is set to 10, the CPU is enabled and the MBAR register is at 0x003FF00. 16-bit interface CONFIG[2:0]='101' 32-bit interface CONFIG[2:0]='100'

Table 1. MC68360 to HPI Pin Connections (Continued)

HPI Pin	MC68360 Pin	Comments
-	AVEC='0'	The Auto Vector input function is selected in normal operation.
$\overline{\text{HRDY}}$	$\overline{\text{DSACK1}}$	The SPS bits in the MC68360 option registers need to be set to indicate that $\overline{\text{DSACK1}}$ is generated externally by HPI. (See the *MC68360 User's Manual* for details)
$\overline{\text{HINT}}$	$\overline{\text{IRQx}}$	User can select interrupt level ($\overline{\text{IRQ1}}$ to $\overline{\text{IRQ7}}$). Priority level 7 interrupt is a special case. Level 7 interrupts are non-maskable interrupts (NMI). $\overline{\text{IRQ7}}$ is a level-sensitive input and must remain low until the second instruction processing module (CPU32+) returns an interrupt acknowledge cycle for interrupt 7. (See the *MC68360 Quad Integrated Communications Controller User's Manual* for a detailed description.)

$\overline{\text{DS}}$ (data strobe) of the MC68360 is not used in this interface because the MC68360 asserts $\overline{\text{DS}}$ only after it latches a $\overline{\text{DSACK}}$ low. However, the HPI of the C6000 does not assert $\overline{\text{HRDY}}$ ($\overline{\text{DSACK1}}$) until after $\overline{\text{DS}}$ is asserted. Because of this timing conflict, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ of the TMS320C6000 HPI are tied logic low and high, respectively, to enable data strobe at all times.

The HPI must keep $\overline{\text{DSACKx}}$ asserted until it detects the negation of $\overline{\text{AS}}$ or $\overline{\text{DS}}$ (whichever it detects first). The C6000 must negate $\overline{\text{DSACKx}}$ within approximately one clock period after sampling negation of $\overline{\text{AS}}$ or $\overline{\text{DS}}$. $\overline{\text{DSACKx}}$ signals that remain asserted beyond this limit may be prematurely detected for the next bus cycle. This is avoided by using an OR combination of the $\overline{\text{HRDY}}$ and $\overline{\text{CSx}}$ signals.

$\overline{\text{HBE1}}$ and $\overline{\text{HBE2}}$ of the HPI are tied low to enable host access to both lower and upper bytes of the halfword during a write in the TMS320C6201/6701. Although the MC68360 has byte write enable signals $\overline{\text{WE1}}$ and $\overline{\text{WE0}}$, they are not used in this interface because of timing issues. The HPI expects control signals, including $\overline{\text{HBE1}}$ and $\overline{\text{HBE0}}$, to be ready before data strobe (which is $\overline{\text{HCS}}$ in this case) is asserted. However, MC68360 asserts chip-select and write-enable signals at the same time. Therefore, $\overline{\text{WE1}}$ and $\overline{\text{WE0}}$ cannot be used.

The auto-vector (AVEC) signal is used to terminate interrupt acknowledge cycles, indicating that the QUICC should internally generate a vector (auto-vector) number to locate an interrupt handler routine. AVEC is ignored during all other bus cycles.

1.1 Configuration

The QUICC is comprised of three modules:

- CPU32+ core
- System integration module (SIM60)
- Communication processor module (CPM)

The memory controller is a sub-block of the SIM60 that is responsible for up to eight general-purpose chip-select lines. The general-purpose chip-selects are available on lines CS0-CS7. CS0 also functions as the global (boot) chip-select for accessing the boot EPROM. The SIM60 supports a glue-less interface to HPI.

All internal memory and registers of the MC68360 occupy a single 8K-byte memory block that can be relocated along 8K-byte boundaries. The location is fixed by writing the desired base address of the 8K-byte memory block to the MBAR. The 8K-byte block is divided into two 4K-byte sections. The RAM occupies the first section; the internal registers occupy the second section. The LSB (least significant bit) of the MBAR register indicates when the contents of the MBAR are valid (if the bit is equal to one the content is valid).

The MC68360's general-purpose chip-selects are controlled by the global memory register (GMR) and the memory controller status register (MSTAT). There is one GMR and MSTAT in the memory controller. The MSTAT reports write-protect violations and parity errors for all banks. The 32-bit read-write GMR contains selections that are common to the entire memory controller. The GMR is used to control global parameters for memory banks. The DPS bit field of the GMR register must be set to DPS[1:0] = 11 to enable external DSACKx response. The PBEE bit of the GMR register should be set to zero to disable parity bus error detection.

The 32-bit read-write GMR contains selections that are common to the entire memory controller. The GMR is used to control global parameters for memory banks.

The MSTAT reports write-protect violations and parity errors for all banks.

The configuration of the BR and OR registers is shown in Table 2 and Table 3.

Table 2. Base Register 0 (BR0) Relevant Bits (MC68360)

Bit Field	Description	Value
CSNTQ	CS negate timing This bit is used to determine when CS is negated during an internal QUICC or external QUICC/MC68030-type bus-master write cycle.	Set to 0 (CS negated normally).
TRLXQ	Timing relax This bit delays the beginning of the internal QUICC or external QUICC/MC68030-type bus-master cycle to relax the timing constraints on the user.	Set to 0 (do not relax timing).
V	Valid bit	1 = content of BR0 and OR0 pair is valid
PAREN	Parity checking enable	0 = parity checking disabled
BA31-BA11	Base address The base address field, the upper 21 bits of each BR, and the function field are compared to the address on address bus to determine if a DRAM/SRAM region is being accessed by an internal QUICC master.	

The option register is 32-bit read-write register that may be accessed at any time.

Table 3. Option Register (OR) Relevant Bits (MC68360)

Bit Field	Description	Value
DSSEL	Dynamic RAM select This bit determines if the bank is SRAM or DRAM.	For HPI, set to 0.
SPS1-SPS0	SRAM port size Because external DSACKx is used, SPS[1:0] = 11	SPS0 = 1 SPS1 = 1
AM27-AM11	Address mask Mask any of the corresponding bits in the associated BR. By masking the address bits independently, external devices of different address range sizes can be used.	All base address and function code bits will be used in the bank hit comparison (all bits of the AM bit field are set to one).
TCYC3-TCYC0	Cycle length in clocks	Because external DSACKx is selected with SPS, TCYC should not be set to zero.

2 MC68360 to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) an MC68360 write to HPI and 2) an MC68360 read from HPI. In each instance, timing requirements were compared for each of the devices. The results are shown in Figure 3 through Figure 6 and the timing requirements tables immediately following these figures. In all figures and tables, timing parameters are named in the same way as those in the data sheets for the TMS320C6000 and MC68360 devices. Actual timing parameter values are listed in Appendix A and Appendix B.

Figure 3 through Figure 6 and the timing requirement tables show that the timing parameters for both devices are met in all interfaces between the MC68360 and HPI. These interfaces are based on a MC68360/25-MHz device and TMS320C6x™ devices operating at any frequency range.

TMS320C6x is a trademark of Texas Instruments.

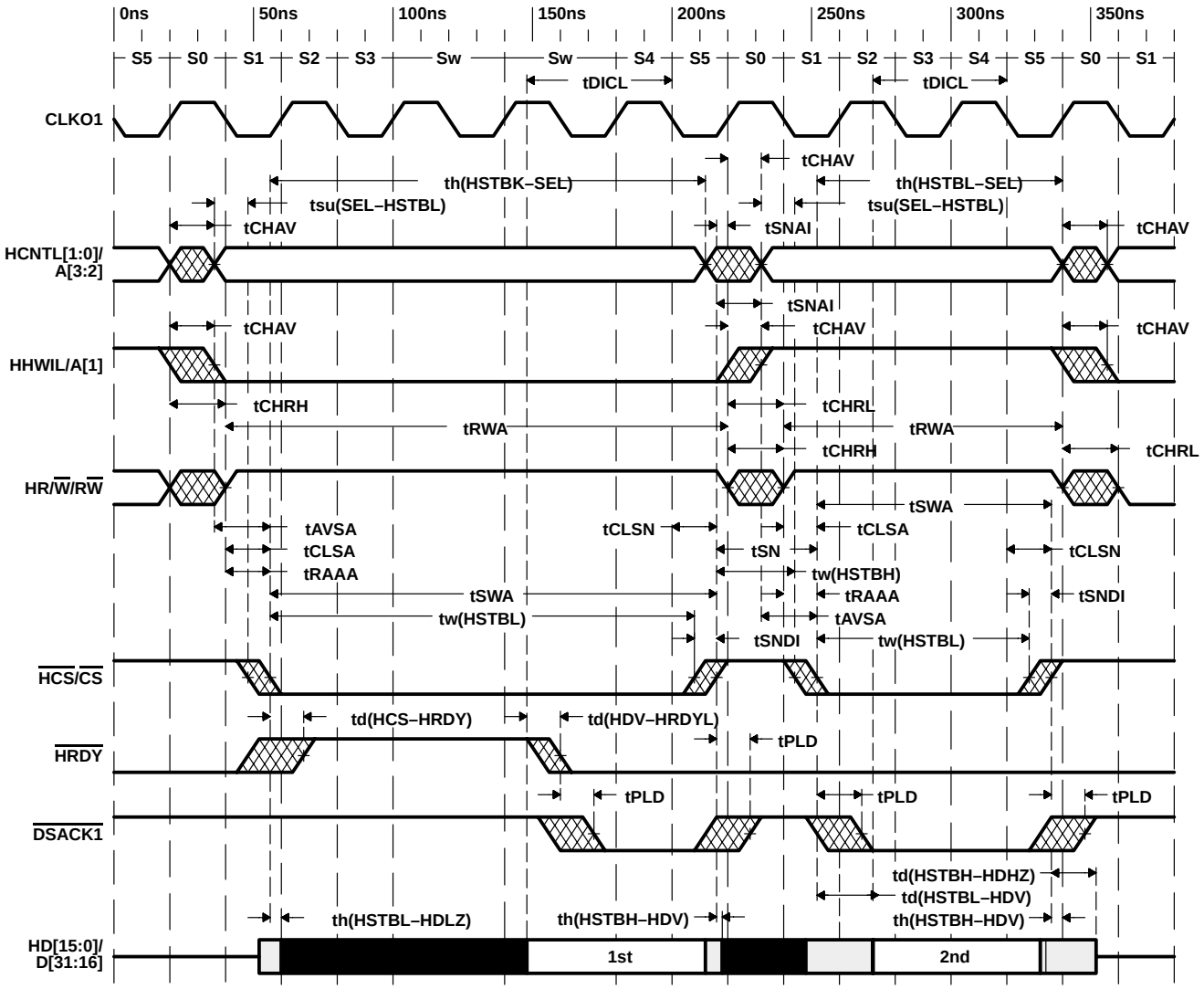

Figure 3. MC68360 Reads Internal Memory of TMS320C62x/C67x/C64x (HPI16 Mode) Using HPI (Read Without Auto-Increment)

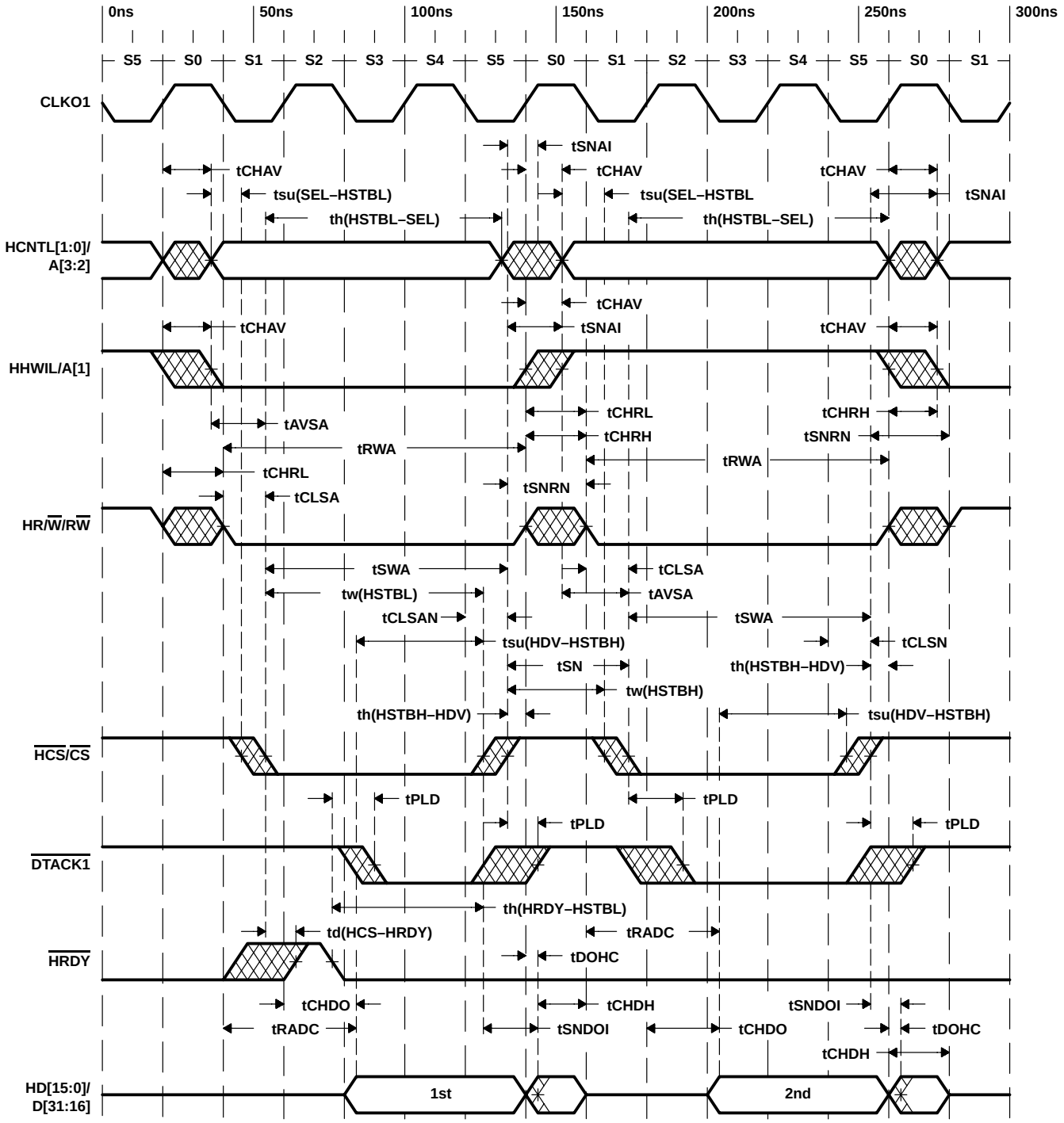

Figure 4. MC68360 Write to TMS320C62x/C67x/C64x (HPI16 Mode) HPI

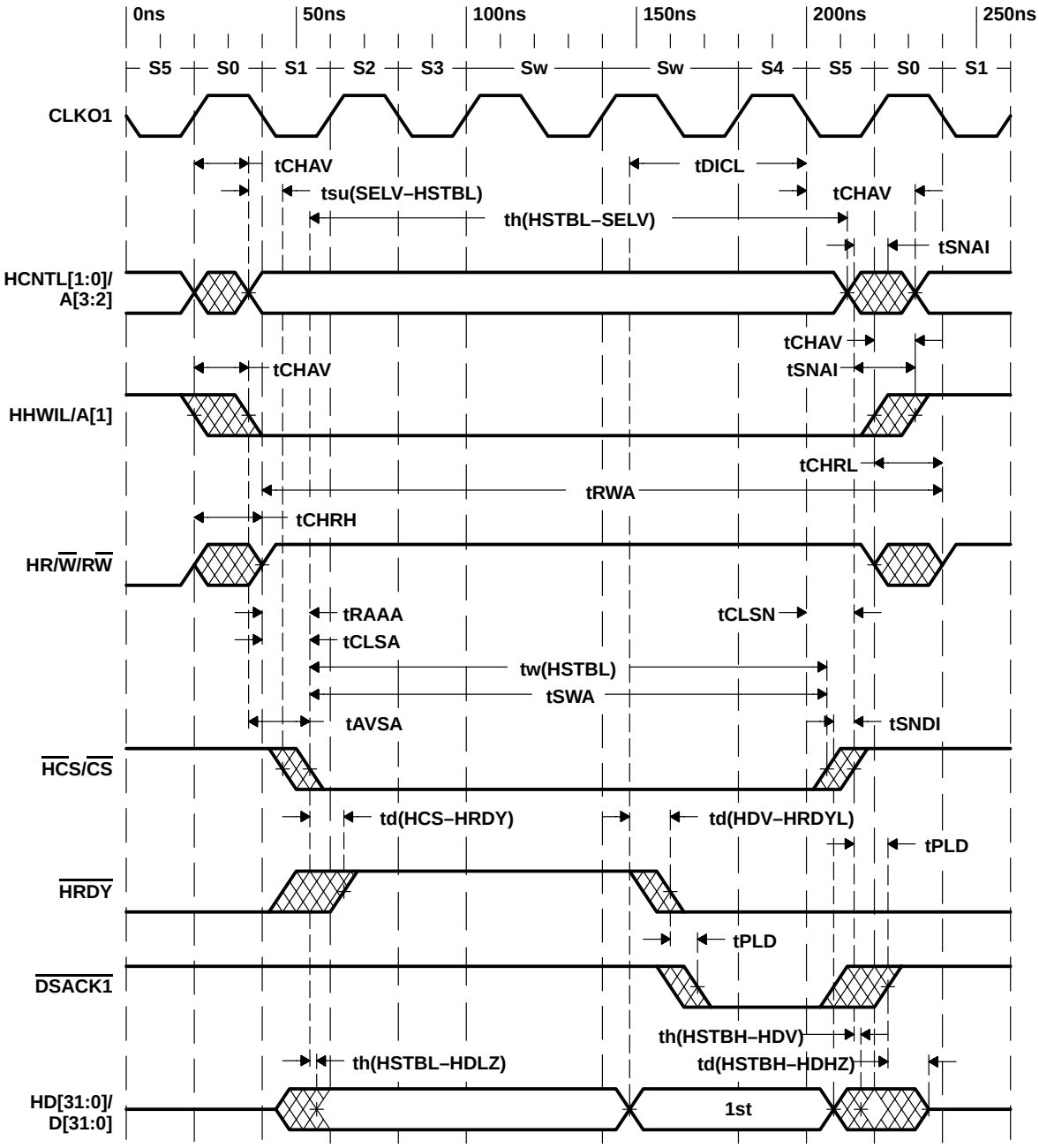

Figure 5. MC68360 Reads Internal Memory of TMS320C64x (HPI32 Mode) Using HPI (Read Without Auto-Increment)

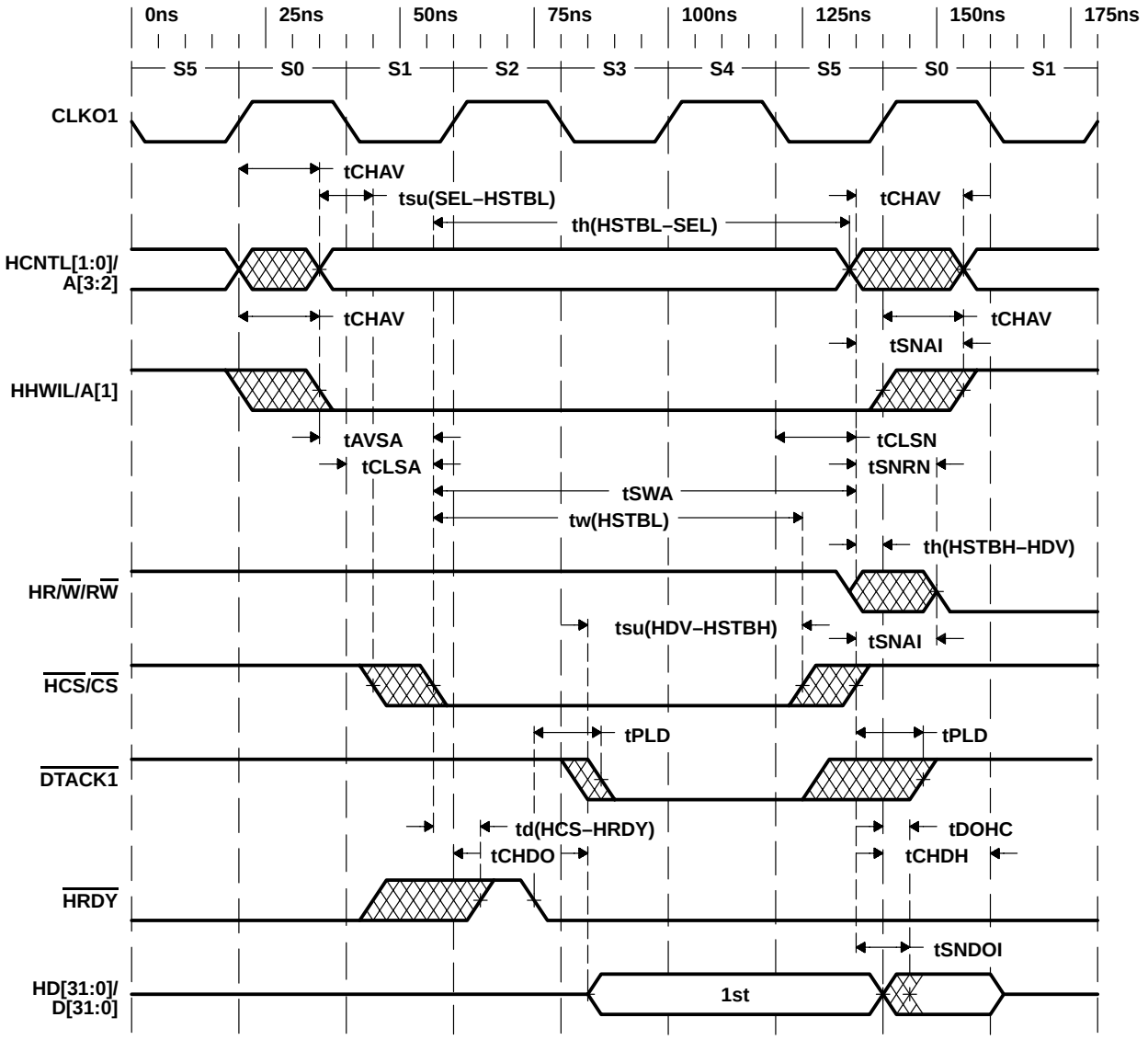

Figure 6. MC68360 Write to TMS320C64x (HPI32 Mode) HPI

Table 4. Timing Requirements for the C6201/C6701 HPI

HPI Symbol	MC68360 Symbol		Min HPI (ns)	Min MC68360 (ns)
$t_{su(SEL-HSTBL)}$	t_{AVSA}	Setup time, select signals valid before HSTROBE low	4	10
$t_{h(HSTBL-SEL)}$	$t_{SNAI} + t_{SWA}$	Hold time, select signals valid after HSTROBE low	2	85
$t_{w(HSTBL)}$	t_{SWA}	Pulse duration, HSTROBE low	$2*P_H = 10$	75
$t_{w(HSTBH)}$	t_{SN}	Pulse duration, HSTROBE high	$2*P_H = 10$	35
$t_{su(HDV-HSTBH)}$	$1.5*P_M - t_{CHDO} + t_{CLSN}$	Setup time, host data valid before HSTROBE high	3	41
$t_{h(HSTBH-HDV)}$	t_{SNDOI}	Hold time, host data valid after HSTROBE high	2	10
$t_{h(HRDYL-HSTBL)}$	$0.5* P_M + t_{CLSN}$	Hold time, HSTROBE low after HRDY low	1	24

NOTE: P_H = Period of TMS3206201/6701DSP clock = 5 ns @ 200 MHz.
P_M = Period of MC68360 clock = 40 ns @ 25 MHz.

Table 5. Timing Requirements for MC68360 Interfaced to the C6201/C6701 HPI

HPI Symbol	MC68360 Symbol		Min HPI (ns)	Min MC68360 (ns)
$t_{oh(HSTBH-HDV)}$	t_{SNDI}	Hold time, input data from $\overline{CS}$ negated	2	0
$2* P_M - t_{CLSA} - t_{d(HSTBL-HDV)}$	t_{DICL}	Read set-up time, data-in valid to clock low	52	1

NOTE: P_M = Period of MC68360 clock = 40ns @ 25 MHz.

Table 6. Timing Requirements for the C6211/C6711 HPI

HPI Symbol	MC68360 Symbol		Min HPI (ns)	Min MC68360 (ns)
$t_{su(SELV-HSTBL)}$	t_{AVSA}	Setup time, Select signals valid before HSTROBE low	5	10
$t_{h(HSTBL-SELV)}$	$t_{SNAI} + t_{SWA}$	Hold time, select signals valid after HSTROBE low	4	85
$t_{w(HSTBL)}$	t_{SWA}	Pulse Duration, HSTROBE low	$4*P_H = 24$	75
$t_{w(HSTBH)}$	t_{SN}	Pulse Duration, HSTROBE high	$4*P_H = 24$	35
$t_{su(HDV-HSTBH)}$	$1.5*P_M - t_{CHDO} + t_{CLSN}$	Setup time, host data valid before HSTROBE high	5	41
$t_{h(HSTBH-HDV)}$	t_{SNDOI}	Hold time, host data valid after HSTROBE high	3	10
$t_{h(HRDYL-HSTBL)}$	$0.5* P_M + t_{CLSN}$	Hold time, HSTROBE low after HRDY low	2	24

NOTE: P_H = Period of TMS3206211/6711 DSP clock = 6 ns @ 167 MHz.
P_M = Period of MC68360 clock = 40 ns @ 25 MHz.

Table 7. Timing Requirements for MC68360 Interfaced to the C6211/C6711 HPI

HPI Symbol	MC68360 Symbol		Min HPI (ns)	Min MC68360 (ns)
$t_{oh(HSTBH-HDV)}$	t_{SNDI}	Hold time, input data from $\overline{CS}$ negated	2	0
$2* P_M - t_{CLSA} - t_{d(HSTBL-HDV)}$	t_{DICL}	Read set-up time, data-in valid to clock low	52	1

NOTE: P_M = Period of MC68360 clock = 40 ns @ 25 MHz.

Table 8. Timing Requirements for the C64x HPI

HPI Symbol	MC68360 Symbol		Min HPI (ns)	Min MC68360 (ns)
$t_{su(SEL-HSTBL)}$	t_{AVSA}	Setup time, select signals valid before HSTROBE low	4	10
$t_{h(HSTBL-SEL)}$	$t_{SNAI} + t_{SWA}$	Hold time, select signals valid after HSTROBE low	2	85
$t_{w(HSTBL)}$	t_{SWA}	Pulse duration, HSTROBE low	$4*P_H = 10$	75
$t_{w(HSTBH)}$	t_{SN}	Pulse duration, HSTROBE high	$4*P_H = 10$	35
$t_{su(HDV-HSTBH)}$	$1.5*P_M - t_{CHDO} + t_{CLSN}$	Setup time, host data valid before HSTROBE high	5	41
$t_{h(HSTBH-HDV)}$	t_{SNDOI}	Hold time, host data valid after HSTROBE high	2	10
$t_{h(HRDYL-HSTBL)}$	$0.5* P_M + t_{CLSN}$	Hold time, HSTROBE low after HRDY low	2	24

NOTE: P_H = Period of TMS320C64x DSP clock = 2.5 ns @ 400 MHz.
P_M = Period of MC68360 clock = 40 ns @ 25 MHz.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest datasheet for numbers.

Table 9. Timing Requirements for MC68360 Interfaced to the C64x HPI

HPI Symbol	MC68360 Symbol		Min HPI (ns)	Min MC68360 (ns)
$t_{oh(HSTBH-HDV)}$	t_{SNDI}	Hold time, input data from $\overline{CS}$ negated	2	0
$2* P_M - t_{CLSA} - t_{d(HSTBL-HDV)}$	t_{DICL}	Read set-up time, data-in valid to clock low	52	1

NOTE: P_M = Period of MC68360 clock = 40 ns @ 25 MHz.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest datasheet for numbers.

3 References

1. *TMS320C6200 Peripherals Reference Guide* (SPRU190).
2. *TMS320C6201 Digital Signal Processor* (SPRS051).
3. *TMS320C6701 Floating-Point Digital Signal Processor* (SPRS067).
4. *TMS320C6211, TMS320C6211B Fixed-Point Digital Signal Processors* (SPRS073).
5. *TMS320C6416 Fixed-Point Digital Signal Processor* (SPRS164).
6. MC68360 Quad Integrated Communications Controller User's Manual, Motorola, Inc.

Appendix A TMS320C6x Timing Requirements

Table A–1. TMS320C6201/C6701 Host Port Timing Specifications

Symbol	Characteristic	Min (ns)	Max (ns)
$t_{su(SEL-HSTBL)}$	Setup time, select signals§ valid before HSTROBE low †	4	
$t_{h(HSTBL-SEL)}$	Hold time, select signals§ valid after HSTROBE low †	2	
$t_{w(HSTBL)}$	Pulse duration, HSTROBE low †	2P‡	
$t_{w(HSTBH)}$	Pulse duration, HSTROBE high between consecutive accesses †	2P‡	
$t_{su(HDV-HSTBH)}$	Setup time, host data valid before HSTROBE high †	3	
$t_{h(HSTBH-HDV)}$	Hold time, host data valid after HSTROBE high †	2	
$t_{h(HRDYL-HSTBL)}$	Hold time, HSTROBE† low after HRDY low. HSTROBE should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.†	1	
$t_{d(HCS-HRDY)}$	Delay time, HCS to HRDY ¶	1	9
$t_{d(HSTBL-HRDYH)}$	Delay time, HSTROBE† low to HRDY high #	3	12
$t_{oh(HSTBL-HDLZ)}$	Output hold time, HD low impedance after HSTROBE† low for an HPI read	4	
$t_{d(HDV-HRDYL)}$	Delay time, HD valid to HRDY low	P‡ – 3	P‡ + 3
$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE† high	2	12
$t_{d(HSTBH-HDHZ)}$	Delay time, HSTROBE† high to HD high impedance	3	12
$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE† low to HD valid	3	12
$t_{d(HSTBH-HRDYH)}$	Delay time, HSTROBE† high to HRDY high ‖	3	12

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Table A–2. TMS320C6211/C6711 Host Port Timing Specifications

Symbol	Characteristic	Min (ns)	Max (ns)
$t_{su(SELV-HSTBL)}$	Setup time, select signals§ valid before HSTROBE low †	5	
$t_{h(HSTBL-SELV)}$	Hold time, select signals§ valid after HSTROBE low †	4	
$t_{w(HSTBL)}$	Pulse duration, HSTROBE low †	4P‡	
$t_{w(HSTBH)}$	Pulse duration, HSTROBE high between consecutive accesses †	4P‡	
$t_{su(HDV-HSTBH)}$	Setup time, host data valid before HSTROBE high †	5	
$t_{h(HSTBH-HDV)}$	Hold time, host data valid after HSTROBE high †	3	
$t_{h(HRDYL-HSTBL)}$	Hold time, HSTROBE† low after HRDY low. HSTROBE† should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	2	
$t_{d(HCS-HRDY)}$	Delay time, HCS to HRDY ¶	1	15
$t_{d(HSTBL-HRDYH)}$	Delay time, HSTROBE† low to HRDY high #	3	15
$t_{oh(HSTBL-HDLZ)}$	Output hold time, HD low impedance after HSTROBE† low for an HPI read	2	
$t_{d(HDV-HRDYL)}$	Delay time, HD valid to HRDY low	2P‡ – 4	2P‡
$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE high †	3	15
$t_{d(HSTBH-HDHZ)}$	Delay time, HSTROBE high to HD high impedance †	3	15
$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE low to HD valid †	3	15
$t_{d(HSTBH-HRDYH)}$	Delay time, HSTROBE † high to HRDY high ‖	3	15

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Table A–3. TMS320C64x Host Port Timing Specifications

Symbol	Characteristic	Min (ns)	Max (ns)
$t_{su(SELV-HSTBL)}$	Setup time, select signals§ valid before HSTROBE† low	5	
$t_{h(HSTBL-SELV)}$	Hold time, select signals§ valid after HSTROBE† low	2	
$t_{w(HSTBL)}$	Pulse duration, HSTROBE† low	4P‡	
$t_{w(HSTBH)}$	Pulse duration, HSTROBE† high between consecutive accesses	4P‡	
$t_{su(HDV-HSTBH)}$	Setup time, host data valid before HSTROBE† high	5	
$t_{h(HSTBH-HDV)}$	Hold time, host data valid after HSTROBE† high	2	
$t_{h(HRDYL-HSTBL)}$	Hold time, HSTROBE† low after HRDY low. HSTROBE† should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	2	
$t_{d(HCS-HRDY)}$	Delay time, HCS to HRDY¶	1	7
$t_{d(HSTBL-HRDYH)}$	Delay time, HSTROBE low to HRDY high #	3	12
$t_{oh(HSTBL-HDLZ)}$	Output hold time, HD low impedance after HSTROBE† low for an HPI read	2	
$t_{d(HDV-HRDYL)}$	Delay time, HD valid to HRDY low	2P‡ – 6	
$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE† high	3	
$t_{d(HSTBH-HDHZ)}$	Delay time, HSTROBE† high to HD high impedance		12
$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE† low to HD valid		12
$t_{d(HSTBH-HRDYH)}$	Delay time, HSTROBE† high to HRDY high ‖	3	12

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.
NOTE: The timing specifications above are preliminary and the actual numbers may vary with a TMS part. Please refer to the latest data sheet for numbers.

The timing requirements in the tables above are provided for quick reference only. For detailed description, notes, and restrictions, please see the data sheets listed in the section.

Appendix B MC68360 Timing Requirements

Table B–1. Motorola MC68360 Timing Parameters

Symbol	Characteristic	Min (ns)	Max (ns)
t_{CHAV}	CLKO1 high to address, FC valid [6]	0	15
t_{CHAZn}	CLKO1 high to address, FC Invalid [8]	0	
t_{CLSA}	CLKO1 low to $\overline{CS}$ asserted [9]	4	16
t_{STSA}	AS to DS or $\overline{CS}$ asserted [9A]	–6	6
t_{STCA}	AS to $\overline{CS}$ asserted [9C]	14	26
t_{AVSA}	Address valid to AS,$\overline{CS}$,OE asserted [11]	10	
t_{CLSN}	CLKO1 low to $\overline{CS}$ negated [12]	4	16
t_{SNAI}	AS,DS,$\overline{CS}$,OE,WE negated to address, FC invalid (address hold) [13]	10	
t_{SWA}	AS,$\overline{CS}$,OE and DS (read) width asserted [14]	75	
t_{SN}	AS,DS,$\overline{CS}$,OE width negated [15]	35	
t_{CHSZ}	CLKO1 high to AS,DS,R/$\overline{W}$ high impedance [16]		40
t_{SNRN}	AS,DS,$\overline{CS}$,WE negated to R/W high [17]	10	
t_{CHRH}	CLKO1 high to R/W high [18]	0	20
t_{CHRL}	CLKO1 high to R/W low [20]	0	20
t_{RAAA}	R/W high to AS,$\overline{CS}$, OE asserted [21]	10	
t_{RASA}	R/$\overline{W}$ low to $\overline{DS}$ asserted (write) [22]	47	
t_{CHDO}	CLKO1 high to data-out valid [23]		23
t_{SNDOI}	DS,$\overline{CS}$,WE negated to data-out invalid (data out hold) [25]	10	
t_{DVSA}	Data out valid to DS asserted (write) [26]	10	
t_{DICL}	Data In to CLKO1 low (data setup) [27]	1	
t_{SNDN}	AS,DS, negated to $\overline{DSACK}$ negated [28]	0	50
t_{SNDI}	DS,$\overline{CS}$,OE negated to data in invalid (data in hold) [29]	0	
t_{SHDI}	DS,$\overline{CS}$,OE negated to data in high Z [29A]		40
t_{DADV}	$\overline{DSACK}$ asserted to $\overline{DSACK}$ valid (skew) [31A]		10
t_{RWA}	R/$\overline{W}$ width asserted (write or read) [46]	100	
t_{AIST}	Async input setup time [47A]	5	
t_{AIHT}	Async input hold time [47B]	10	
t_{DOHC}	Data out from CLKO1 high [53]	0	

Table B–1. Motorola MC68360 Timing Parameters (Continued)

Symbol	Characteristic	Min (ns)	Max (ns)
t_{CHDH}	CLKO1 high to data-out high Z [54]		20
t_{RADC}	R/W asserted to data bus impedance change [55]	25	

The timing requirements in are provided for quick reference only. For detailed description, notes, and restrictions, please see the *MC68360 Quad Integrated Communications Controller User's Manual*.

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