Application Report
SPRA542A

TMS320C6000 EMIF to External Asynchronous SRAM Interface

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Abstract

Interfacing external asynchronous static RAM (ASRAM) to the Texas Instruments (TI™) TMS320C6000 series of digital signal processors (DSPs) is simple compared to previous generations of TI DSPs, thanks to the advanced external memory interface (EMIF). The EMIF provides a glueless interface to a variety of external memory devices.

This document describes:

- EMIF control registers and ASRAM signals
- ASRAM functionality and performance considerations
- Full example using Toshiba's TC55V1664FT-12 (64k x 16, 12 ns)
- Full example using the IDT71V016S25 (64k x 16, 25 ns) from Integrated Device Technology, Inc. (IDT)

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Asynchronous SRAM Interface

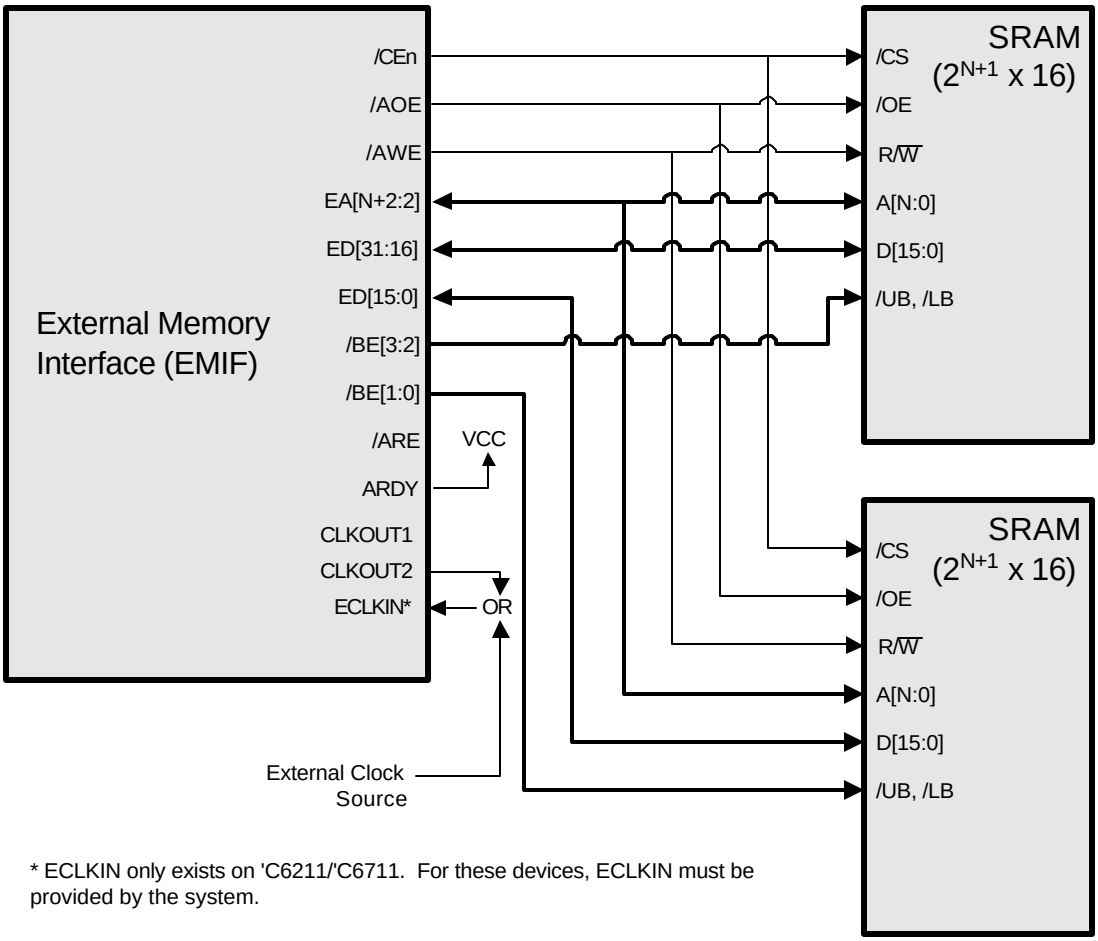
The asynchronous interface of the EMIF offers users configurable memory cycles and can be used to interface to a variety of memory and peripheral types; including SRAM, EPROM, and FLASH as well as FPGA and ASIC designs. This document focuses on the interface between the EMIF and asynchronous SRAM (ASRAM).

Figure 1 shows an interface to 16-bit-wide standard SRAM. Most ‘C6000 devices support only a 32 bit-wide interface, so, in this example, two devices must be used in parallel to produce a 32-bit word. Similarly, if an 8-bit-wide ASRAM is used, four devices are required.

Some devices in the ‘C6000 family support 32-, 16-, and 8-bit-wide memory interfaces. An example interface is shown in Figure 2 using a single 8-bit-wide device.

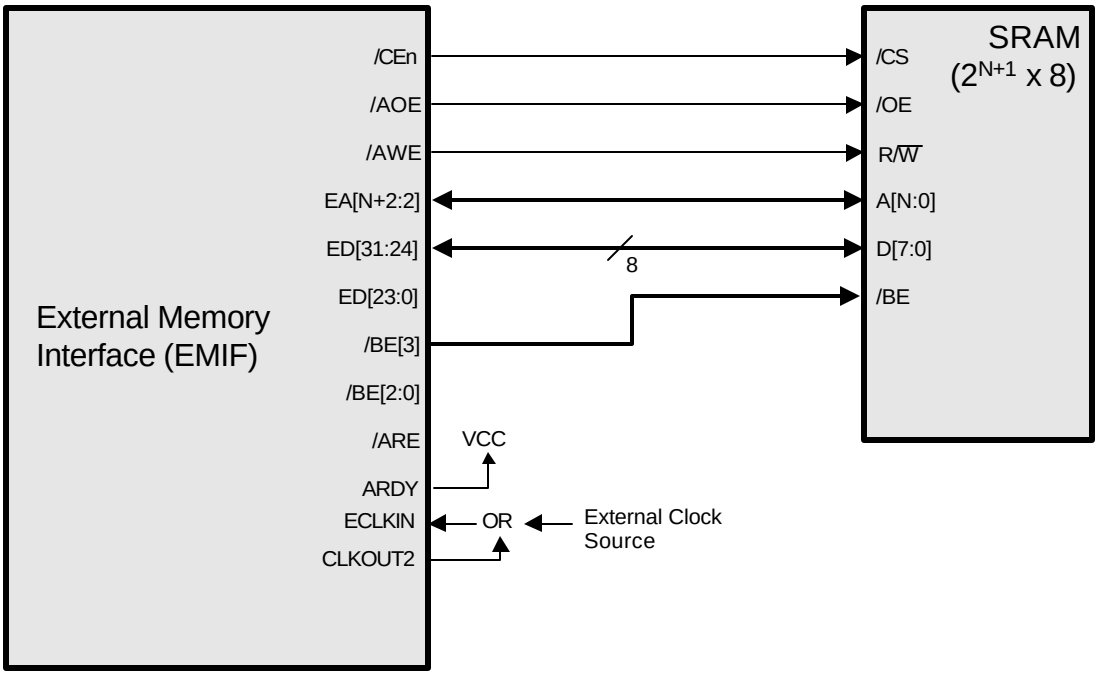
Note that in these diagrams there is no clock interface between the SRAM and the EMIF, as is indicated by the term asynchronous. The EMIF still uses the internal clock to coordinate the timing of its signals but the SRAM responds to the signals at its inputs irrespective of any clock.

Figure 1. EMIF-SRAM Interface (All C6000 Devices)



* ECLKIN only exists on 'C6211/'C6711. For these devices, ECLKIN must be provided by the system.

Figure 2. EMIF—Big-Endian x8 ASRAM Interface ('C6211/'C6711 Only)



Overview of EMIF

'C6201/'C6202/'C6701 ASRAM Interface

- Signals are timed relative to CLKOUT1.
- Supports only 32-bit-wide ASRAM Interface. Supports x16 and x8 read-only interfaces.

'C6211/'C6711 ASRAM Interface

- Signals are timed relative to ECLKIN. An external clock can be tied to ECLKIN for maximum flexibility or CLKOUT2 can be routed back to ECLKIN for simplicity. ECLKIN can operate at up to 100 MHz.
- Supports 32-, 16-, and 8-bit-wide ASRAM interface.

EMIF Signal Descriptions

Figure 3 and Figure 4 show a block diagram of the EMIF. As the figures show, the EMIF is the interface between external memory and the other internal units of the ‘C6000. The interface with the processor on the ‘C6201/’C6202/’C6701 is provided via the DMA controller, program memory controller, and the data memory controller. The interface with the processor on the ‘C6211/’C6711 is provided via the enhanced DMA. The signals described in Table 1, however, focus on the ASRAM interface and the shared interface signals.

Figure 3. Block Diagram of ‘C6201/’C6202/’C6701 EMIF

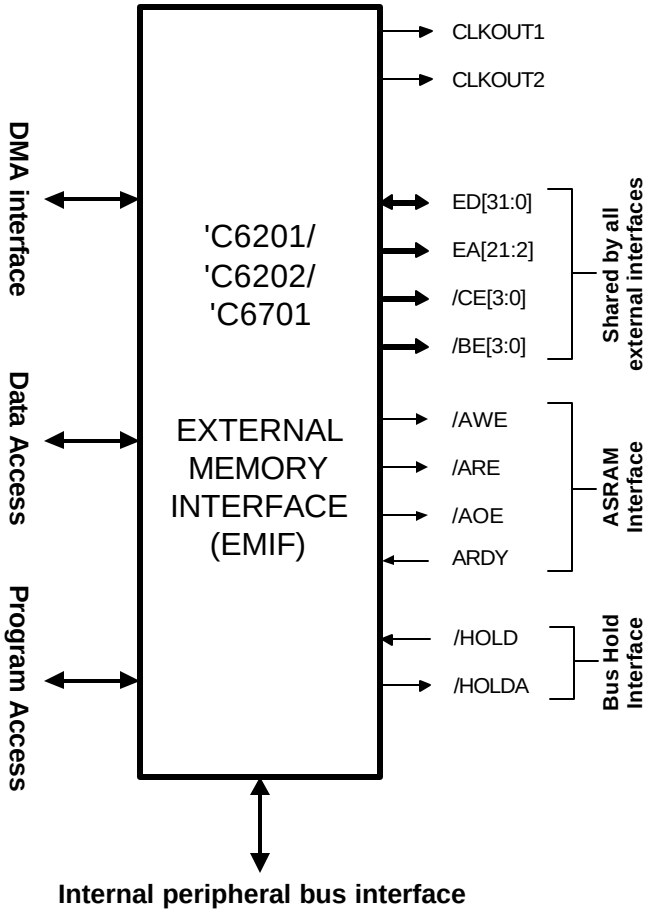


Figure 4. Block Diagram of 'C6211/'C6711 EMIF

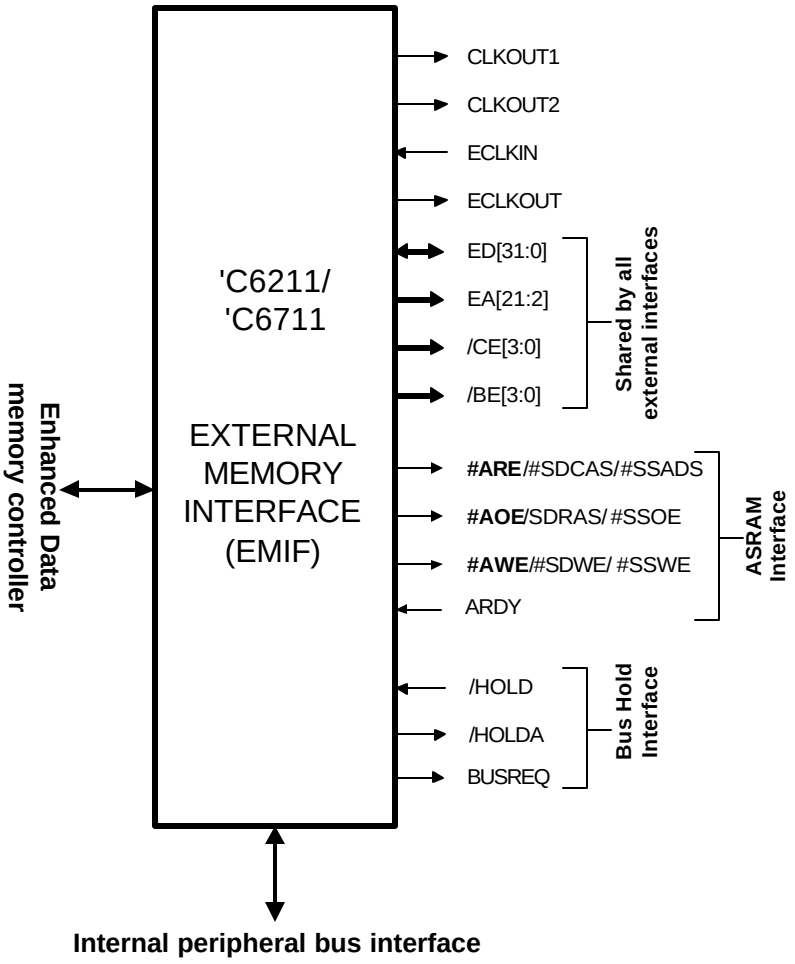


Table 1. EMIF Signal Descriptions: Shared Signals and ASRAM Signals

EMIF Pin	ASRAM Signal	Description
ED[31:0]	DQ	Data I/O. 32-bit data input/output from external memories and peripherals
EA[21:2]	A	External address output. Drives bits 21-2 of the byte address.
/CE[3:0]	CS	External /CE space chip-select. Active-low chip-select for memory spaces 0 through 3.
/BE[3:0]	_UB/ _LB	Byte enables. Active-low byte strobes. Individual bytes and halfwords can be selected for both read and write cycles. Decoded from two LSBs of the byte address.
/AOE	/OE	Output enable—active low during the entire period of a read access
/AWE	/WE	Write enable—active low during a write transfer strobe period
/ARE	N/A	Read enable—active low during a read transfer strobe period. Although not used for standard ASRAM interface, still used logically to determine when the data is read by the EMIF.
ARDY	N/A	Ready input used to insert wait states into the memory cycle. Not used for standard ASRAM interface.

Clocking the ‘C6211/’C6711 EMIF

The EMIF of the ‘C6211/’C6711 requires an external clock to be provided via the ECLKIN input. For simplicity, CLKOUT2 can be routed into the ECLKIN pin to avoid the extra hardware required to create a clock externally. This method has the restriction of only allowing a memory interface at 1/2x the CPU clock speed (which is 75 MHz for a 150-MHz device).

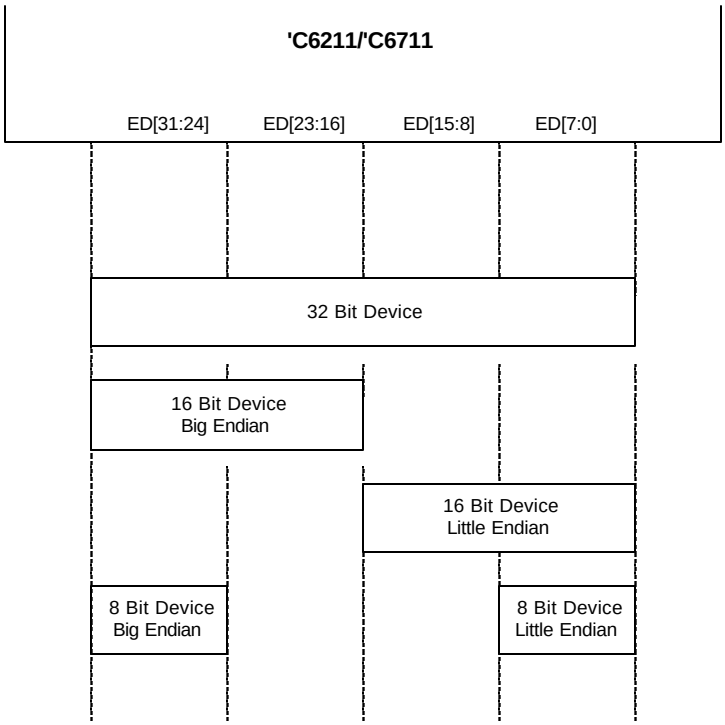
If an external clock is provided, the EMIF can operate up to 100 MHz. The *TMS320C6211 Fixed-Point Digital Signal Processor* and *TMS320C6711 Floating-Point Digital Signal Processor* data sheets specify that the rise/fall time of the externally provided clock must be no longer than 3 ns. This can prove difficult with most off-the-shelf oscillators. The recommended approach is to use the ICS501 PLL multiplier chip, which can produce a wide range of frequency outputs with standard crystals.

Byte Lane Alignment on the ‘C6211/’C6711 EMIF

The ‘C6211/‘C6711 EMIF offers the capability to interface to 32-, 16-, and 8-bit-wide memories. Depending on the endianness of the system, a different byte lane is used for all-memory interfaces. The alignment required is shown in Figure 5.

Note that BE3 always corresponds to ED[31:24], BE2 always corresponds to ED[23:16], BE1 always corresponds to ED[15:8], and BE0 always corresponds to ED[7:0], regardless of endianness.

Figure 5. Byte Lane Alignment vs. Endianness on the 'C6211/'C6711



EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory-mapped registers within the EMIF. The memory-mapped registers are shown in Table 2.

Table 2. EMIF Memory Mapped Registers

Byte Address	Name
0x01800000	EMIF global control
0x01800004	EMIF CE1 space control
0x01800008	EMIF CE0 space control
0x0180000C	Reserved
0x01800010	EMIF CE2 space control
0x01800014	EMIF CE3 space control

CE Space Control Registers

The four CE space control registers (Figure 6) correspond to the four CE spaces supported by the EMIF. The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply. If an asynchronous type is selected (ROM or 32-bit asynchronous), the remaining fields specify the shaping of the address and control signals for access to that space. Table 3 contains a more detailed description of the asynchronous configuration fields.

Figure 6. 'C6201/'C6202/'C6701 EMIF CE(0/1/2/3) Space Control Register Diagram

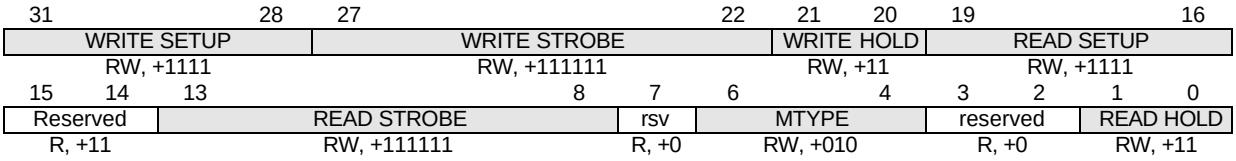


Figure 7. 'C6211/'C6711 EMIF CE(0/1/2/3) Space Control Register Diagram

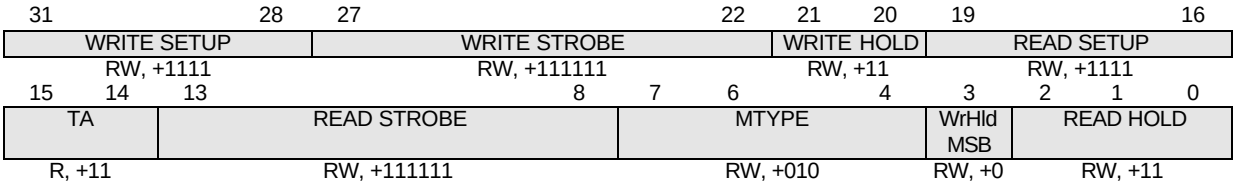


Table 3. EMIF CE(0/1/2/3) Space Control Registers Bitfield Description

Field	Description
READ SETUP WRITE SETUP	Setup width. Number of clock† cycles of setup for address (EA) and byte enables (/BE(0-3)) before read strobe (/ARE) or write strobe (/AWE) falling. On the first access to a CE space, this is also the setup after /CE falling.
READ STROBE WRITE STROBE	Strobe width. The width of read strobe (/ARE) and write strobe (/AWE) in clock* cycles.
READ HOLD WRITE HOLD	Hold width. Number of clock† cycles that address (EA) and byte strobes (/BE(0-3)) are held after read strobe (/ARE) or write strobe (/AWE) rising. These fields are extended by one bit on the 'C6211/'C6711.
MTYPE	Memory type 'C6201/'C6202/'C6701 only: MTYPE = 000b: 8-bit-wide ROM (CE1 only) MTYPE = 001b: 16-bit-wide ROM (CE1 only) MTYPE = 010b: 32-bit-wide asynchronous interface 'C6211/'C6711 only: MTYPE = 0000b: 8-bit-wide asynchronous interface MTYPE = 0001b: 16-bit-wide asynchronous interface MTYPE = 0010b: 32-bit-wide asynchronous interface
TA‡	Turnaround time. Controls the number of ECLKOUT cycles between a read and a write or between two reads.

† Clock = CLKOUT1 for 'C6201/'C6202/'C6701. Clock = ECLKOUT for 'C6211/'C6711.
‡ Applies to 'C6211/'C6711 only.

Programmable ASRAM Parameters

The EMIF allows a high degree of programmability for shaping asynchronous accesses. The programmable parameters that allow this are:

- **Setup:** Time between the beginning of a memory cycle (/CE low, address valid) and the activation of the read or write strobe
- **Strobe:** Time between the activation and deactivation of the read (/ARE) or write strobe (/AWE)
- **Hold:** Time between the deactivation of the read or write strobe and the end of the cycle (which may be either an address change or the deactivation of the /CE signal)
- **Turnaround[1]:** Time between the end of a read cycle and the beginning of a write cycle, or the time between two reads from different CE spaces.

On the 'C6201/'C6202/'C6701, these parameters are programmable in terms of CPU clock cycles (CLKOUT1) via fields in the EMIF CE space control registers. On the 'C6211/'C6711, these parameters are programmable in terms of ECLKOUT cycles. Separate setup, strobe, and hold parameters are available for read and write accesses. The SETUP, HOLD, and STROBE fields represent actual cycle counts, in contrast to the SDRAM parameters, which are the cycle counts - 1.

[1] Applies to 'C6211/'C6711 only

The minimum settings are

- Setup ≥ 1 (0 treated as 1)
- Strobe ≥ 1 (0 treated as 1)
- Hold ≥ 0

Because the SETUP and STROBE fields have minimum counts of 1, a value of 0 in these fields is interpreted as a 1 by the C6000. On the 'C6201/'C6701/'C6202, for the first access in a set of consecutive accesses or a single access, the setup period has a minimum of 2. HOLD has a minimum of 0.

The following sections explain these parameters and the guidelines that should be used when setting the SETUP, HOLD, and STROBE parameters. Table 5 through Table 8 define constraints used in the following discussion.

Margin Considerations

Notice that the output signals from the C6000 are output a time t_d after the rising edge of CLKOUT1 ('C6201/'C6202/'C6701) or ECLKOUT ('C6211/'C6711). The data sheet for the C6000 gives both a maximum delay time and a minimum delay time. Therefore, over a range of operating temperatures and supply voltage levels, the actual value of t_d can range between these two extremes. However, for a given set of operating conditions, the delay time will be the same more or less for both the transition from inactive to active and again for the transition from active to inactive. Therefore, the effect of t_d on output signals cancels itself out. Based on design simulations, the maximum skew between any two output control, address, and data signal can be approximated as 2 ns. This parameter (referred to as t_{skew}) is used in the following calculations.

For example, assume that a write pulse (t_{wp}) of 5 ns is required by the memory, the 'C6201B CPU is operating at a frequency of 200 MHz (5 ns CLKOUT1), and the delay time, t_d, is 3 ns (see Figure 10). Assuming that STROBE is set to 1, the transition of AWE from inactive to active occurs ~3 ns after the rising edge of CLKOUT1, and the transition from active to inactive occurs ~3 ns after the next rising edge of CLKOUT1. This leaves a write strobe length of 5 ns, as desired. This example assumes no margin is included. To ensure that timings are met, additional time must be inserted to account for t_{skew} and any other board skew.

Therefore, for the calculations below, the delay time is not included for output signal requirements, but the time t_{skew} is. A time t_{margin} is calculated for each of the measurements in the examples below to account for any additional board level skew time and loading issues. As a general constraint, the examples require the output margin to be within 1 ns. If the necessary margin is not met, the corresponding parameter can be increased by a cycle. This time is only a rough guideline. For any system, the necessary margin should be determined.

For the read cycles, two situations arise that require different amounts of margin. First, for the parameters that affect the input setup to the 'C6000, extra timing margin (~2ns) is recommended to account for the propagation of the output control/address signals from the C6000 to the memory and the propagation of the data back to the C6000 from the memory. For these calculations, the maximum output delay of the C6000 is also included to create a worst-case calculation because there is no canceling effect of the delay times for this situation. No additional margin is required for the input hold time requirement of the C6000 because of the two propagation delays previously mentioned. The propagation delays guarantee that hold timings are met without any additional margin added in.

It is important to realize that the recommended margins described here are only a guideline, which might apply to a well-designed board with relatively short board traces. The timing margin required for any design should be verified. With the asynchronous interface, additional margin can always be created by adding additional cycles in the appropriate field.

For the following discussion, t_{cyc} refers to the period of the clock used for asynchronous programming. Therefore, for the 'C6201/'C6202/'C6701, t_{cyc} is equal to the period of the CPU clock (which is equal to CLKOUT1). For the 'C6211/'C6711, t_{cyc} is equal to the period of ECLKOUT (which is equal to ECLKIN).

Table 4. Recommended Timing Margin

Timing Parameter	Recommended Margin
Output Setup	~1 ns
Output Hold	~1 ns
Input Setup	~2 ns
Input Hold	~0 ns

Table 5. EMIF—Input Timing Requirements (Input Data)

Timing Parameter	Definition
t_{isu}	Data setup time, read D before CLKOUT1 high
t_h	Data hold time, read D after CLKOUT1 high

Table 6. EMIF—Output Timing Characteristics (Data, Address, Control)

Timing Parameter	Definition
t_d	Output delay time, CLKOUT1 high to output signal valid

Table 7. ASRAM—Input Timing Requirement

Timing Parameter	Definition
$t_{xw(m)}$	Time from control/data signals active to /AWE inactive
$t_{wp(m)}$	Write pulse width
$t_{ih(m)}$, $t_{wr(m)}$	Maximum of either write recovery time or data hold time
$t_{rc(m)}$	Length of the read cycle
$t_{wc(m)}$	Length of the write cycle

Table 8. ASRAM—Output Timing Characteristics

Timing Parameter	Definition
$t_{acc(m)}$	Access time, from EA, /BE, /AOE, /CE active to ED valid
$t_{oh(m)}$	Output hold time

Asynchronous Reads

Figure 8 illustrates an asynchronous read cycle with a setup/strobe/hold timing of 1/2/1. An asynchronous read proceeds as follows:

- At the beginning of the setup period
  - /CE becomes active low.
  - /AOE becomes active low.
  - /BE[3:0] becomes valid.
  - EA becomes valid.
  - ‘C6201/’C6202/’C6701: For the first access, setup has a minimum value of 2; after the first access, setup has a minimum value of 1 (see Figure 8).
  - ‘C6211/’C6711: Setup is always a minimum of 1 (see Figure 9).
- At the beginning of a strobe period
  - /ARE becomes active low.
- At the beginning of a hold period
  - /ARE becomes inactive high.
  - Data is sampled on the CLKOUT1 rising edge concurrent with the beginning of the hold period (end of the strobe period), just prior to the /ARE low-to-high transition.
- At the end of the hold period
  - /AOE becomes inactive as long as another read access to the same /CE space is not scheduled for the next cycle.
  - ‘C6201/’C6202 /’C6701: After the last access (burst transfer or single access) CE stays active for seven minus the value of read-hold cycles. For example, if READ HOLD = 1, CE stays active for six more cycles. This does not affect performance but merely reflects the EMIF overhead. (see Figure 8)

- ‘C6211/’C6711: CE goes inactive at the end of the hold period (see Figure 9).

Figure 8. ‘C6201/’C6202/’C6701 Asynchronous Read Timing Example (1/2/1)

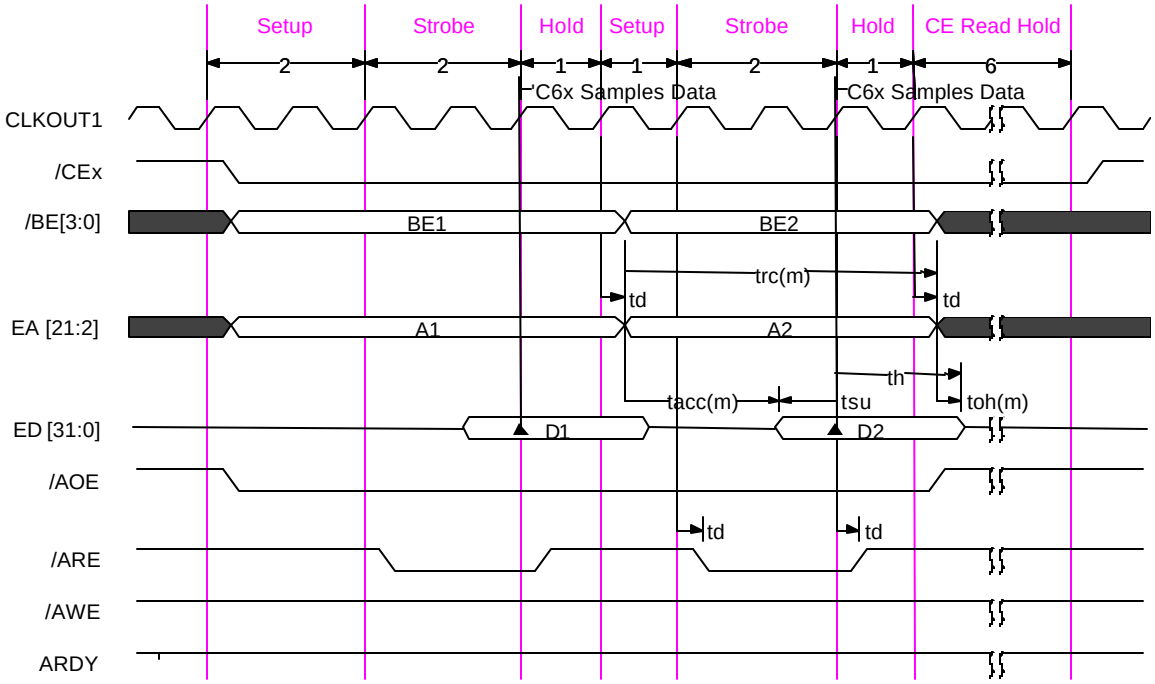
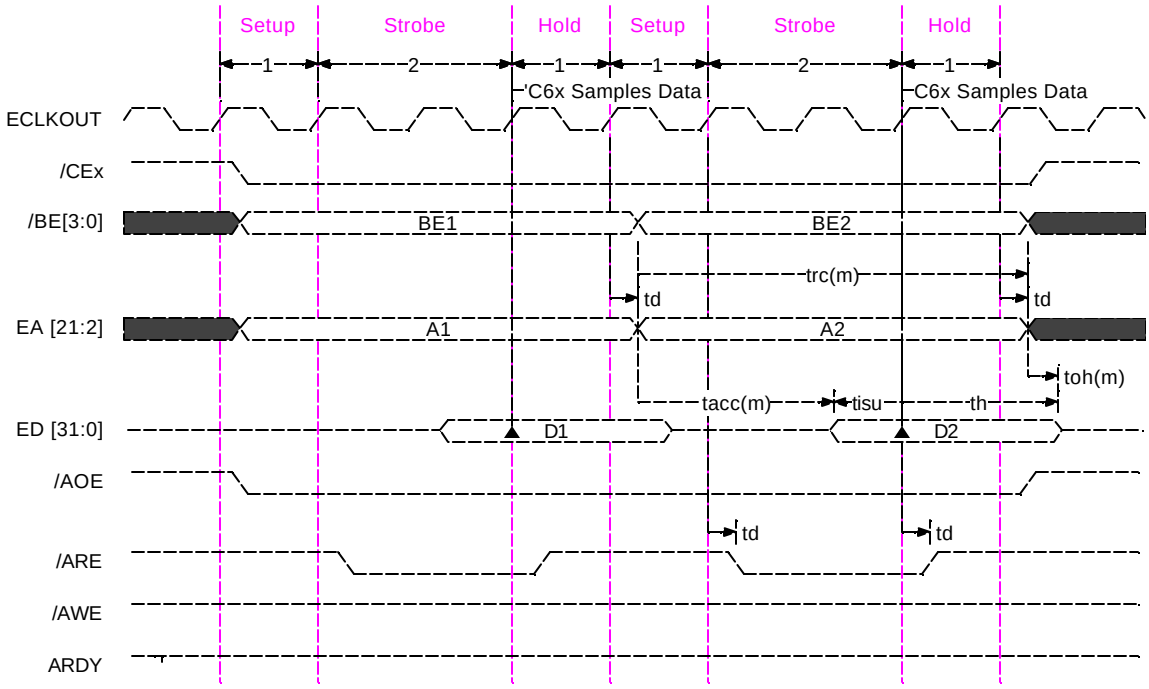


Figure 9. 'C6211/'C6711 Asynchronous Read Timing Example (1/2/1)



Setting Read Parameters for a Specific Asynchronous SRAM

Notice in Figure 8 and Figure 9 that the actual timing used by the C6000 to determine when read data is valid is based on the /ARE signal. Data is actually read on the rising clock edge corresponding to the cycle prior to which /ARE goes high, which is the end of the STROBE period. However, Figure 1 shows that /ARE is not connected to asynchronous SRAM. This is pointed out to stress the significance of the SETUP, STROBE, and HOLD times for the C6000 and compare them to the significant timing parameters of actual ASRAM.

ASRAM is not synchronized to any clock; however, it does have a maximum access time (t_{acc}) that relates when the output data is valid after receiving the required inputs. Thus, the data should be sampled at a time t_{acc} plus t_{isu} after the inputs are valid, which, as mentioned, should correspond to the end of the strobe period.

Therefore, when defining the parameters for the C6000 for SETUP, STROBE, and HOLD, the following constraints apply:

- SETUP + STROBE ≥ ($t_{acc(m)}$ + t_{su} + t_{dmax})/t_{cyc} (Note that t_{skew} is not used because t_{dmax} is used.)
- SETUP + STROBE + HOLD ≥ ($t_{rc(m)}$ + t_{skew})/t_{cyc}
- HOLD ≥ (t_h – t_{dmin} – $t_{oh(m)}$)/t_{cyc} (Note that t_{skew} is not used because t_{dmin} is used.)

Normally, SETUP can be set to 1 cycle, then STROBE can be solved for using constraint (1). HOLD can then be solved for using constraint (2). Of course, the smallest value possible should be used for all three parameters to satisfy the constraints while giving the necessary timing margin, because normally speed is an important consideration when accessing memory.

Asynchronous Writes

Figure 10 illustrates back-to-back asynchronous write with a setup/strobe/hold of 1/1/1. An asynchronous write proceeds as follows.

- At the beginning of the setup period
  - /CE becomes active low.
  - /BE[3:0] becomes valid.
  - EA becomes valid.
  - ED becomes valid.
  - ‘C6201/’C6202/’C6701: For the first access, setup has a minimum value of 2; after the first access setup has a minimum value of 1 (see Figure 10).
  - ‘C6211/’C6711: Setup is always a minimum of 1 (see Figure 11).
- At the beginning of a strobe period
  - /AWE becomes active low.
- At the beginning of a hold period
  - /AWE becomes inactive high.
- At the end of the hold period
  - ED goes into the high-impedance state only if another write to the same /CE space is not scheduled for the next cycle.
  - ‘C6201/’C6202/’C6701: If no write accesses are scheduled for the next cycle and write HOLD is set to 1 or greater, CE will stay active for three cycles after the programmed HOLD period. If write HOLD is set to 0, /CE will stay active for four more cycles. This does not affect performance but merely reflects the EMIF overhead. (see Figure 10)
  - ‘C6211/’C6711: CE goes inactive at the end of the hold period (see Figure 11).

Figure 10. 'C6201/'C6202/'C6701 Asynchronous Write Timing Example (1/1/1)

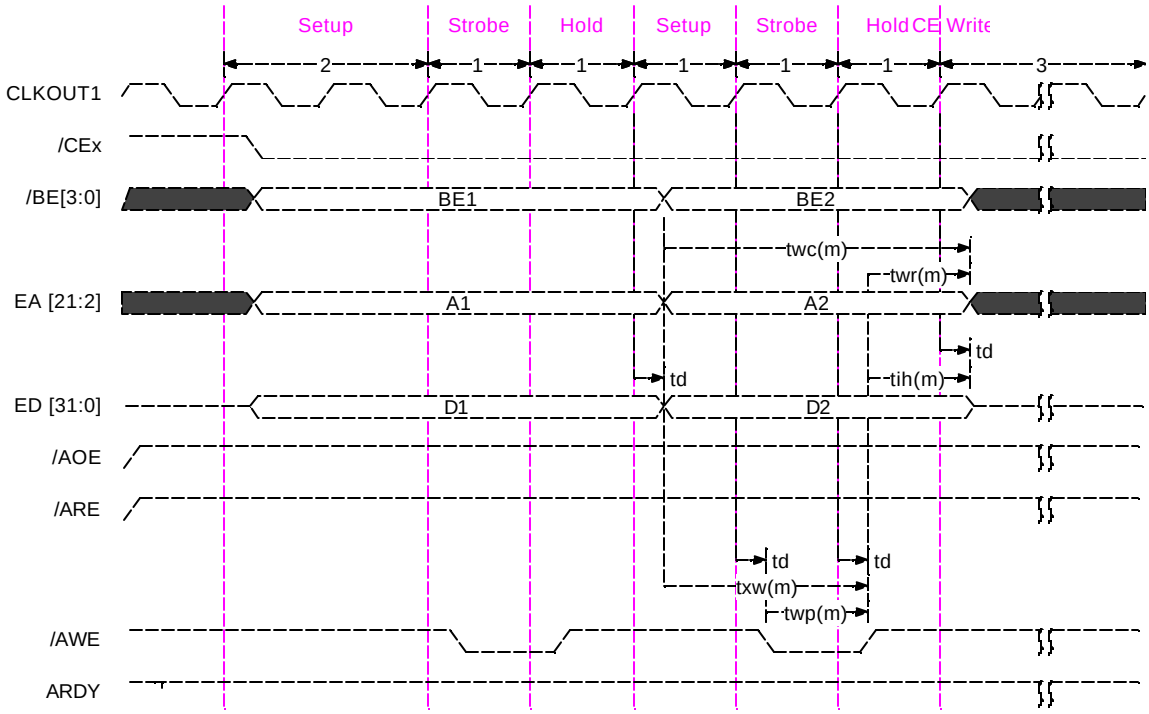
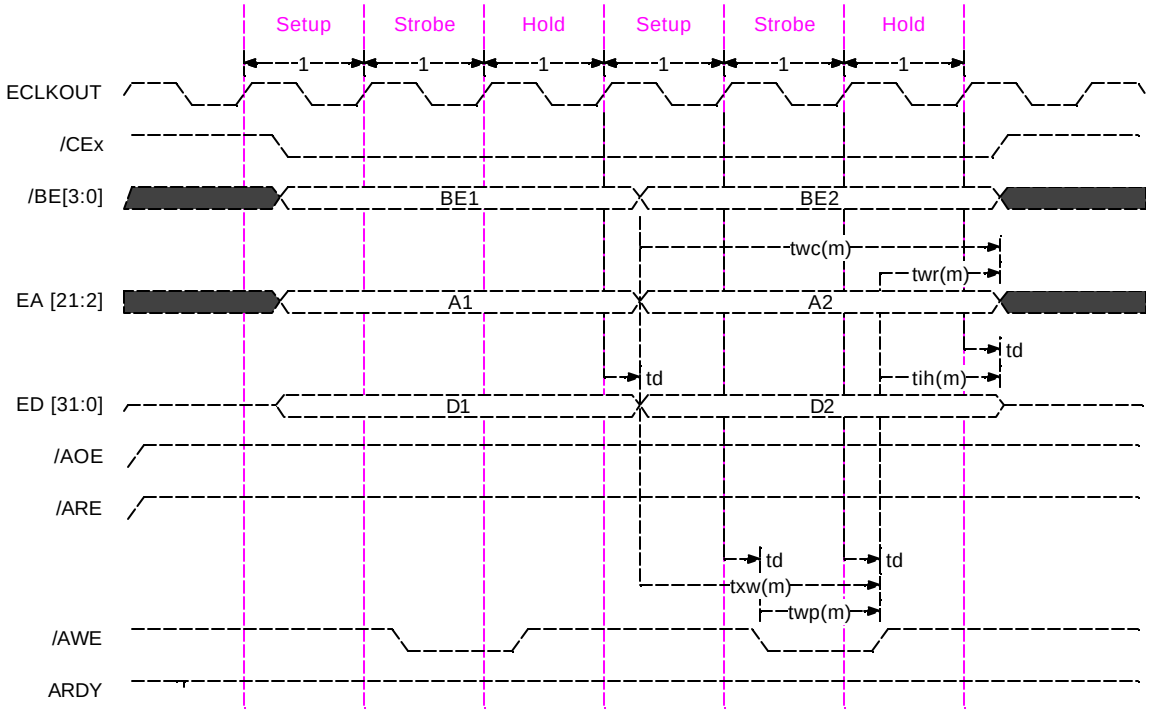


Figure 11. 'C6211/'C6711 Asynchronous Write Timing Example (1/1/1)



Setting Write Parameters for a Specific Asynchronous SRAM

For an ASRAM write, the SETUP, STROBE, and HOLD parameters should be set according to the following constraints:

1) STROBE ≥ $(t_{wp(m)})/t_{cyc}$. Note that t_{skew} is not included because $t_{wp(m)}$ is only relative to a single signal (AWE).

2) SETUP + STROBE ≥ $(t_{xw(m)} + t_{skew}) / t_{cyc}$

3) HOLD ≥ $(\max(t_{ih(m)}, t_{wr(m)}) + t_{skew})/t_{cyc}$

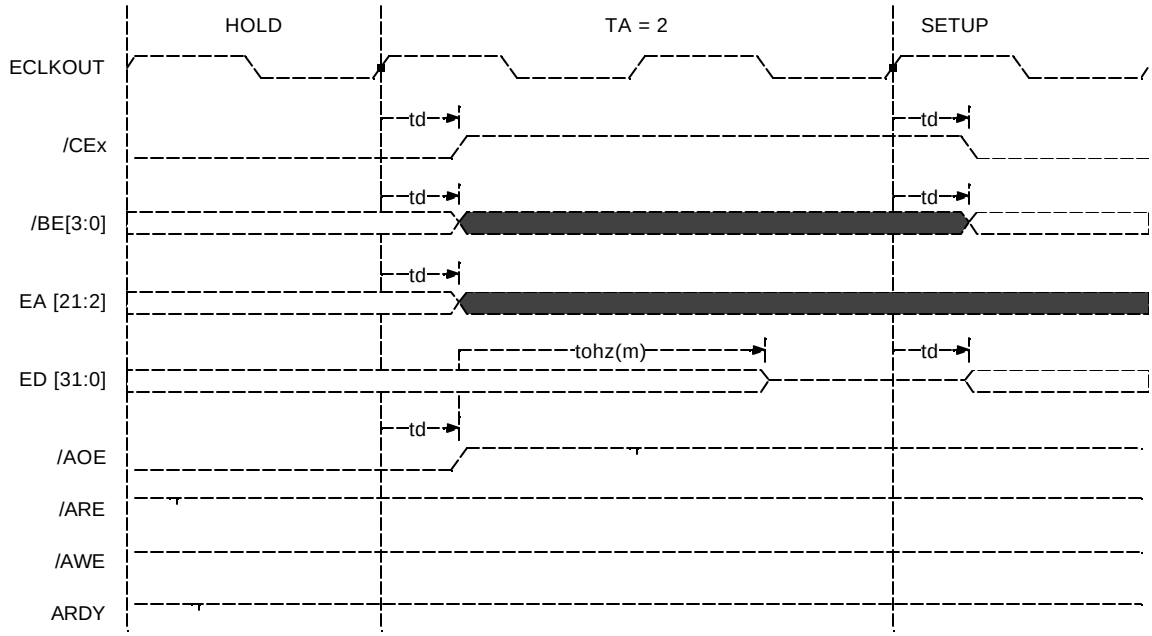
4) SETUP + STROBE + HOLD ≥ $(t_{wc(m)} + t_{skew})/t_{cyc}$

Read to Write Timing for 'C6211/'C6711

The 'C6211/'C6711 EMIF offers an additional parameter, TA, which defines the turnaround time between read and write cycles. This parameter protects against the situation in which the output turn off time of the memory is longer than the time it takes to start the next write cycle. If this were the case, the C6211/'C6711 could be driving data at the same time as the memory, causing contention on the bus.

The fact that the 'C6201/'C6202/'C6701 asynchronous interface does not have this feature does not cause any problems because the read cycle of these devices append a CE hold period that protects against bus contention.

Figure 12. Turnaround Time on 'C6211/'C6711



Setting TA Parameters for a Specific Asynchronous SRAM

The Turnaround time on the 'C6211/'C6711 should be set as follows:

$TA >= (t_{skew} + t_{ohz(m)})/ t_{cvc}$

Full Examples

This section walks through the configuration steps required to implement Toshiba's TC55V1664FT-12 ASRAM with the 'C6201B and IDT's IDT71V016S25 ASRAM with the 'C6211. Both of these SRAMs are 64k x 16 devices, with access times of 12 ns and 25 ns respectively.

Register Configuration for Toshiba's TC55V1664FT-12 With the 'C6201B

For the 'C6201B interface, the following assumptions are used:

- ASRAM is used in address space CE0.
- CPU clock speed is 200 MHz, therefore the CLKOUT1 speed is 5 ns and t_{cyc} = 5 ns.
- The physical interface is the same as shown in Figure 1.

Table 9 and Table 10 summarize the timing characteristics of the 'C6201B asynchronous interface. Table 11 and Table 12 summarize the timing characteristics of the TC55V1664BFT-12, which will be used to calculate the values for the CE0 pace configuration register. This data was taken from the TMS320C6201/6201B Fixed-Point Digital Signal Processors data sheet and the *TC55V1664BFT-12 Data Sheet*.

Table 9. 'C6201B EMIF—Input Requirements

		MIN	MAX	UNIT
t_{su}	Setup time, read ED before CLKOUT1 high	4		ns
t_h	Data hold time, read D after CLKOUT1 high	0.8		

Table 10. 'C6201B EMIF—Output Timing Characteristics

		MIN	MAX	UNIT
t_d	Output delay time, CLKOUT1 high to output signal valid	-0.2	4	ns

Table 11. ASRAM Input Requirements From EMIF for TC55V1664BFT-12

		MIN	MAX	UNIT
$t_{xw(m)}$	Time from control/data signals active to /AWE inactive	8		ns
$t_{wp(m)}$	Write pulse width	8		ns
$t_{ih(m)}$, $t_{wr(m)}$	Maximum of either write recovery time or data hold time	0		ns
$t_{rc(m)}$	Length of the read cycle	12		ns
$t_{wc(m)}$	Length of the write cycle	12		ns

Table 12. ASRAM—Output Timing Characteristics for TC55V1664FT-12

		MIN	MAX	UNIT
$t_{acc(m)}$	Access time from EA, /BE, /AOE, /CE active to ED valid		12	ns
$t_{oh(m)}$	Output hold time	3		

Read Calculations

- **SETUP = 1**, based on the suggestion stated in the section, Setting Read Parameters for a Specific Asynchronous SRAM.
- SETUP + STROBE ≥ $(t_{acc(m)} + t_{su} + t_{dmax})/t_{cyc}$

  Therefore,

  STROBE ≥ $(t_{acc(m)} + t_{su} + t_{dmax})/t_{cyc}$ – SETUP

  ≥ (12 ns + 4 ns + 4 ns)/ 5 ns -1

  ≥ 4 cycles - 1 cycle = 3 cycles

  STROBE = 4 cycles because a margin of 0 ns is not acceptable; t_{margin} = 5 ns
- SETUP + STROBE + HOLD ≥ $(t_{rc(m)} + t_{skew})/t_{cyc}$

  Therefore,

  HOLD ≥ $(t_{rc(m)} + t_{skew})/t_{cyc}$ – SETUP - STROBE

  ≥ (12ns + 2ns)/5ns – 1 – 4 = -2.2 cycles

  HOLD = 0 cycles because it cannot be negative;t_{margin}=11 ns
- HOLD ≥ $(t_h – t_{dmin} - t_{oh(m)})/t_{cyc}$

  Therefore,

  HOLD ≥ $(t_h – t_{dmin} – t_{oh(m)})/t_{cyc}$

  ≥ (0 – (-0.2ns) – 3 ns)/ 5ns = -0.6 cycles

  The previously calculated hold value satisfies this condition with t_{margin} = 3 ns.

With the settings specified in bold, the margin recommended is met.

Write Calculations

- STROBE $\geq (t_{wp(m)})/t_{cyc}$

  $\geq$ (8ns)/ 5ns = 1.6 cycles

  STROBE = 2 cycles; t_{margin} = 2 ns

- SETUP + STROBE $\geq (t_{xw(m)} + t_{skew})/t_{cyc}$

  Therefore,

  SETUP $\geq (t_{xw(m)} + t_{skew})/t_{cyc}$ – STROBE

  = (8ns + 2ns)/5ns – 2 cycles

  = 0.0 cycles

  SETUP = 1 cycle, minimum value; t_{margin} = 5 ns

- HOLD $\geq (\max(t_{ih(m)}, t_{wr(m)}) + t_{skew})/t_{cyc}$

  $\geq$ (0 + 2ns)/5 ns = 0.4 cycles

  HOLD = 1 cycles; t_{margin} = 3 ns. The value of HOLD is extended to 1 cycle to provide additional timing margin.

- SETUP + HOLD + STROBE $\geq t_{wc}$

  This requirement is satisfied. The sum of the three parameters is 4 cycles, which is greater than 12 ns (2.4 cycles). t_{margin}=8 ns

Using the above calculations, the CE space control register can now be properly configured. Figure 13 shows the CE0 space control register with the properly assigned values for each field. MTYPE = 010 identifies the memory in this address space as 32-bit-wide asynchronous memory; the other fields are used as calculated above.

Figure 13. EMIF CE0 Space Control Register Diagram for TC55V1664FT-12

31 – 28	27 – 22	21 – 20	19 – 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
0001	000010	01	0001

15 – 14	13 – 8	7	6 – 4	3 – 2	1 – 0
Reserved	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	000100	0	010	00	00

Sample Code

The following code segment sets up the EMIF as described above using the TMS320C6000 Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.     /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Configure CE0 as ASRAM  */
LOAD_FIELD(&ce0_ctrl, MTYPE_32ASYNC, MTYPE       , MTYPE_SZ       );
LOAD_FIELD(&ce0_ctrl, 1            , READ_SETUP  , READ_SETUP_SZ  );
LOAD_FIELD(&ce0_ctrl, 4            , READ_STROBE , READ_STROBE_SZ );
LOAD_FIELD(&ce0_ctrl, 0            , READ_HOLD   , READ_HOLD_SZ   );
LOAD_FIELD(&ce0_ctrl, 1            , WRITE_SETUP , WRITE_SETUP_SZ );
LOAD_FIELD(&ce0_ctrl, 2            , WRITE_STROBE, WRITE_STROBE_SZ);
LOAD_FIELD(&ce0_ctrl, 1            , WRITE_HOLD  , WRITE_HOLD_SZ  );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                  sdram_ctrl, sdram_ref);
.
.     /*OTHER USER CODE*/
.
```

Register Configuration for IDT's IDT71V016S25 With the 'C6211

For the 'C6211 interface, the following assumptions are used:

- ASRAM is used in address space CE0.
- EMIF clocked by ECLKIN = 100 MHz, therefore t_{cyc} = 10 ns.
- The physical interface is the same as shown in Figure 1.

Table 13 and Table 14 summarize the timing characteristics of the 'C6211 asynchronous EMIF interface. Table 15 and Table 16 summarize the timing characteristics of the IDT71V016S25, which is used to calculate the values for the CE0 space configuration register. This data was taken from the *TMS320C6211 Fixed-Point Digital Signal Processor* data sheet and the *IDT71V016 Data Sheet*. Note that for this example, ECLKIN is driven from an external source at its maximum frequency of 100 MHz. This implies t_{cyc} = 10 ns.

Table 13. 'C6211 EMIF—Input Requirements

		MIN	MAX	UNIT
t_{su}	Setup time, read ED before CLKOUT1 high	1.5		ns
t_h	Data hold time, read D after CLKOUT1 high	1.0		ns

Table 14. 'C6211 EMIF—Output Timing Characteristics

		MIN	MAX	UNIT
t_d	Output delay time, CLKOUT1 high to output signal valid	1.5	6	ns

Table 15. ASRAM Input Requirements From EMIF for IDT71V016S25

		MIN	MAX	UNIT
$t_{xw(m)}$	Time from control/data signals active to /AWE inactive	14		ns
$t_{wp(m)}$	Write pulse width	14		ns
$t_{ih(m)}$, $t_{wr(m)}$	Maximum of either write recovery time or data hold time	0		ns
$t_{rc(m)}$	Length of the read cycle	25		ns
$t_{wc(m)}$	Length of the write cycle	25		ns

Table 16. ASRAM—Output Timing Characteristics for IDT71V016S25

		MIN	MAX	UNIT
$t_{acc(m)}$	Access time, from EA, /BE, /AOE, /CE active to ED valid		25	ns
$t_{oh(m)}$	Output hold time	5		ns
$t_{ohz(m)}$	Output turn off time		8	ns

Read Calculations

- **SETUP = 1**, based on the suggestion stated in the section, *Setting Read Parameters for a Specific Asynchronous SRAM*.
- SETUP + STROBE ≥ $(t_{acc(m)} + t_{su} + t_{dmax})/t_{cyc}$

  Therefore,

  STROBE ≥ $(t_{acc(m)} + t_{su} + t_{dmax})/t_{cyc}$ – SETUP

  ≥ (25 ns + 1.5 ns + 6 ns)/ 10 ns – 1

  ≥ 3.25 cycles – 1 cycle = 2.25 cycles

  STROBE = 3 cycles; t_{margin} = 7.5 ns
- SETUP + STROBE + HOLD ≥ $(t_{rc(m)} + t_{skew})/t_{cyc}$

  Therefore,

  HOLD ≥ $(t_{rc(m)} + t_{skew})/t_{cyc}$ – SETUP – STROBE

  ≥ (25 ns + 2 ns)/10 ns – 1 – 3 = –1.3 cycles

  HOLD = 0 cycles because it cannot be negative; t_{margin}=13 ns
- HOLD ≥ $(t_h – t_{dmin} – t_{oh(m)})/t_{cyc}$

  Therefore,

  HOLD ≥ $(t_h – t_{dmin} – t_{oh(m)})/t_{cyc}$

  ≥ (0 – 1.5 ns – 5 ns)/10 ns = -0.65 cycles

  The previously calculated hold value satisfies this condition with t_{margin} = 6.5 ns.

With the settings specified in bold, the margin recommended is met.

Write Calculations

- STROBE ≥ $(t_{wp(m)})/t_{cyc}$

  ≥ (14 ns)/10 ns = 1.4 cycles

  STROBE = 2 cycles; t_{margin} = 6 ns

- SETUP + STROBE ≥ $(t_{xw(m)} + t_{skew})/t_{cyc}$

  Therefore,

  SETUP ≥ $(t_{xw(m)} + t_{skew})/t_{cyc}$ - STROBE

  = (14 ns + 2 ns)/10 ns – 2 cycles

  = –0.4 cycles

  SETUP = 1 cycle, minimum value; t_{margin} = 14 ns

- HOLD ≥ $(\max(t_{ih(m)}, t_{wr(m)}) + t_{skew})/t_{cyc}$

  ≥ (0 + 2 ns)/10 ns = 0.2 cycles

  HOLD = 1 cycle; t_{margin} = 8 ns

- SETUP + HOLD + STROBE ≥ t_{wc}

  This requirement is satisfied. The sum of the three parameters is 4 cycles, which is greater than 25 ns (2.5 cycles). t_{margin} = 15 ns

Turnaround Calculation

- TA ≥ $(t_{skew} + t_{ohz(m)})/t_{cyc}$

  Therefore,

  TA ≥ (2 ns + 8 ns)/10 ns

  = 1 cycle.

  TA = 2 cycles because a margin of 0 ns is normally not acceptable; t_{margin} = 10 ns

Using the previous calculations, the CE space control register can now be properly configured. Figure 14 shows the CE0 space control register with the properly assigned values for each field. MTYPE = 0010 identifies the memory in this address space as 32-bit-wide asynchronous memory; the other fields are used as calculated above.

Figure 14. EMIF CE0 Space Control Register Diagram for IDT71V016S25

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
0001	000010	01	0001

15 14	13 8	7 4	3	2 0
TA	READ STROBE	MTYPE	WH MSB	READ HOLD
10	000011	0010	00	00

Sample Code

The following code segment sets up the EMIF as described above using the TMS320C6000 Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.     /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Configure CE0 as ASRAM, w/ calculated timings */
LOAD_FIELD(&ce0_ctrl, MTYPE_32ASYNC, MTYPE       , MTYPE_SZ       );
LOAD_FIELD(&ce0_ctrl,  1           , READ_SETUP  , READ_SETUP_SZ  );
LOAD_FIELD(&ce0_ctrl,  3           , READ_STROBE , READ_STROBE_SZ );
LOAD_FIELD(&ce0_ctrl,  0           , READ_HOLD   , READ_HOLD_SZ   );
LOAD_FIELD(&ce0_ctrl,  1           , WRITE_SETUP , WRITE_SETUP_SZ );
LOAD_FIELD(&ce0_ctrl,  2           , WRITE_STROBE, WRITE_STROBE_SZ);
LOAD_FIELD(&ce0_ctrl,  1           , WRITE_HOLD  , WRITE_HOLD_SZ  );
LOAD_FIELD(&ce0_ctrl,  2           , TURN_AROUND , TURN_AROUND_SZ );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                  sdram_ctrl, sdram_ref);
.
.     /*OTHER USER CODE*/
.
```

References

TMS320C6201/6201B Fixed-Point Digital Signal Processors Data Sheet, Literature number SPRS051, April 1999, Texas Instruments.

TMS320C6202 Fixed-Point Digital Signal Processor Data Sheet, Literature number SPRS072, January 1999, Texas Instruments.

TMS320C6211 Fixed-Point Digital Signal Processor Data Sheet, Literature number SPRS073, March 1999, Texas Instruments.

TMS320C6701 Floating-Point Digital Signal Processor Data Sheet, Literature number SPRS067, March 1999, Texas Instruments.

TMS320C6711 Floating-Point Digital Signal Processor Data Sheet, Literature number SPRS088, March 1999, Texas Instruments.

TMS320C6000 Peripherals Reference Guide, Literature number SPRU190, March 1999, Texas Instruments.

TMS320C6000 Peripheral Support Library Programmers Reference, Literature number SPRU273, June 1998, Texas Instruments.

TC55V1664FT Data Sheet, Toshiba America, Inc., http://www.toshiba.com

IDT71V016 Data Sheet, Integrated Device Technology, Inc., http://www.idt.com